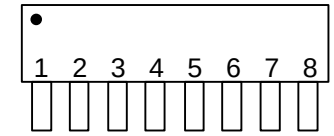
5-TAP, HCMOS-INTERFACED FIXED DELAY LINE (SERIES DDU222C)

FEATURES

- Five equally spaced outputs
- Very narrow device (SIP package)
- Stackable for PC board economy
- Input & outputs fully CMOS interfaced & buffered
- 10 T^2L fan-out capability

PACKAGES



DDU222F-xx Commercial
DDU222F-xxM Military

FUNCTIONAL DESCRIPTION

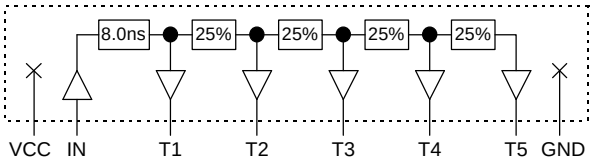
The DDU222C-series device is a 5-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T5), shifted in time by an amount given by the device dash number. For dash numbers less than 40, the total delay of the line is measured from T1 to T5, with the nominal value given by the dash number. The nominal tap-to-tap delay increment is given by 1/4 of this number. The inherent delay from IN to T1 is nominally 8.0ns. For dash numbers greater than or equal to 40, the total delay of the line is measured from IN to T5, with the nominal value given by the dash number. The nominal tap-to-tap delay increment is given by 1/5 of this number.

PIN DESCRIPTIONS

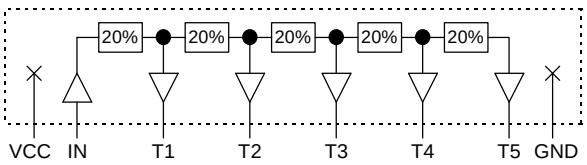
IN	Signal Input
T1-T5	Tap Outputs
VDD	+5 Volts
GND	Ground

SERIES SPECIFICATIONS

- **Minimum input pulse width:** 40% of total delay
- **Output rise time:** 8ns typical
- **Supply voltage:** 5VDC ± 5%
- **Supply current:** I_{CCL} = 40µa typical
  I_{CCH} = 10ma typical
- **Operating temperature:** 0° to 70° C
- **Temp. coefficient of total delay:** 300 PPM/°C



Functional diagram for dash numbers < 40



Functional diagram for dash numbers >= 40

DASH NUMBER SPECIFICATIONS

Part Number	Total Delay (ns)	Delay Per Tap (ns)
DDU222C-10	10 ± 2.0 *	2.5 ± 1.0
DDU222C-20	20 ± 2.0 *	5.0 ± 2.0
DDU222C-50	50 ± 3.0	10.0 ± 3.0
DDU222C-60	60 ± 3.0	12.0 ± 3.0
DDU222C-75	75 ± 4.0	15.0 ± 3.0
DDU222C-100	100 ± 5.0	20.0 ± 3.0
DDU222C-125	125 ± 6.5	25.0 ± 3.0
DDU222C-150	150 ± 7.5	30.0 ± 3.0
DDU222C-175	175 ± 8.0	35.0 ± 4.0
DDU222C-200	200 ± 10.0	40.0 ± 4.0
DDU222C-250	250 ± 12.5	50.0 ± 5.0

*** Total delay is referenced to first tap output**
Input to first tap = 8.0ns ± 2ns

NOTE: Any dash number between 10 and 250 not shown is also available.

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The DDU222C tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 40% of the total delay and periods as small as 80% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The DDU222C relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VDD to GND, located as close as possible to the VDD pin, is recommended. A wide VDD trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

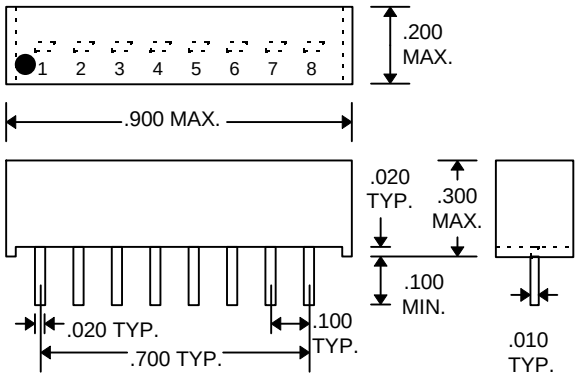
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

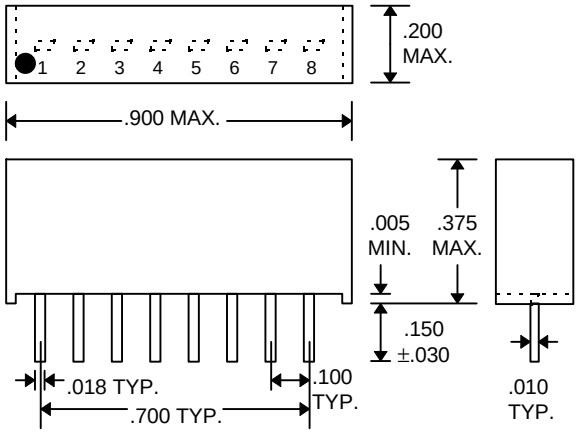
(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V_{OH}	3.98	4.4		V	V_{DD} = 5.0, I_{OH} = MAX V_{IH} = MIN, V_{IL} = MAX
Low Level Output Voltage	V_{OL}		0.15	0.26	V	V_{DD} = 5.0, I_{OL} = MAX V_{IH} = MIN, V_{IL} = MAX
High Level Output Current	I_{OH}			-4.0	mA	
Low Level Output Current	I_{OL}			4.0	mA	
High Level Input Voltage	V_{IH}	3.15			V	
Low Level Input Voltage	V_{IL}			1.35	V	
Input Current	I_{IH}			0.10	µA	V_{DD} = 5.0

PACKAGE DIMENSIONS



DDU222C-xx (Commercial)



DDU222C-xxM (Military)

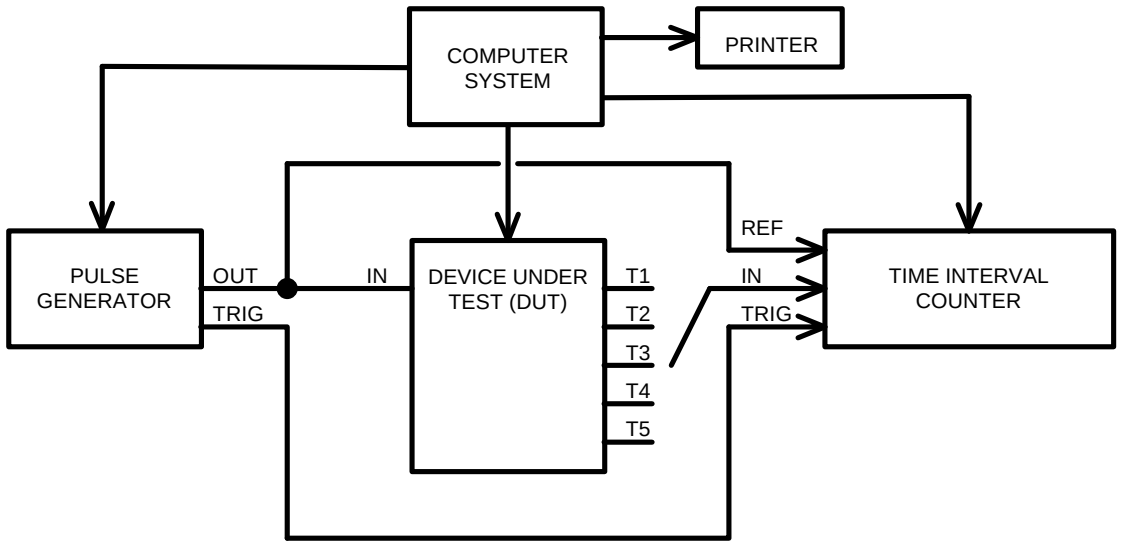
DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

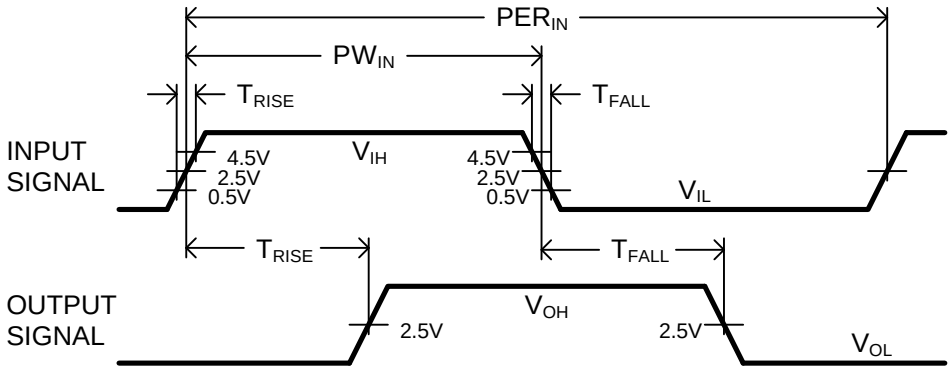
INPUT:	
Ambient Temperature:	25°C ± 3°C
Supply Voltage (VDD):	5.0V ± 0.1V
Input Pulse:	High = 5.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance:	50Ω Max.
Rise/Fall Time:	5.0 ns Max. (measured between 0.5V and 4.5V)
Pulse Width:	PW_{IN} = 1.5 x Total Delay
Period:	PER_{IN} = 10 x Total Delay

OUTPUT:	
Load:	1 FAST-TTL Gate
C_{load}:	5pf ± 10%
Threshold:	2.5V (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing