DS1210
Nonvolatile Controller Chip

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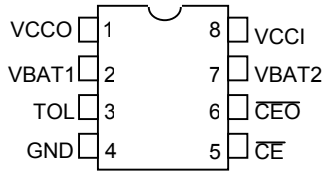
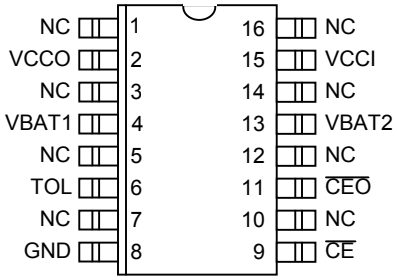
FEATURES
- Converts CMOS RAMs into Nonvolatile Memories
- Unconditionally Write Protects when V_{CC} is Out-of-Tolerance
- Automatically Switches to Battery when Power-Fail Occurs
- Space-Saving 8-Pin DIP
- Consumes <100nA of Battery Current
- Tests Battery Condition on Power up
- Provides for Redundant Batteries
- Optional 5% or 10% Power-Fail Detection
- Low Forward Voltage Drop on the V_{CC} Switch
- Optional 16-Pin SOIC Surface Mount Package
- Optional Industrial (N) Temperature Range of -40°C to +85°C

PIN ASSIGNMENT



DS1210 8-pin DIP (300-mil)
See Mech. Drawings Section



DS1210S 16-pin SOIC (300-mil)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CCO}	- RAM Supply
V_{BAT1}	- + Battery 1
TOL	- Power Supply Tolerance
GND	- Ground
$\overline{CE}$	- Chip Enable Input
$\overline{CEO}$	- Chip Enable Output
V_{BAT2}	- + Battery 2
V_{CCI}	- + Supply
NC	- No Connect

DESCRIPTION

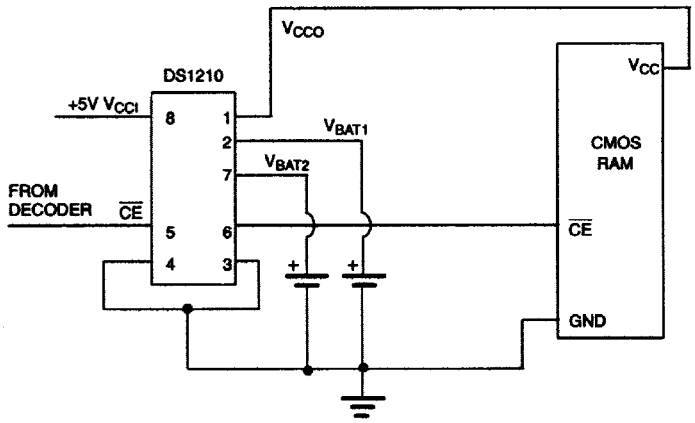
The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power-fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power-fail and inhibits chip enable ($\overline{CEO}$). The third function of write protection is accomplished by holding the $\overline{CEO}$ output signal to within 0.2 volts of the V_{CCI} or battery supply. If $\overline{CE}$ input is low at the time power-fail detection occurs, the $\overline{CEO}$ output is kept in its present state until $\overline{CE}$ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power-fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V_{CCO}, then power-fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CE}$ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V_{BAT2} pin will not activate a battery-fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery backup. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the $\overline{CEO}$ and V_{CCO} will be forced to V_{OL}. When the batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not provide battery back-up until V_{CCI} exceeds V_{CCTP}, as set by the T_{OL} pin, and then falls below V_{BAT}.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power-up to prevent spurious writes.

SECTION A - BATTERY BACKUP Figure 1

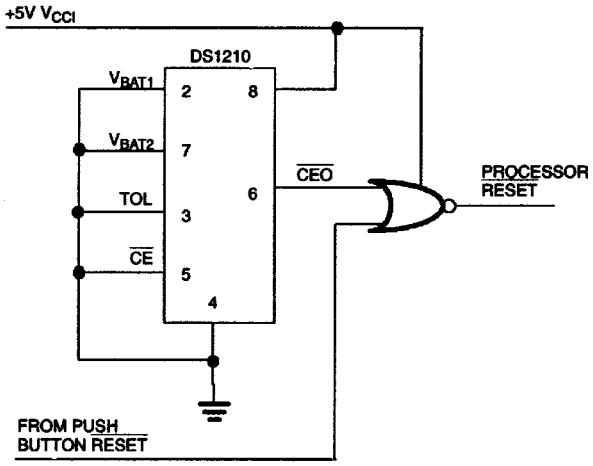


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	100 nA
RAM I_{CC02}	10 µA
Total Drain	10.1 µA

SECTION B - PROCESSOR RESET



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C, -40°C to +85°C for N parts
Storage Temperature	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (See Note 9)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(See Note 9; V_{CCI} = 4.75 to 5.5V PIN 3 = GND)
(V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CEO}$ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CEO}$ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CCO})	V_{CCTP}	4.25	4.37	4.49	V	1

(See Note 9; V_{CCI} = < V_{BAT})

$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	7
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2, 3
Battery Backup Current @ V_{CCO} = V_{BAT} – 0.3V	I_{CCO2}			50	µA	6, 7

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(See Note 9; V_{CCI} = 4.75V to 5.5V, PIN 3 = GND)

(V_{CCI} = 4.75V to 5.5V, PIN 3 = GND)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

(See Note 9; V_{CCI} = 4.75V, PIN 3 = GND; V_{CCI} < 4.5, PIN 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power-Down	t_F	300			µs	
V_{CC} Slew Rate Power-Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power-Down	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	8

NOTES:

1. All voltages are referenced to ground.

2. Only one battery input is required. Unused battery inputs must be grounded.

3. Measured with V_{CCO} and $\overline{CEO}$ open.

4. I_{CC01} is the maximum average load which the DS1210 can supply to the memories.

5. Measured with a load as shown in Figure 2.

6. I_{CC02} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.

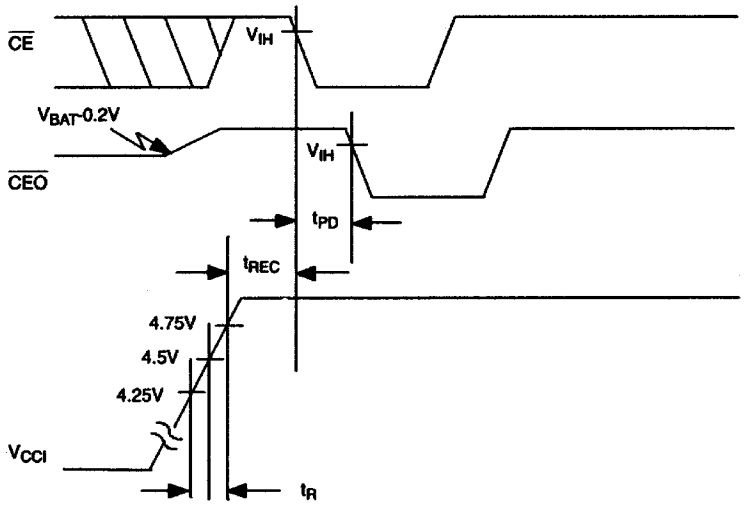
7. t_{CE} max. must be met to ensure data integrity on power loss.

8. $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

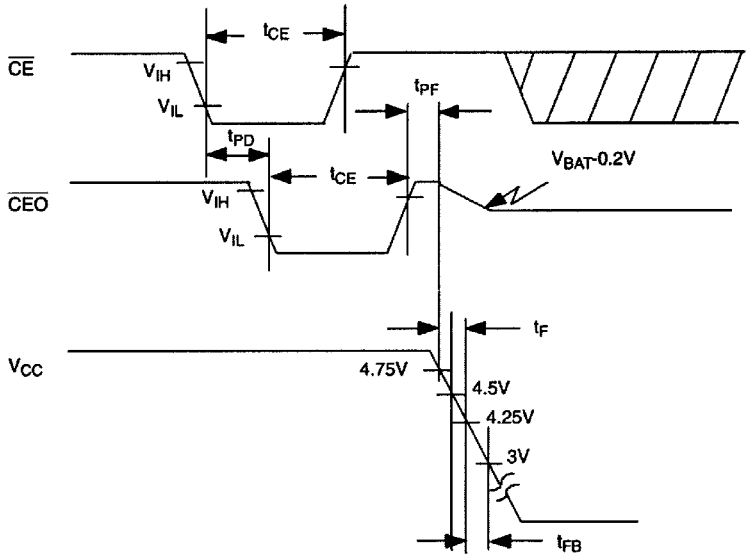
9. All AC and DC electrical characteristics are valid for the full temperature range. For commercial products, this range is 0 to +70°C. For industrial products (N), this range is -40°C to +85°C.

10. DS1210 is recognized by Underwriters Laboratory (U.L.®) under file E99151.

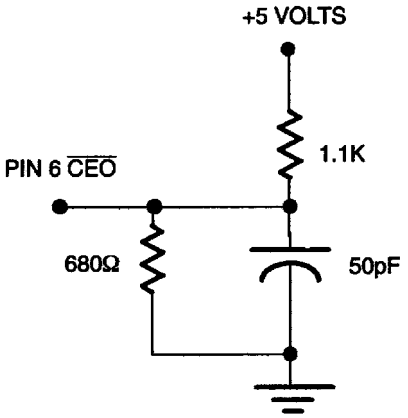
TIMING DIAGRAM: POWER-UP



TIMING DIAGRAM: POWER-DOWN



OUTPUT LOAD Figure 2



DS1210

Part Number Table

Notes:

1. See the DS1210 QuickView Data Sheet for further information on this product family or download the DS1210 full data sheet (PDF, 144kB).
2. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
3. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See full data sheet or Part Naming Conventions.
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
DS1210N+			PDIP;8 pin;300 Dwg: 56-G5005-000A (PDF) Use pkgcode/variation: P8+9*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
DS1210+			PDIP;8 pin;300 Dwg: 56-G5005-000A (PDF) Use pkgcode/variation: P8+9*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
DS1210N			PDIP;8 pin;300 Dwg: 56-G5005-000A (PDF) Use pkgcode/variation: P8-9*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
DS1210S/T&R			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16-11*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
DS1210S			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16-11*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
DS1210S+TRL			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16+12*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
DS1210S+			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16+12*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis

DS1210SN+			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16+2*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
DS1210SN/T&R			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16-11*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
DS1210SN			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16-11*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
DS1210SN+T&R			SOIC;16 pin;300 Dwg: 56-G4009-001B (PDF) Use pkgcode/variation: W16+11*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis

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