3A, Rad Hard, Positive, Ultra Low Dropout Regulator

ISL75051SRH

The ISL75051SRH is a radiation hardened low-voltage, high-current, single-output LDO specified for up to 3.0A of continuous output current. These devices operate over an input voltage range of 2.2V to 6.0V and are capable of providing output voltages of 0.8V to 5.0V adjustable based on resistor divider setting. Dropout voltages as low as 65mV can be realized using the device.

The OCP pin allows the short circuit output current limit threshold to be programmed by means of a resistor from the OCP pin to GND. The OCP setting range is from 0.5A minimum to 8.5A maximum. The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value. It subsequently enters an ON/OFF cycle until the fault is removed. The ENABLE feature allows the part to be placed into a low current shutdown mode that typically draws about 1µA. When enabled, the device operates with a typical low ground current of 11mA, which provides for operation with low quiescent power consumption.

The device is optimized for fast transient response and single event effects. This reduces the magnitude of SET seen on the output. Additional protection diodes and filters are not needed. The device is stable with tantalum capacitors as low as 47µF and provides excellent regulation all the way from no load to full load. Programmable soft-start allows the user to program the inrush current by means of the decoupling capacitor value used on the BYP pin.

Applications

- LDO Regulator for Space Application
- DSP, FPGA and µP Core Power Supplies
- Post-regulation of Switched Mode Power Supplies
- Down-hole Drilling

Features

- DLA SMD#5962-11212
- Output Current Up to 3.0A at T_J = 150°C
- Output Accuracy ±1.5% over MIL Temp Range
- Ultra Low Dropout:
  - 65mV Typ Dropout at 1.0A
  - 225mV Typ Dropout at 3.0A
- Noise of 100μV_{RMS} from 300Hz to 300kHz
- SET Mitigation with No Added Filtering/Diodes
- Input Supply Range: 2.2V to 6.0V
- Fast Load Transient Response
- Shutdown Current of 1µA Typ
- Output Adjustable Using External Resistors
- PSRR 66dB Typ @ 1kHz
- Enable and PGood Feature
- Programmable Soft-start/Inrush Current Limiting
- Adjustable Overcurrent Limit from 0.5A to 8.5A
- Over-temperature Shutdown
- Stable with 47µF Min Tantalum Capacitor
- 18 Ld Ceramic Flatpack Package
- Radiation Environment
  - High Dose . . . . . 100 krad(Si)
  - SET/SEL/SEB . . . . . .86 MeV·cm^2/mg

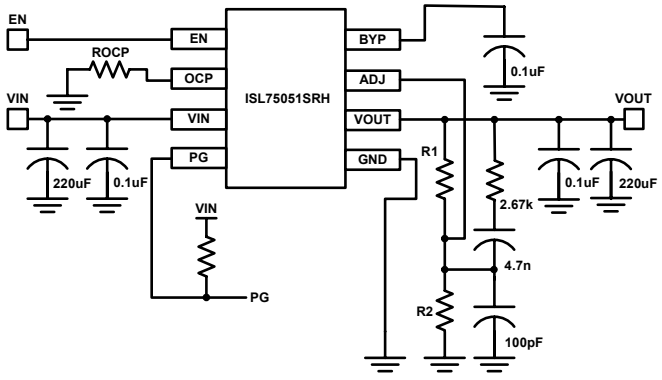


FIGURE 1. TYPICAL APPLICATION

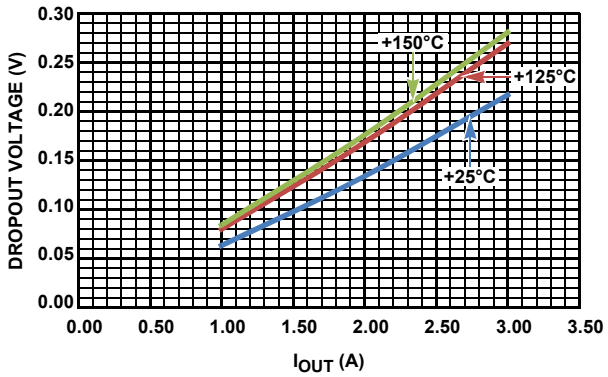
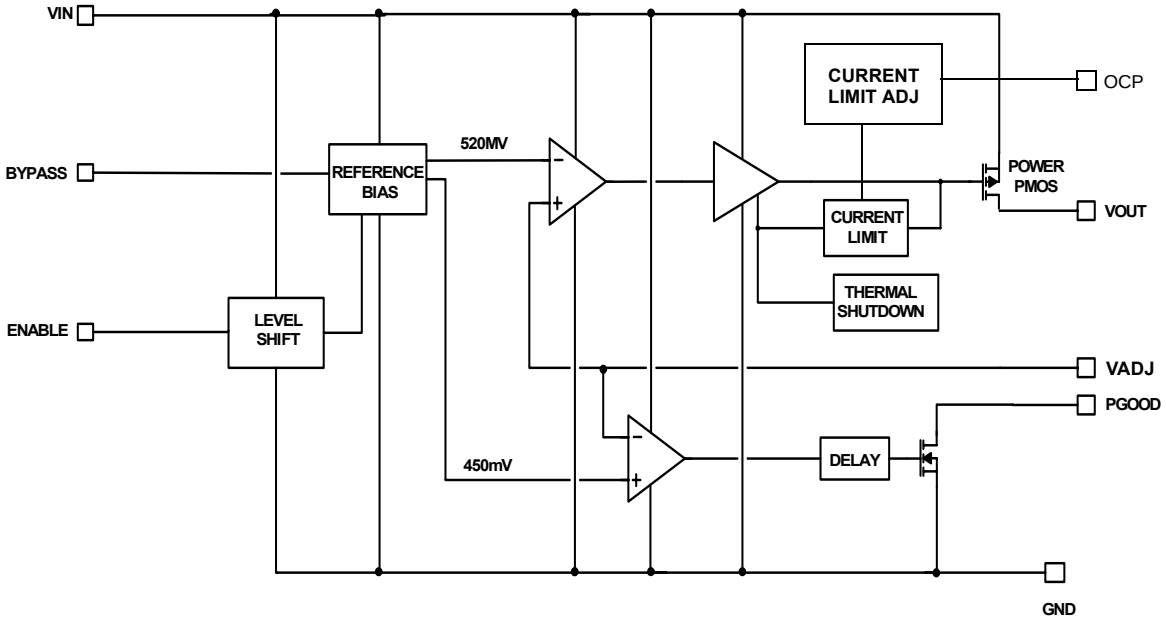
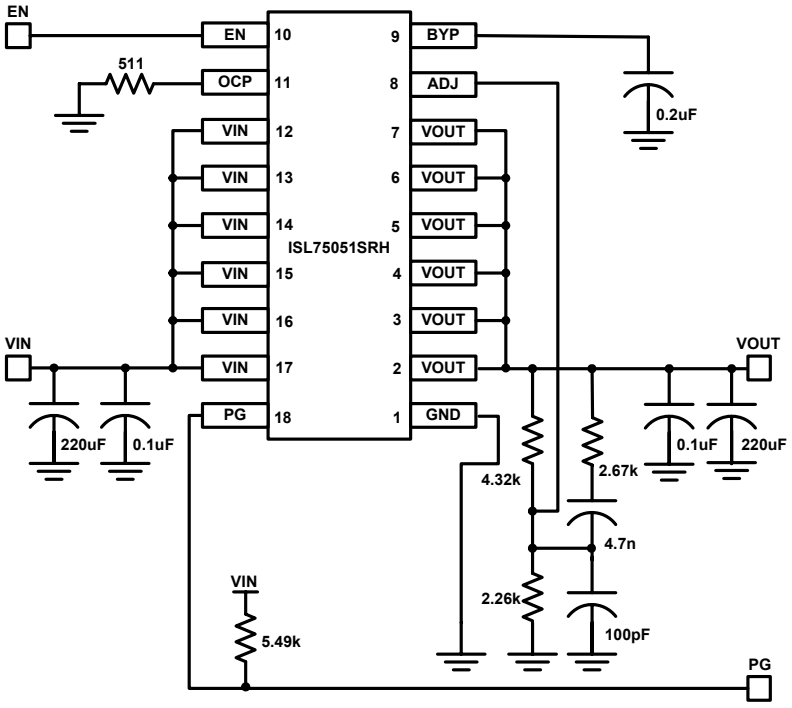


FIGURE 2. DROPOUT vs I_{OUT}

Block Diagram

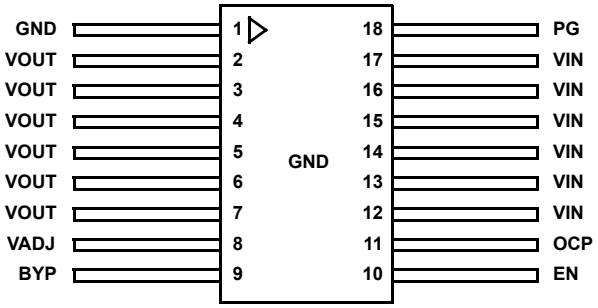


Typical Applications



Pin Configuration

ISL75051SRH
(18LD CDFP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
12, 13, 14 15, 16, 17	V_{IN}	Input supply pins
18	PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Must be grounded if not used.
1	GND	GND pin
2, 3, 4 5, 6, 7	V_{OUT}	Output voltage pins
8	VADJ	VADJ pin allows V_{OUT} to be programmed with an external resistor divider.
9	BYP	To filter the internal reference, connect a 0.1µF capacitor from BYP pin to GND.
10	EN	V_{IN} independent chip enable. TTL and CMOS compatible.
11	OCP	Allows current limit to be programmed with an external resistor.
Top Lid	GND	The top lid is connected to GND pin of the package.

Ordering Information

ORDERING NUMBER	PART NUMBER (NOTES 1, 2)	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
5962R1121201VXC	ISL75051SRHVF	-55 to +125	18 Ld CDFP	K18.D
5962R1121201QXC	ISL75051SRHQF	-55 to +125	18 Ld CDFP	K18.D
5962R1121201V9A	ISL75051SRHVX	-55 to +125	Die	
ISL75051SRHX/SAMPLE	ISL75051SRHX/SAMPLE	-55 to +125	Die Sample	
ISL75051SRHF/PROTO	ISL75051SRHF/PROTO	-55 to +125	18 Ld CDFP	K18.D
ISL75051SRHEVAL1Z	Evaluation Board			

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL75051SRH. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

V_{IN} Relative to GND (Note 3) . . . . . -0.3 to +6.7V
V_{OUT} Relative to GND (Note 3) . . . . . -0.3 to +6.7V
PG, EN, OCP/ADJ Relative to GND (Note 3) . . . . . -0.3 to +6.7VDC
Junction Temperature (T_J) . . . . . +175°C

Recommended Operating Conditions (Note 4)

Ambient Temperature Range (T_A) . . . . . -55°C to +125°C
Junction Temperature (T_J) (Note 3) . . . . . +150°C
V_{IN} Relative to GND . . . . . 2.2V to 6.0V
V_{OUT} Range . . . . . .0.8V to 5.0V
PG, EN, OCP/ADJ relative to GND . . . . . 0V to +6.0V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
18 Ld CDFP Package (Notes 5, 6)	28	4

Storage Temperature Range . . . . . -65°C to +150°C

Radiation Information

Max Total Dose
(Dose Rate = 50 - 300radSi/s . . . . . 100 krad (Si)
SET (V_{OUT} < ±5% During Events (Note 7) . . . . . 86MeV•cm^2/mg
SEL/B (No Latchup/Burnout . . . . . 86MeV•cm^2/mg
The output capacitance used for SEE testing is 220µF for C_{IN} and C_{OUT}, 200nF for BYPASS

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
4. Refer to "Thermal Guidelines" on page 12.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379
6. For θ_{JC}, the "case temp" location is the center of the package underside.
7. The device can work down to V_{OUT} = 0.8V; however, the SET performance of < ±5% at LET = 86MeV.cm^2/mg is guaranteed at V_{OUT} = >1.5V only. SET tests performed with 220µF 10V 25mΩ and 0.1µF CDR04 capacitor on the input and output.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: V_{IN} = V_{OUT} + 0.4V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 220µF 25mΩ and 0.1µF X7R, T_J = +25°C, I_L = 0A. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Applications Information" on page 11 of the datasheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A defines guaranteed limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} Resistor adjust to 0.52V, 1.5V and 1.8V				
		2.2V < V_{IN} < 3.6V; 0A < I_{LOAD} < 3.0A	**-1.5**	0.2	**1.5**	%
		V_{OUT} Resistor adjust to 5.0V				
		V_{OUT} + 0.4V < V_{IN} < 6.0V; 0A < I_{LOAD} < 3.0A	**-1.5**	0.2	**1.5**	%
Feedback Pin	V_{ADJ}	2.2V < V_{IN} < 6.0V; I_{LOAD} = 0A	**514.8**	520	**525.2**	mV
BYP Pin	V_{BYP}	2.2V < V_{IN} < 6.0V; I_{LOAD} = 0A		520		mV
DC Input Line Regulation		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.5V, +25°C & -55°C (Note 9)		1.13	3.5	mV
DC Input Line Regulation		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.5V, +125°C (Note 9)		1.13	8.0	mV
DC Input Line Regulation		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.8V, +25°C & -55°C (Note 9)		1.62	3.5	mV
DC Input Line Regulation		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.8V, +125°C (Note 9)		1.62	10.5	mV
DC Input Line Regulation		V_{OUT} + 0.4V < V_{IN} < 6.0V, V_{OUT} = 5.0V (Note 9)		12.50	**20.0**	mV
DC Output Load Regulation		V_{OUT} = 1.5V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V (Note 9)	**-4.0**	-0.8	**-0.1**	mV
DC Output Load Regulation		V_{OUT} = 1.8V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V (Note 9)	**-4.0**	-1.2	**-0.05**	mV
DC Output Load Regulation		V_{OUT} = 5.0V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V (Note 9)	**-15.0**	-6.0	**-0.05**	mV

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 220\mu F$ 25mΩ and 0.1µF X7R, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Applications Information" on page 11 of the datasheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Feedback Input Current		V_{ADJ} = 0.5V			**1**	µA
Ground Pin Current	I_Q	V_{OUT} = 1.5V; I_{LOAD} = 0A, V_{IN} = 2.2V		11	**12**	mA
Ground Pin Current	I_Q	V_{OUT} = 5.0V; I_{LOAD} = 0A, V_{IN} = 6.0V		16	**18**	mA
Ground Pin Current	I_Q	V_{OUT} = 1.5V; I_{LOAD} = 3.0A, V_{IN} = 2.2V		11	**13**	mA
Ground Pin Current	I_Q	V_{OUT} = 5.0V; I_{LOAD} = 3.0A, V_{IN} = 6.0V		16	**18**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0V, V_{IN} = 6.0V		1	**10**	µA
Dropout Voltage	V_{DO}	I_{LOAD} = 1.0A, V_{OUT} = 2.5V (Note 10)		65	**100**	mV
Dropout Voltage	V_{DO}	I_{LOAD} = 2.0A, V_{OUT} = 2.5V (Note 10)		140	**200**	mV
Dropout Voltage	V_{DO}	I_{LOAD} = 3.0A, V_{OUT} = 2.5V (Note 10)		225	**300**	mV
Output Short Circuit Current	ISCL	V_{OUT} = 0V, V_{IN} = 2.2V, R_{SET} = 5.11k		1.1		A
Output Short Circuit Current	ISCL	V_{OUT} = 0V, V_{IN} = 6.0V, R_{SET} = 5.11k		1.2		A
Output Short Circuit Current	ISCH	V_{OUT} = 0V, V_{IN} = 2.2V, R_{SET} = 511Ω		5.7		A
Output Short Circuit Current	ISCH	V_{OUT} = 0V, V_{IN} = 6.0V, R_{SET} = 511Ω		6.2		A
Thermal Shutdown Temperature	TSD	V_{OUT} + 0.4V < V_{IN} < 6.0V		175		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	V_{OUT} + 0.4V < V_{IN} < 6.0V		25		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	V_{P-P} = 300mV, f = 1kHz, I_{LOAD} = 3A; V_{IN} = 2.5V, V_{OUT} = 1.8V	**42**	66		dB
Input Supply Ripple Rejection	PSRR	V_{P-P} = 300mV, f = 100kHz, I_{LOAD} = 3A; V_{IN} = 2.5V, V_{OUT} = 1.8V		30		dB
Phase Margin	PM	V_{OUT} = 1.8V, C_L = 220µF Tantalum		70		dB
Gain Margin	GM	V_{OUT} = 1.8V, C_L = 220µF Tantalum		16		dB
Output Noise Voltage		I_{LOAD} = 10mA, BW = 300Hz < f < 300kHz, BYPASS to GND capacitor = 0.2µF		100		μV_{RMS}
DEVICE START-UP CHARACTERISTICS: ENABLE PIN						
Rising Threshold		2.2V < V_{IN} < 6.0V	**0.6**	0.9	**1.2**	V
Falling Threshold		2.2V < V_{IN} < 6.0V	**0.47**	0.7	**0.9**	V
Enable Pin Leakage Current		V_{IN} = 6.0V, EN = 6.0V			**1**	µA
Enable Pin Propagation Delay		V_{IN} = 2.2V, EN rise to I_{OUT} rise	**225**	300	**450**	µs
Enable Pin Turn-on Delay		V_{IN} = 2.2V, V_{OUT} = 1.8V, I_{LOAD} = 1A, C_{OUT} = 220µF, C_{BYP} = 0.2µF		6		ms
Enable Pin Turn-on Delay		V_{IN} = 2.2V, V_{OUT}=1.8V, I_{LOAD} = 1A, C_{OUT} = 47µF, C_{BYP} = 0.2µF		50		µs
Hysteresis		Must be independent of V_{IN}; 2.2V < V_{IN} < 6.0V	**90**	200	**318**	mV
DEVICE START-UP CHARACTERISTICS: PG PIN						
V_{OUT} Error Flag Rising Threshold		2.2V < VIN < 6.0V	**85**	90	**96**	%
V_{OUT} Error Flag Falling Threshold		2.2V < VIN < 6.0V	**82**	88	**93**	%
V_{OUT} Error Flag Hysteresis		2.2V < VIN < 6.0V	**2.5**	3.2	**4.0**	$\%V_{OUT}$

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 220\mu F$ 25mΩ and 0.1µF X7R, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Applications Information" on page 11 of the datasheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Error Flag Low Voltage		I_{SINK} = 1mA		35	**100**	mV
Error Flag Low Voltage		I_{SINK} = 6mA		185	**400**	mV
Error Flag Leakage Current		V_{IN} = 6.0V, PG = 6.0V		0.01	**1**	µA

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Line and Load Regulation done under pulsed condition for T<10ms.
10. Dropout is defined as the difference between the supply V_{IN} and V_{OUT}, when the supply produces a 2% drop in V_{OUT} from its nominal value. Data measured within a 3ms period.

Typical Operating Performance

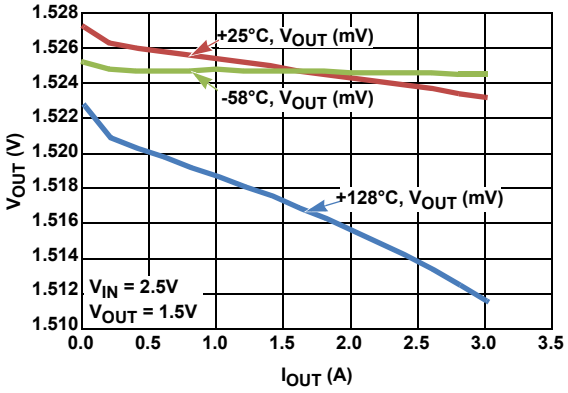


FIGURE 3. LOAD REGULATION, V_{OUT} vs I_{OUT}

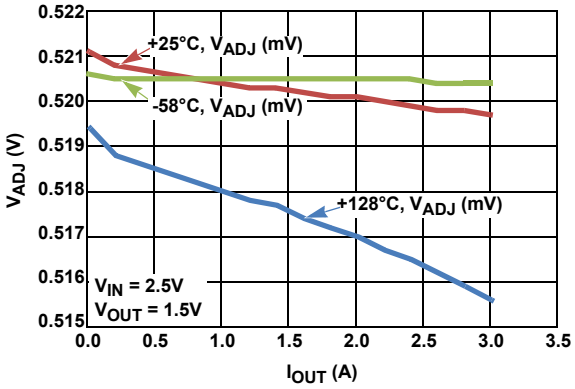


FIGURE 4. LOAD REGULATION, V_{ADJ} vs I_{OUT}

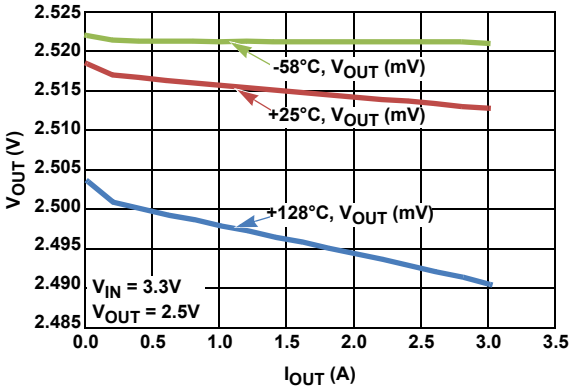


FIGURE 5. LOAD REGULATION, V_{OUT} vs I_{OUT}

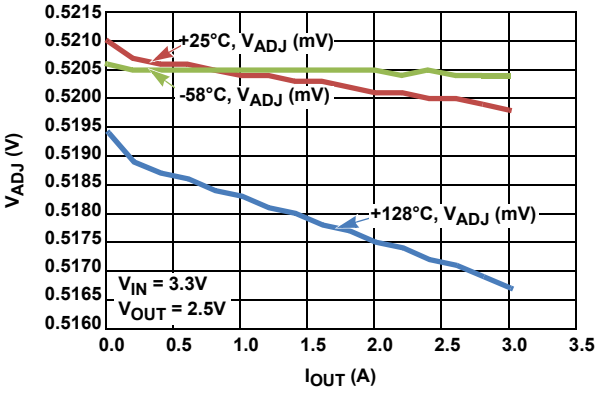


FIGURE 6. LOAD REGULATION, V_{ADJ} vs I_{OUT}

Typical Operating Performance (Continued)

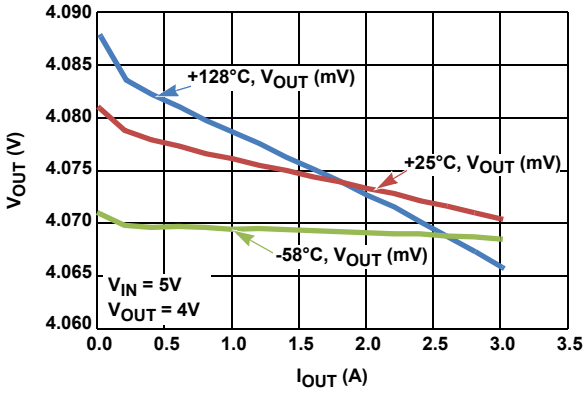


FIGURE 7. LOAD REGULATION, V_{OUT} vs I_{OUT}

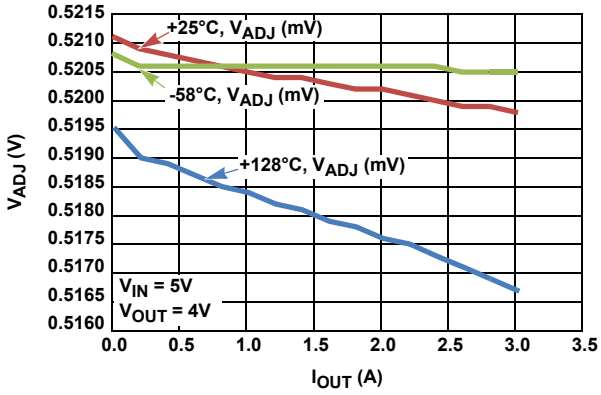


FIGURE 8. LOAD REGULATION, V_{ADJ} vs I_{OUT}

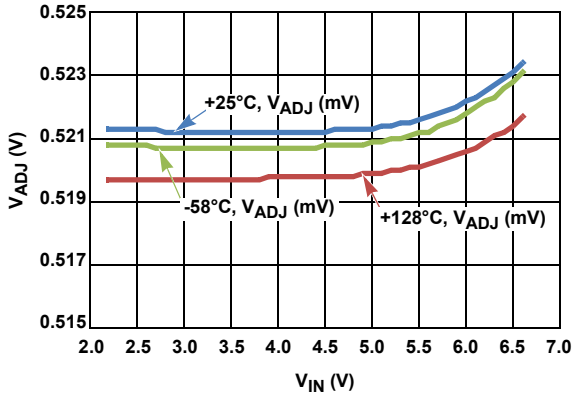


FIGURE 9. V_{IN} vs V_{ADJ} OVER TEMPERATURE

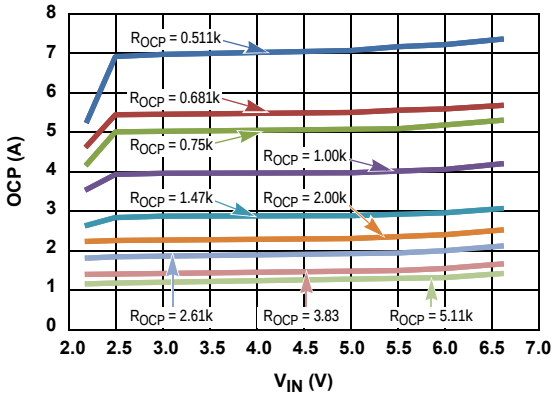


FIGURE 10. R_{OCP} vs OCP AT +25°C, V_{OUT} = 1.5V

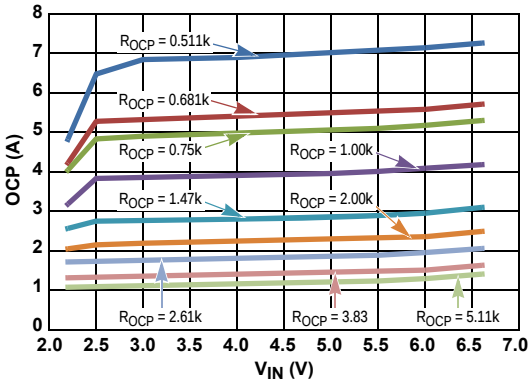


FIGURE 11. R_{OCP} vs OCP AT +128°C, V_{OUT} = 1.5V

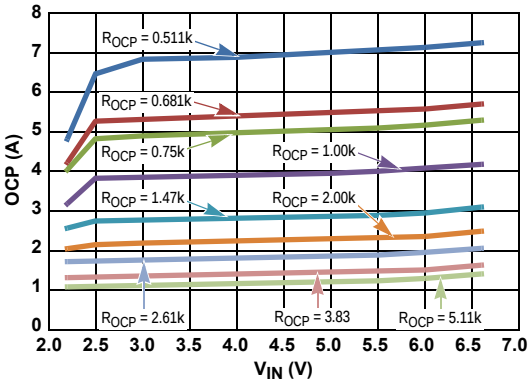


FIGURE 12. R_{OCP} vs OCP AT -58°C, V_{OUT} = 1.5V

Typical Operating Performance (Continued)

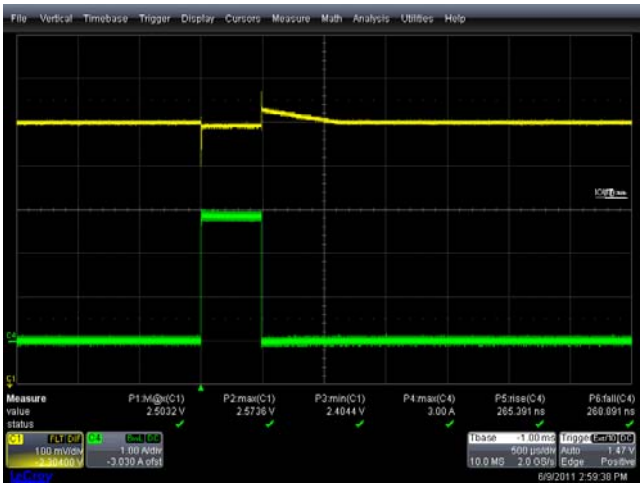


FIGURE 13. TRANSIENT LOAD RESPONSE, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 47µF, 35mΩ

FIGURE 14. TRANSIENT LOAD RESPONSE, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 220µF, 25mΩ

FIGURE 15. POWER-ON AND POWER-OFF, EN = 0 TO 1, +25°C, V_{IN} = 6V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD TURN-ON

FIGURE 16. POWER-ON AND POWER-OFF, EN = 0 TO 1, +25°C, V_{IN} = 2.2V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD TURN-ON

FIGURE 17. POWER-ON AND POWER-OFF, EN = 1 TO 0, +25°C, V_{IN} = 6V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD TURN-OFF

FIGURE 18. POWER-ON AND POWER-OFF, EN = 1 TO 0, +25°C, V_{IN} = 2.2V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD TURN-OFF

Typical Operating Performance (Continued)

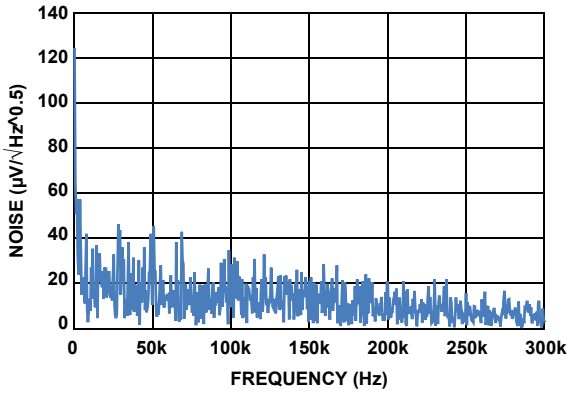


FIGURE 19. NOISE (µV/√Hz 0.5)

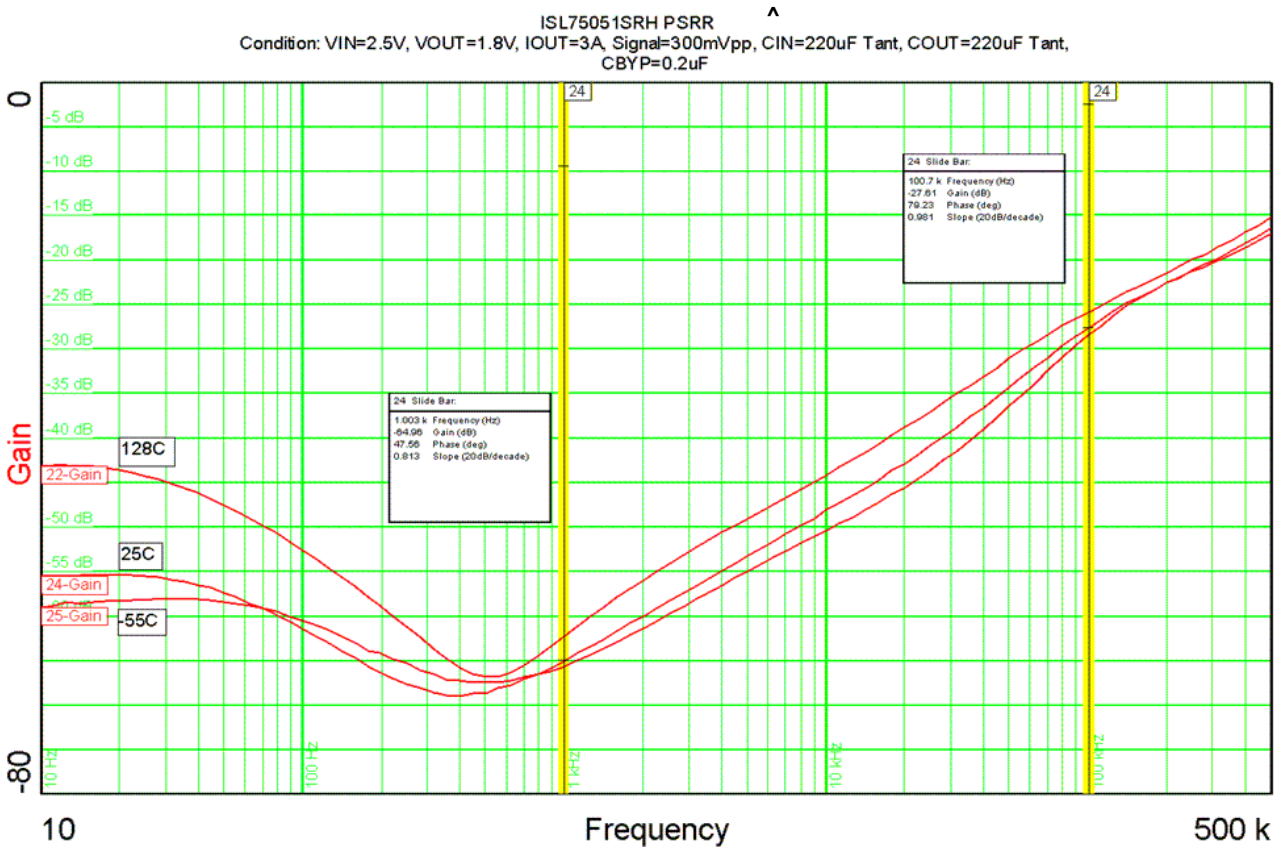


FIGURE 20. PSRR

Applications Information

Input Voltage Requirements

This RH LDO will work from a V_{IN} in the range of 2.2V to 6.0V. The input supply can have a tolerance of as much as ±10% for conditions noted in the “Electrical Specifications” table starting on page 5. Minimum guaranteed input voltage is 2.2V. However, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage, plus dropout at the maximum rated current of the application, if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The dropout spec of this family of LDOs has been generously specified to allow applications to design for efficient operation.

Adjustable Output Voltage

The output voltage of the RH LDO can be set to any user programmable level between 0.8V to 5.0V. This is achieved with a resistor divider connected between the OUT, ADJ and GND pins. With the internal reference at 0.52V, the divider ratio should be fixed such that when the desired VOUT level is reached, the voltage presented to the ADJ pin is 0.52V. Resistor values for typical voltages are shown in Table 1.

TABLE 1. RESISTOR VALUES FOR TYPICAL VOLTAGES

V_{OUT}	R_{TOP}	R_{BOTTOM}
0.8V	7.87k	4.32k
1.5V	2.26k	4.32k
1.8V	1.74k	4.32k
2.5V	1.13k	4.32k
4.0V	634	4.32k
5.0V	499	4.32k

Input and Output Capacitor Selection

RH operation requires the use of a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 220µF, 25mΩ 10V DSSC 04051-032 rated tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 CDR04 ceramic capacitor, to be connected between V_{IN} to GND pins and V_{OUT} to GND pins of the LDO, with PCB traces no longer than 0.5cm.

The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6mΩ to 100mΩ. At the lower limit of ESR = 6mΩ, the phase margin is about 51°C. On the high side, an ESR of 100mΩ is found to limit the gain margin at around 10dB. The typical GM/PM seen with capacitors are shown in Table 2.

TABLE 2. TYPICAL GM/PM WITH VARIOUS CAPACITORS

CAPACITANCE (µF)	ESR (mΩ)	GAIN MARGIN (dB)	PHASE MARGIN (°)
47	35	14	55
100	25	16	57
220	6	19	51
220	25	16	69
100	100	10	62

Type numbers of KEMET capacitors used in the device are shown in Table 3.

TABLE 3. KEMET CAPACITORS USED IN DEVICE

KEMET TYPE NUMBER	CAPACITOR DETAILS
T525D476M016ATE035	47µF, 10V, 35mΩ
T525D107M010ATE025	100µF, 10V, 25mΩ
T530D227M010ATE006	220µF, 10V, 6mΩ
T525D227M010ATE025	220µF, 10V, 25mΩ
T495X107K016ATE100	100µF, 16V, 100mΩ

A typical gain phase plot measured on the ISL75051SRHEVAL1Z evaluation board for V_{IN} = 3.3V, V_{OUT} = 1.8V and I_{OUT} = 3A with a 220µF, 10V, 25mΩ capacitor is shown in Figure 21 and is measured at GM = 16.3dB and PM = 69.16°.

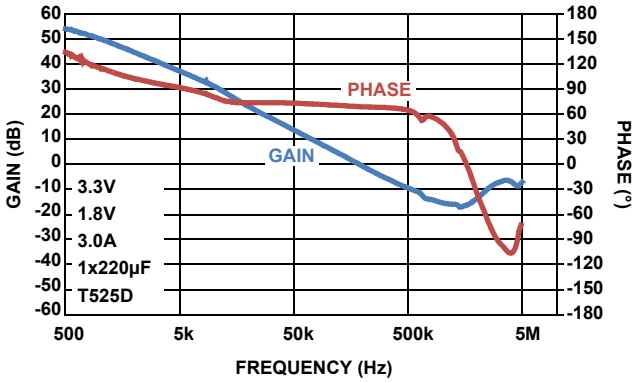


FIGURE 21. TYPICAL GAIN PHASE PLOT

Enable

The device can be enabled by applying a logic high on the EN pin. The enable threshold is typically 0.9V. A soft-start cycle is initiated when the device is enabled using this pin. Taking this pin to logic low disables the device.

EN can be driven from either an open drain or a totem pole logic drive between EN pin and GND. Assuming an open drain configuration, M1 will actively pull down the EN line, as shown in Figure 22, and thereby discharge the input capacitance, shutting off the device immediately.

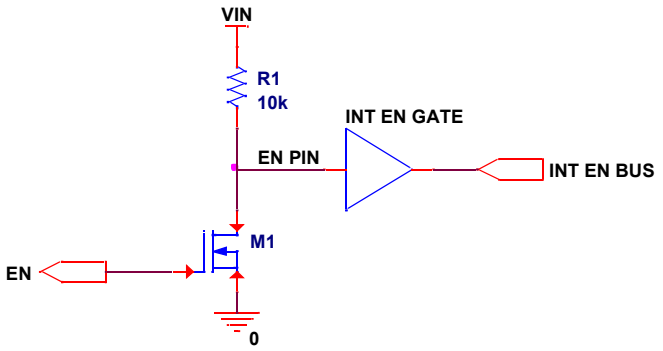


FIGURE 22. ENABLE

Power Good

The Power-Good pin is asserted high when the voltage on the ADJ pin crosses the rising threshold of 0.9 x V_{ADJ} typ. On the falling threshold, Power-Good is asserted low when the voltage on the ADJ pin crosses the falling threshold of 0.88 x V_{ADJ}. The power-good output is an open-drain output rated for a continuous sink current of 1mA.

Soft-start

Soft-start is achieved by means of the charging time constant of the BYP pin. The capacitor value on the pin determines the time constant and can be calculated using Equation 1:

$$T_S = 0.00577 x C_S \quad \text{(EQ. 1)}$$

where T_S = soft-start time in ms, and C_S = BYPASS capacitor in nF.

The BYPASS capacitor, C1, charges with a 90µA source current and provides an EA reference, -IN, with an SS ramp. V_{OUT}, in turn, follows this ramp. The ramp rate can be calculated based on the C1 value. For conditions in which C1 is opened, or for small values of C1, the ramp is provided by C2 = 50pF, with a source of 0.5µA. Connecting C1 min = 0.1µF to the BYPASS pin is recommended for normal operation.

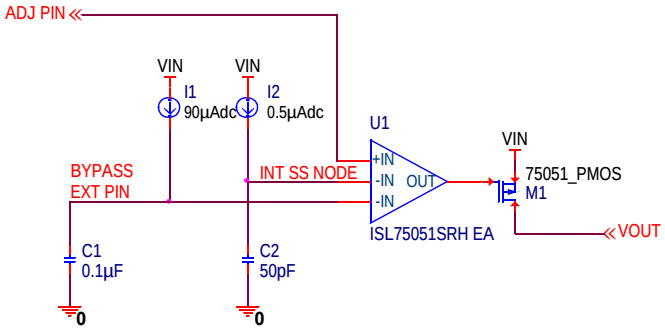


FIGURE 23. SOFT-START

Current Limit Protection

The RH LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit becomes a constant current source when the output current exceeds the current limit threshold, which can be adjusted by means of a resistor connected between the OCP pin and GND. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. OCP can be calculated with Equation 2:

$$OCP = 9.5 \bullet EXP(-0.6 \bullet (ROCP/(1 + 0.1ROCP))) \quad \text{(EQ. 2)}$$

where OCP = Overcurrent Threshold in amps, and ROCP = OCP resistor in kΩ.

In the event of an overload condition based on the set OCP limit, the die temperature may exceed the internal over-temperature limit, and the LDO begins to cycle on and off due to the fault condition (Figure 24). However, thermal cycling may never occur if the heatsink used for the package can keep the die temperature below the limits specified for thermal shutdown.

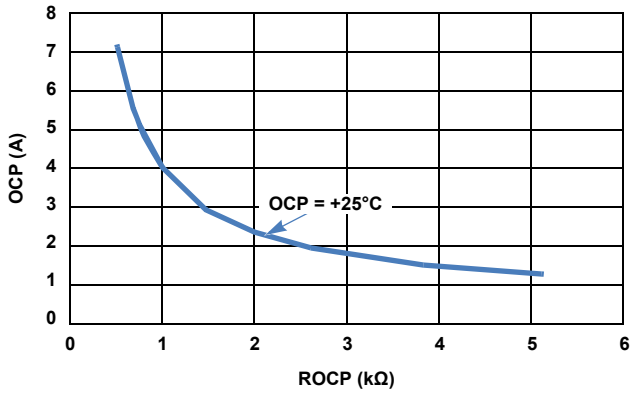


FIGURE 24. OCP vs ROCP OVER TEMP

Thermal Guidelines

If the die temperature exceeds typically +175°C, then the LDO output shuts down to zero until the die temperature cools to typically +155°C. The level of power combined with the thermal impedance of the package (θ_{JC} of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table.

The device should be mounted on a high effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between package base and PCB copper plane. The VIN and VOUT ratios should be selected to ensure that dissipation for the selected VIN range keeps T_J within the recommended operating level of 150°C for normal operation.

Weight Characteristics

Weight of Packaged Device

K18.D: 1.07 Grams typical with leads clipped

Die Characteristics

Die Dimensions

4555µm x 4555µm (179.3 mils x 179.3 mils)
Thickness: 304.8µm ± 25.4µm (12.0 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ± 0.03µm to 1.2µm ± 0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7µm ±0.4µm

BACKSIDE METALLIZATION

None

SUBSTRATE

Type: Silicon

BACKSIDE FINISH

Silicon

PROCESS

0.6µM BiCMOS Junction Isolated

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased

ADDITIONAL INFORMATION

Worst Case Current Density

$< 2 \times 10^5$ A/cm^2

Transistor Count

2932

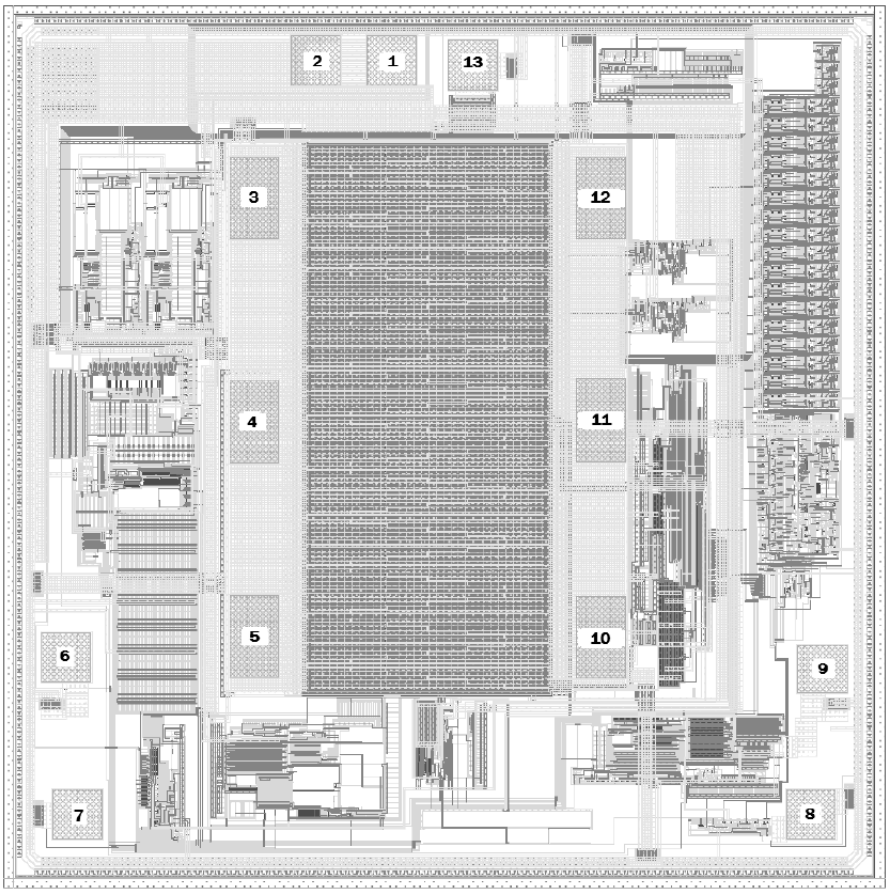
Layout Characteristics

Step and Repeat

4555µm x 4555µm

Metallization Mask Layout

PAD X Y COORDINATES			
PAD	NAME	X µm	Y µm
1	GND	0	0
2	GND	-393	0
3	VOUT	-711	-710
4	VOUT	-711	-1858
5	VOUT	-711	-2964
6	ADJ	-1680	-3070
7	BYP	-1621	-3879
8	EN	2164	-3879
9	OCP	2222	-3131
10	VIN	1078	-2965
11	VIN	1078	-1853
12	VIN	1078	-711
13	PG	420	-25



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 4, 2011	FN7610.1	Removed “Coming Soon” from ISL75051SRHVF, ISL75051SRHQF, ISL75051SRHVX and ISL75051SRHX/SAMPLE in “Ordering Information” table on page 4.
September 30, 2011	FN7610.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL75051SRH

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

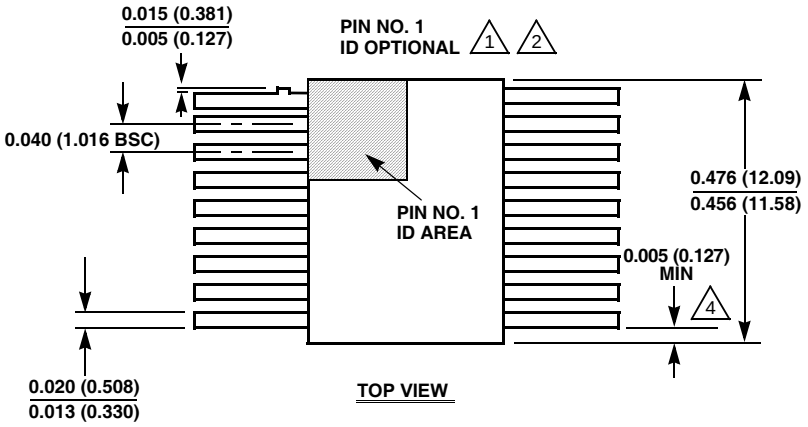
FITs are available from our website at: http://rel.intersil.com/reports/search.php

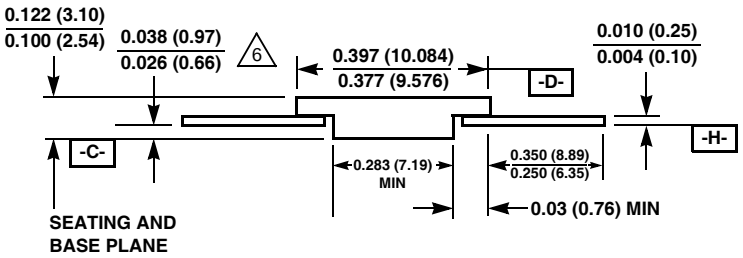
Package Outline Drawing

K18.D

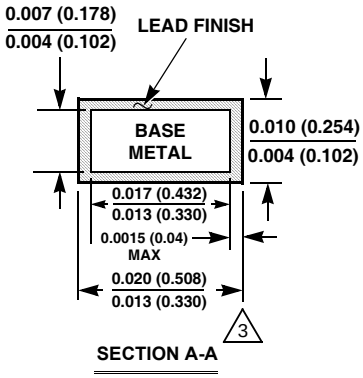
18 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 2, 3/11





SIDE VIEW



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions = INCH (mm). Controlling dimension: INCH.