



# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Description

The ACE24C02/04/08/16B provides 2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The ACE24C02/04/08/16B is available in space-saving 8-lead PDIP, 8-lead SOP, 8-lead MSOP, 8-lead TSSOP, 8-pad DFN, and SOT23-5 packages and is accessed via a two-wire serial interface.

## Features

- Wide Voltage Operation  $V_{CC}=1.8V$  to  $5.5V$
- Operating Ambient Temperature  $-40^{\circ}C$  ~  $85^{\circ}C$
- Internally Organized: ACE24C02B 256\*8 (2K bits) / ACE24C04B 512\*8 (4K bits) / ACE24C08B 1024\*8 (8K bits) / ACE24C16B 2048\*8 (16K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHz(5V), 400kHz(1.8V,2.5V,2.7V)Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-byte Page (2K), 16-byte Page (4K,8K,16K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5ms max)
- High-reliability - Endurance: 1,000,000 Write Cycles  
- Data Retention: 100 Years

## Absolute Maximum Ratings

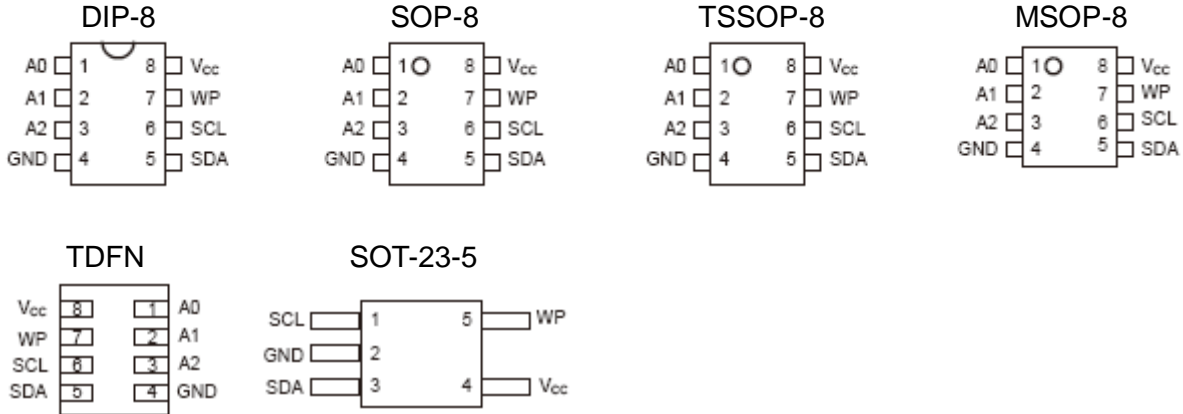
DC Supply Voltage	-0.3 to 6.5V
Input / Output Voltage	GND-0.3V to $V_{CC}+0.3V$
Operating Ambient Temperature	$-40^{\circ}C$ to $85^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $150^{\circ}C$

\*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging Type



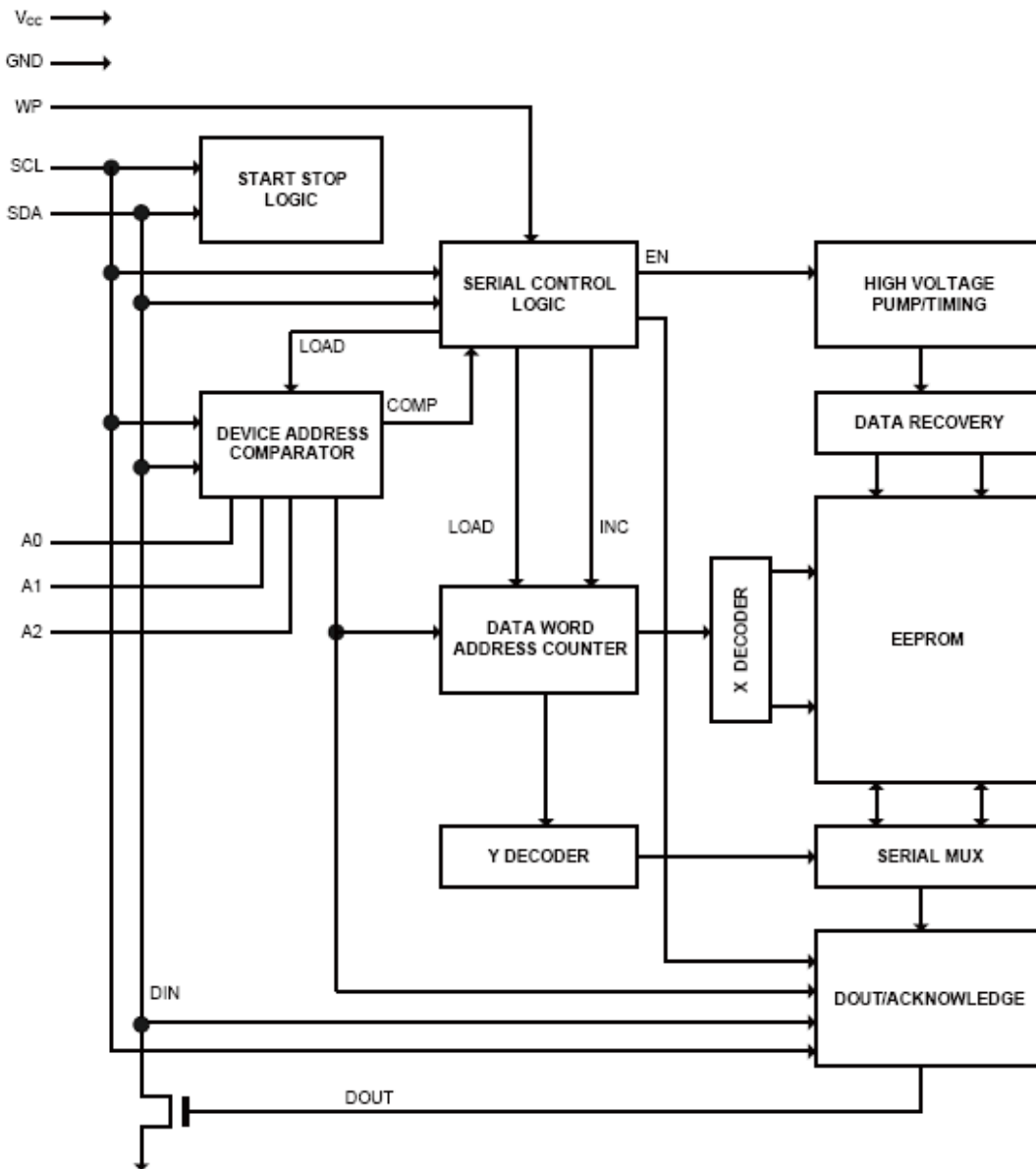
## Pin Configurations

Pin Name	Functions
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V <sub>CC</sub>	Power Supply



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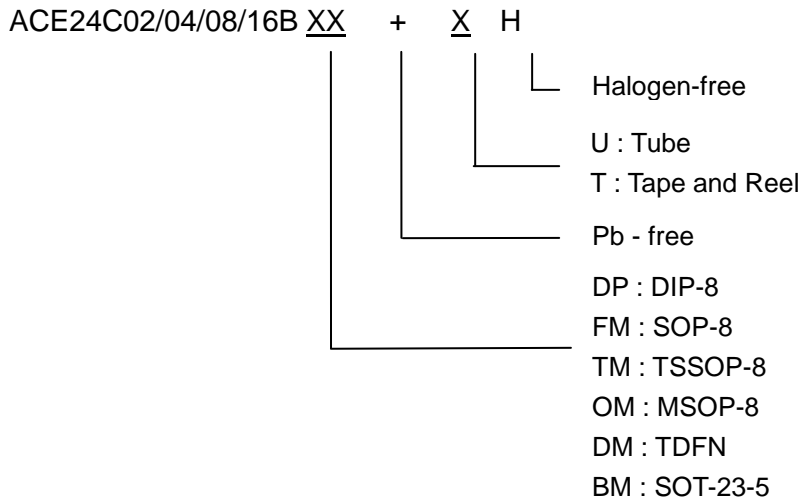
## Block Diagram





# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Ordering information



### Device/Page Addresses (A2, A1 and A0):

The A2, A1 and A0 pins are device address inputs that are hard wired for the ACE24C02B. Eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The ACE24C04B uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect and can be connected to ground.

The ACE24C08B only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects and can be connected to ground.

The ACE24C16B does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1, and A2 pins are no connects and can be connected to ground.

### Serial Data (SDA):

The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

### Serial Clock (SCL):

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

### Write Protect (WP):

The ACE24C02B/ACE24C04B/ACE24C08B/ACE24C16B has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, the write protection feature is enabled and operates as shown in the following.



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## Write Protect Description

WP Pin Status	Part of the Array Protected			
	ACE24C02B	ACE24C04B	ACE24C08B	ACE24C16B
At V <sub>CC</sub>	Full (2K) Array	Full (4K) Array	Full (8K) Array	Upper Half (16K) Array
At GND	Normal Read / Write Operations			

## Memory Organization

ACE24C02B, 2K SERIAL EEPROM:

Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

ACE24C04B, 4K SERIAL EEPROM:

Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

ACE24C08B, 8K SERIAL EEPROM:

Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

ACE24C16B, 16K SERIAL EEPROM:

Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

## Pin Capacitance

Applicable over recommended operating range from: T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
C <sub>I/O</sub>	Input / Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub>	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

## DC Characteristics

Applicable over recommended operating range from: T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +1.8V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V <sub>CC</sub>	Supply Voltage		1.8		5.5	V
I <sub>CC1</sub>	Supply Current	V <sub>CC</sub> = 5.0V, Read at 100kHz		0.4	1.0	mA
I <sub>CC2</sub>	Supply Current	V <sub>CC</sub> = 5.0V, Write at 100 kHz		2.0	3.0	mA
I <sub>SB</sub>	Standby Current	V <sub>IN</sub> = V <sub>CC</sub> /GND			1.0	μA
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> /GND			3.0	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>CC</sub> /GND		0.05	3.0	μA
V <sub>IL</sub>	Input Low Level		-0.3		V <sub>CC</sub> × 0.3	V
V <sub>IH</sub>	Input High Level		V <sub>CC</sub> × 0.7		V <sub>CC</sub> + 0.3	V
V <sub>OL3</sub>	Output Low Level	V <sub>CC</sub> = 5.0V, I <sub>OL</sub> = 3.0 mA			0.4	V



# ACE24C02/04/08/16B Two-wire Serial EEPROM

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V <sub>OL2</sub>	Output Low Level	V <sub>CC</sub> = 3.0V, I <sub>OL</sub> = 2.1 mA			0.4	V
V <sub>OL1</sub>	Output Low Level	V <sub>CC</sub> = 1.8V, I <sub>OL</sub> = 0.15 mA			0.2	V

## AC Characteristics

Applicable over recommended operating range from: T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	1.8-volt			3.6-volt			Units
		Min	Typ	Max	Min	Typ	Max	
f <sub>SCL</sub>	Clock Frequency, SCL			400			1000	kHz
T <sub>LOW</sub>	Clock Pulse Width Low	1.2			0.6			μs
T <sub>HIGH</sub>	Clock Pulse Width High	0.6			0.4			μs
T <sub>AA</sub>	Clock Low to Data Out Valid	0.05		0.9	0.05		0.55	μs
T <sub>BUF</sub> <sup>1</sup>	Time the bus must be free before a new transmission can Start	1.2			0.5			μs
T <sub>HD.STA</sub>	Start Hold Time	0.6			0.25			μs
T <sub>SU.STA</sub>	Start Setup Time	0.6			0.25			μs
T <sub>HD.DAT</sub>	Data In Hold Time	0			0			μs
T <sub>SU.DAT</sub>	Data In Setup Time	100			100			ns
T <sub>R</sub>	Inputs Rise Time			0.3			0.3	μs
T <sub>F</sub>	Inputs Fall Time			300			100	ns
T <sub>SU.STO</sub>	Stop Setup Time	0.6			0.25			μs
T <sub>DH</sub>	Data Out Hold Time	50			50			ns
T <sub>WR1</sub>	Write Cycle Time (for 04B/16B)		3.3	5		3.3	5	ms
T <sub>WR1</sub>	Write Cycle Time (for 02B/08B)		1.5	5		1.5	5	ms
Endurance	5.0V, 25°C, Page Mode	1,000,000						Write Cycles

Notes:1. This parameter is characterized and not 100% tested.

2.AC measurement conditions:

RL (connects to Vcc): 1.3kΩ(2.5V,5V),10kΩ(1.8V)

Input pulse voltages: 0.3 Vcc to 0.7 Vcc

Input rise and fall times: ≤ 50 ns

Input and output timing reference voltages: 0.5Vcc

The value of RL should be concerned according to the actual loading on the user's system.



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## Device Operation

### Clock and Data Transitions:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

### Start Condition:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

### Stop Condition:

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see to Figure 2).

### Acknowledge:

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. The happens during the ninth clock cycle.

### Standby Mode :

The ACE24C02/04/08/16B features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

### Memory Reset :

After an interruption in protocol power loss or system reset, any two-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high and then.
3. Create a start condition.

## Bus Timing

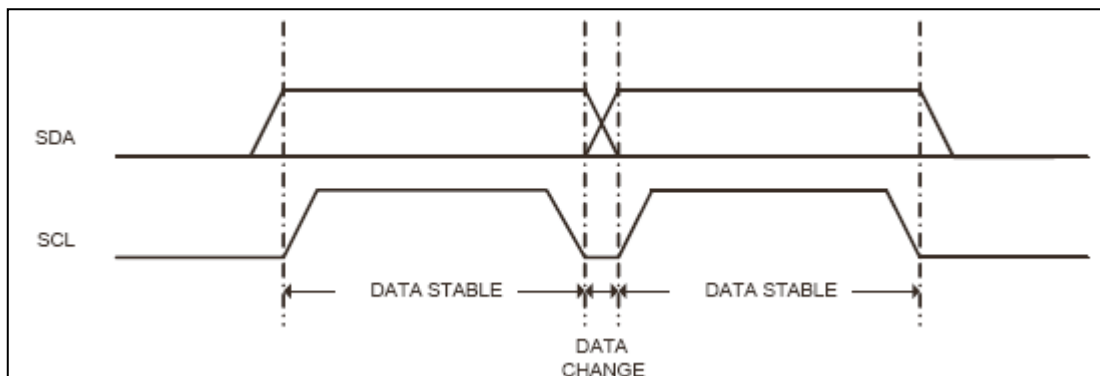


Figure 1 · Data Validity







## ACE24C02/04/08/16B Two-wire Serial EEPROM

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

### Write Operations

#### Byte Write:

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see to Figure 5).

#### Page Write:

The 2K EEPROM is capable of an 8-byte page write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see to Figure 6).

The data word address lower three (2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

#### Acknowledge Polling:

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

### Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.



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### Current Address Read:

The internal data word address counter maintains accessed address, the last and incremented by one. But for ACE24C16B, only lower 8 bits of the internal data word address counter maintains the last accessed address, the higher 3 bits (P2, P1, P0) will follow the device address input at each current address read. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "one" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

### Random Read:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8).

### Sequential Read:

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 9).

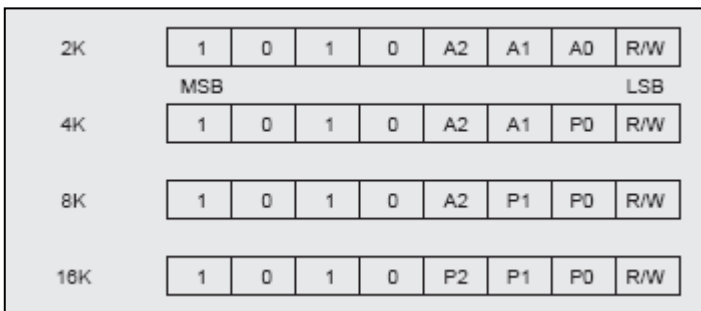


Figure 4 · Device Address



# ACE24C02/04/08/16B Two-wire Serial EEPROM

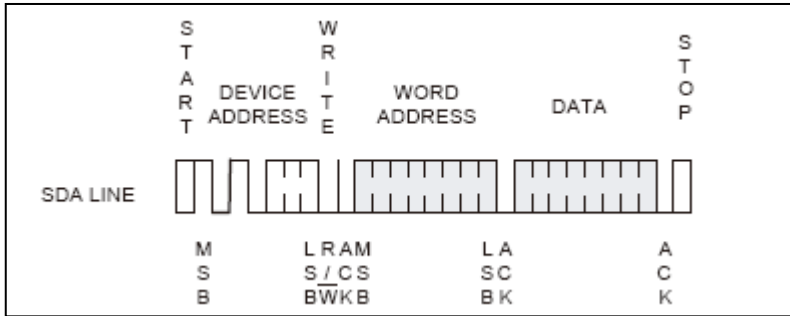


Figure 5 · Byte Write

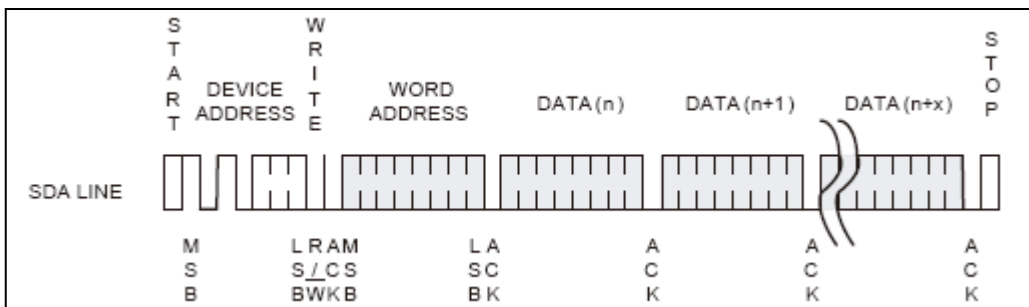


Figure 6 · Page Write

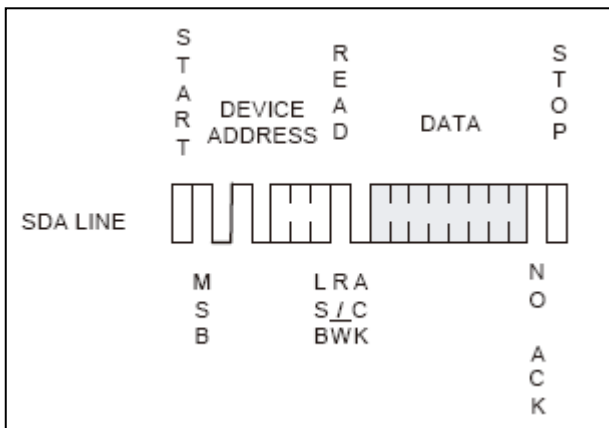


Figure 7 · Current Address Read





# ACE24C02/04/08/16B Two-wire Serial EEPROM

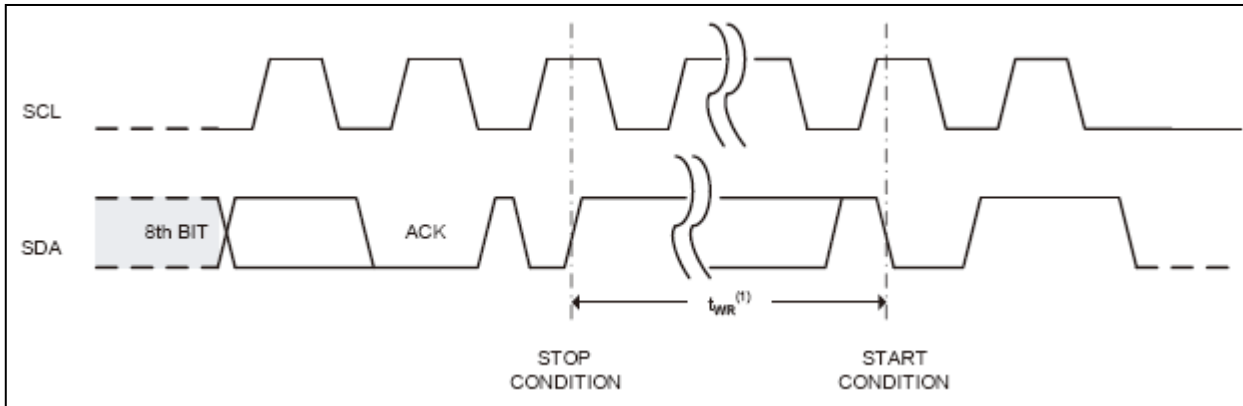


Figure 11 · SCL: Serial Clock, SDA: Serial Data I/O

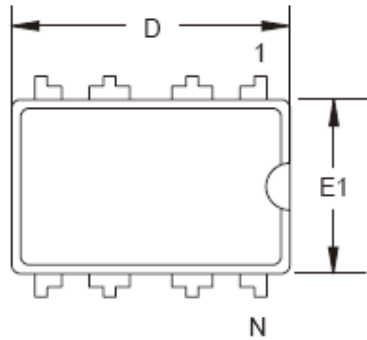
Note: The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.



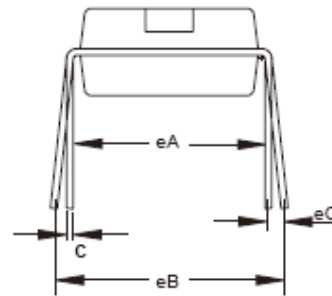
# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging information

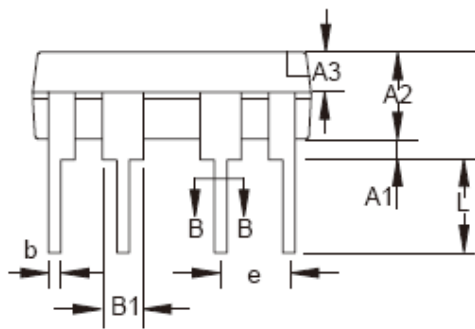
### DIP-8



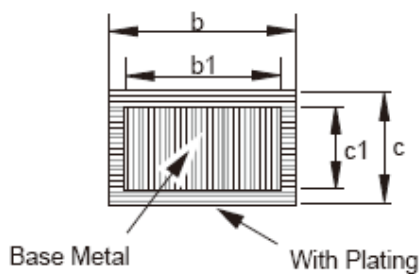
Top View



End View



Side View



Section B-B

### COMMON DIMENSIONS (Unit of Measure = mm)

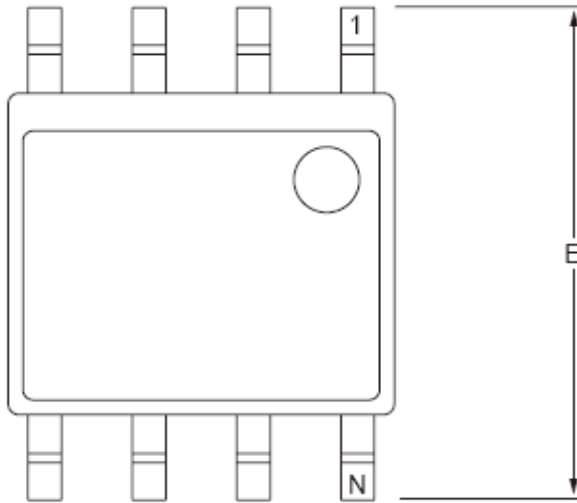
SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.28
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-



# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging information

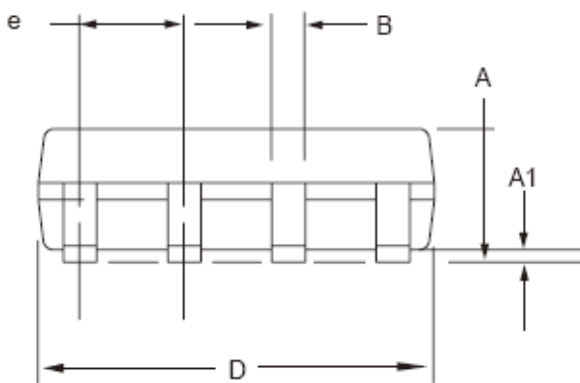
### SOP-8



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

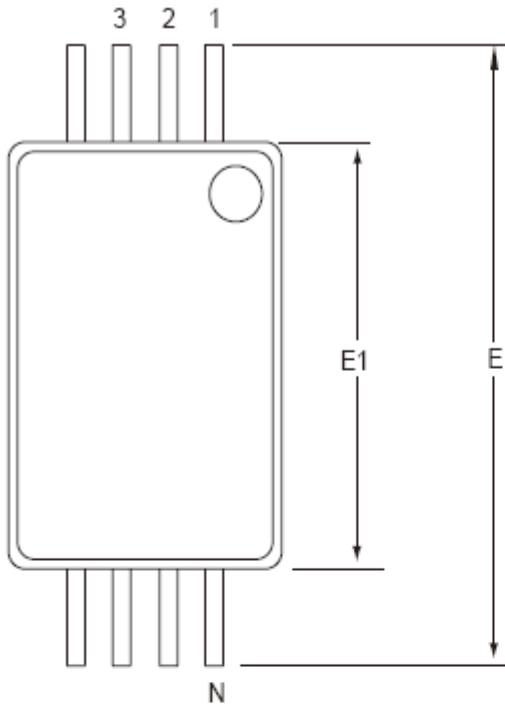
SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
$\theta$	0°	8°



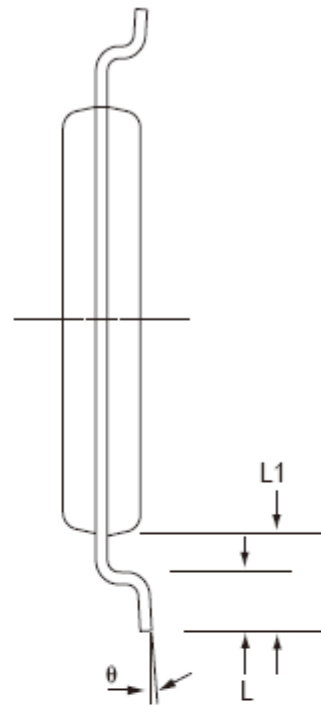
# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging information

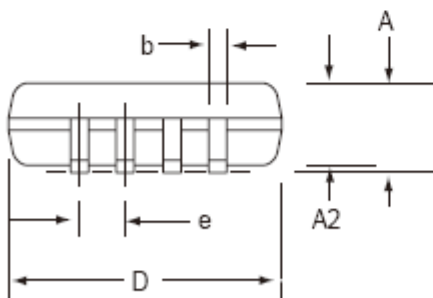
### TSSOP-8



Top View



End View



Side View

#### COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	MAX
D	2.80	3.20
E	6.20	6.60
E1	4.20	4.60
A	-	1.20
A2	0.80	1.15
b	0.19	0.30
e	0.85 BSC	
L	0.45	0.75
L1	1.00 BSC	
$\theta$	0°	8°

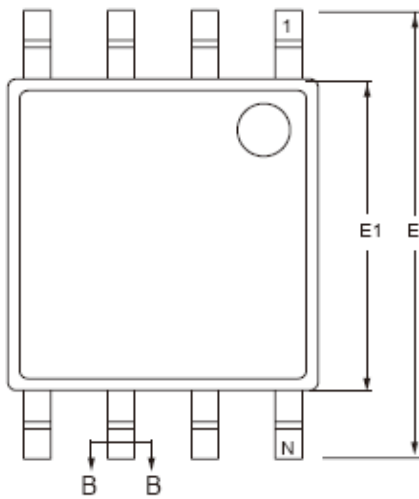




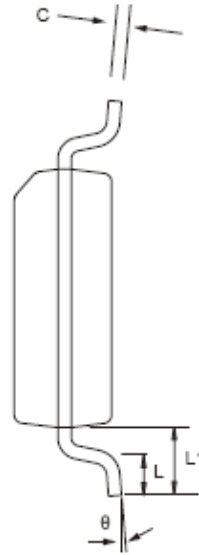
# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging information

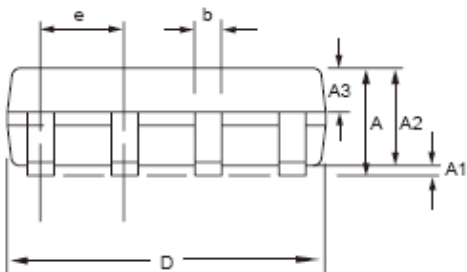
### MSOP-8



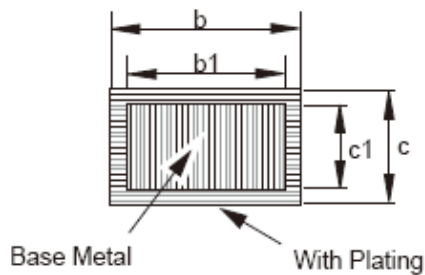
Top View



End View



Side View



Section B-B

COMMON DIMENSIONS  
(Unit of Measure = mm)

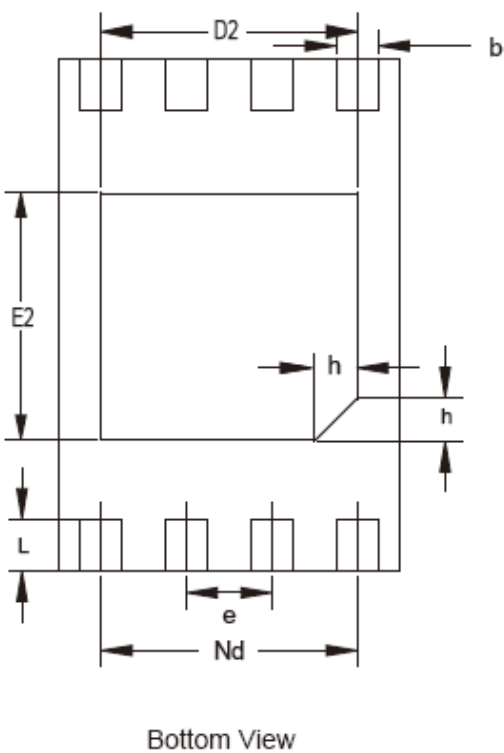
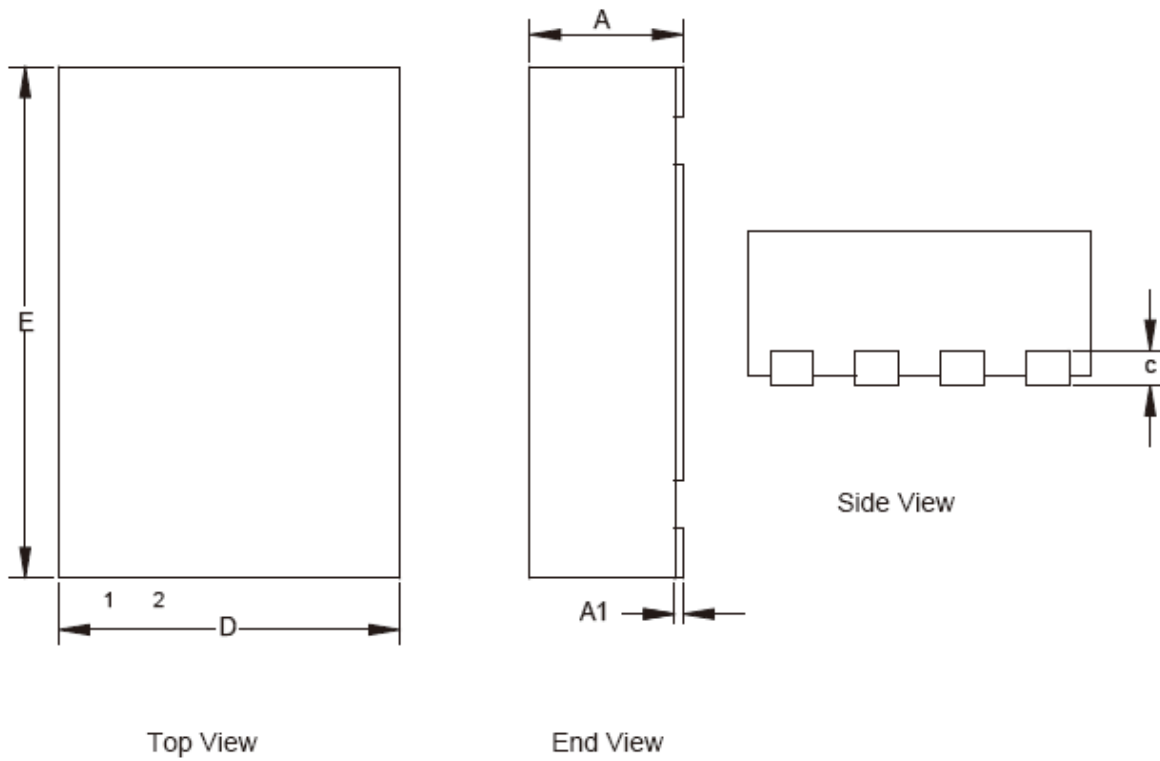
SYMBOL	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65 BSC	
L	0.40	0.70
L1	0.95 BSC	
$\theta$	0°	8°



# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging information

### TDFN



COMMON DIMENSIONS  
(Unit of Measure = mm)

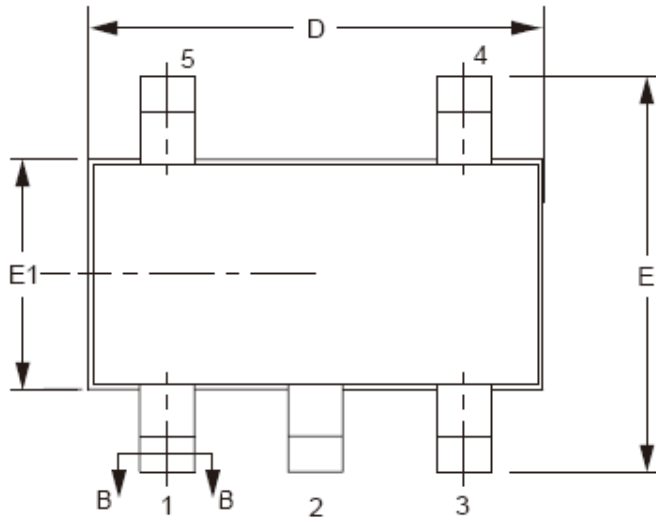
SYMBOL	MIN	MAX
A	0.70	0.80
A1	-	0.05
b	0.18	0.30
c	0.18	0.25
D	1.90	2.10
D2	1.50 REF	
e	0.50 BSC	
Nd	1.50 BSC	
E	2.90	3.10
E2	1.60 BSC	
L	0.30	0.50
h	0.20	0.30



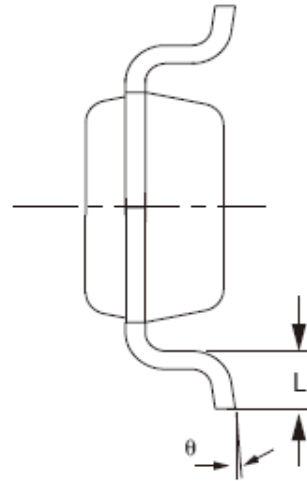
# ACE24C02/04/08/16B Two-wire Serial EEPROM

## Packaging information

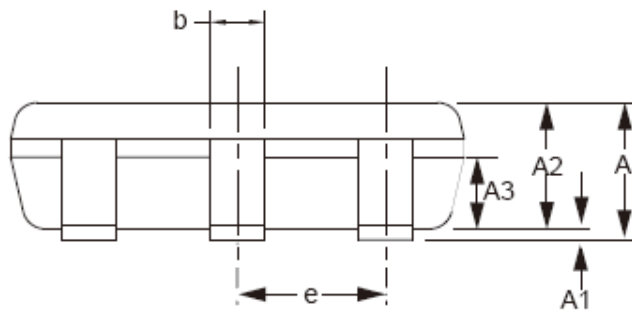
### SOT-23-5



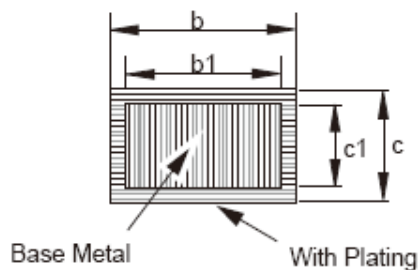
Top View



End View



Side View



Section B-B

#### COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	MAX
A	1.05	1.30
A1	0	0.10
A2	1.00	1.20
A3	0.55	0.75
b	0.30	0.50
b1	0.33	0.38
c	0.10	0.21
c1	0.14	0.16
D	2.72	3.12
E	2.80	3.00
E1	1.40	1.80
e	0.95 BSC	
L	0.30	0.60
$\theta$	0°	8°



## **ACE24C02/04/08/16B Two-wire Serial EEPROM**

### Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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