





EH26 45

Series — RoHS Compliant (Pb-free) 3.3V 4 Pad 5mm x 7mm Ceramic SMD LVCMOS High Frequency Oscillator

Frequency Tolerance/Stability ±50ppm Maximum

Operating Temperature Range – 0°C to +70°C

TS -18.432M

Nominal Frequency 18.432MHz

Pin 1 Connection
Tri-State (High Impedance)

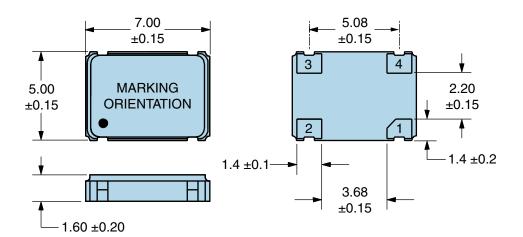
Duty Cycle 50 ±10(%)

Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Agir Shock, and Vibration) Aging at 25°C	ELECTRICAL SPECIFICATIONS		
Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Agir Shock, and Vibration) Aging at 25°C	Nominal Frequency	18.432MHz	
Operating Temperature Range 0°C to +70°C Supply Voltage 3.3Vdc ±0.3Vdc Input Current 35mA Maximum (No Load) Output Voltage Logic High (Voh) 2.7Vdc Minimum (IOH= -8mA) Output Voltage Logic Low (Vol) 0.5Vdc Maximum (IOH= +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum		±50ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)	
Supply Voltage Input Current 35mA Maximum (No Load) Output Voltage Logic High (Voh) 2.7Vdc Minimum (IOH= -8mA) Output Voltage Logic Low (Vol) 0.5Vdc Maximum (IOH= +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter 10mSec Maximum	Aging at 25°C	±5ppm/year Maximum	
Input Current 35mA Maximum (No Load) Output Voltage Logic High (Voh) 2.7Vdc Minimum (IOH= -8mA) Output Voltage Logic Low (Vol) 0.5Vdc Maximum (IOH= +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Operating Temperature Range	0°C to +70°C	
Output Voltage Logic High (Voh) 2.7Vdc Minimum (IOH= -8mA) Output Voltage Logic Low (Vol) 0.5Vdc Maximum (IOH= +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Supply Voltage	3.3Vdc ±0.3Vdc	
Output Voltage Logic Low (Vol) 0.5Vdc Maximum (IOH= +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Input Current	35mA Maximum (No Load)	
Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Output Voltage Logic High (Voh)	2.7Vdc Minimum (IOH= -8mA)	
Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Output Voltage Logic Low (Vol)	0.5Vdc Maximum (IOH= +8mA)	
Load Drive Capability Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)	
Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Duty Cycle	50 ±10(%) (Measured at 50% of waveform)	
Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Load Drive Capability	30pF Maximum	
Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Output Logic Type	CMOS	
output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum	Pin 1 Connection	Tri-State (High Impedance)	
One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical Start Up Time 10mSec Maximum		70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.	
Start Up Time 10mSec Maximum	Absolute Clock Jitter	±250pSec Maximum, ±100pSec Typical	
·	One Sigma Clock Period Jitter	±50pSec Maximum, ±40pSec Typical	
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum	
otoriago romporataro rango	Storage Temperature Range	-55°C to +125°C	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V	
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	
Flammability	UL94-V0	
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	
Mechanical Shock	MIL-STD-883, Method 2002, Condition B	
Moisture Resistance	MIL-STD-883, Method 1004	
Moisture Sensitivity	J-STD-020, MSL 1	
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, Method 1010, Condition B	
Vibration	MIL-STD-883, Method 2007, Condition A	



MECHANICAL DIMENSIONS (all dimensions in millimeters)



PIN	CONNECTION
1	Tri-State (High Impedance)
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	18.432M
3	XXXXXX XXXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters



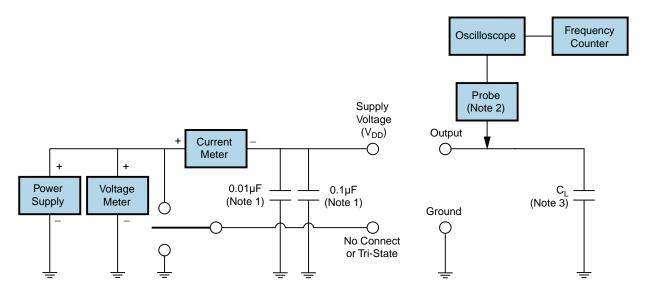
All Tolerances are ±0.1



OUTPUT WAVEFORM & TIMING DIAGRAM



Test Circuit for CMOS Output



- Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value \dot{C}_L includes sum of all probe and fixture capacitance.



Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T _s MAX to T _L (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _s MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T _L to T _P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T _L)	217°C
- Time (t _L)	60 - 150 Seconds
Peak Temperature (T _P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T _P Target)	250°C +0/-5°C
Time within 5°C of actual peak (t _p)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.



Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T _S MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	N/A
- Temperature Typical (T _S TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	60 - 120 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	240°C Maximum
Target Peak Temperature (T _P Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)