

FEATURES

- 12 dB Gain
- +5 V Nominal Supply Voltage
- High Linearity
- Low Noise Figure: 2.7 dB (typ)
- Characterized at +25 dBmV output power
- Wide Band operation to beyond 1 GHz
- -40 to +85 °C
- RoHS-Compliant Package Option

APPLICATIONS

- Driver Amplifier
- CATV - Distribution / Drop Amplifiers
- Set Top Boxes
- Home Gateway

PRODUCT DESCRIPTION

The ABA3100 is a monolithic IC intended for use in applications requiring high linearity, such as Cellular Telephone Base Station Driver Amplifiers, CATV Fiber Receiver and Distribution Amplifiers, CATV Drop Amplifiers, CATV Set Top Boxes and Home Gateways.



Offered in a modified 16 lead surface mount SOIC package, it is well suited for use in amplifiers where small size, reduced component count, and high reliability are important.

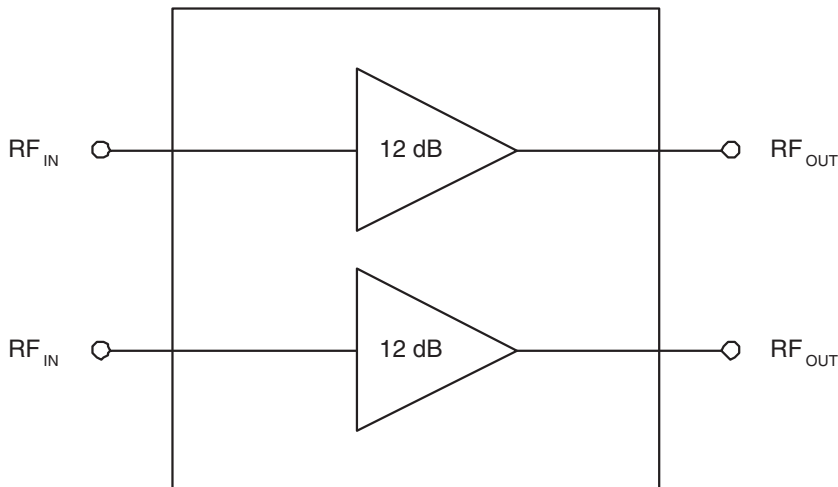


Figure 1: Block Diagram

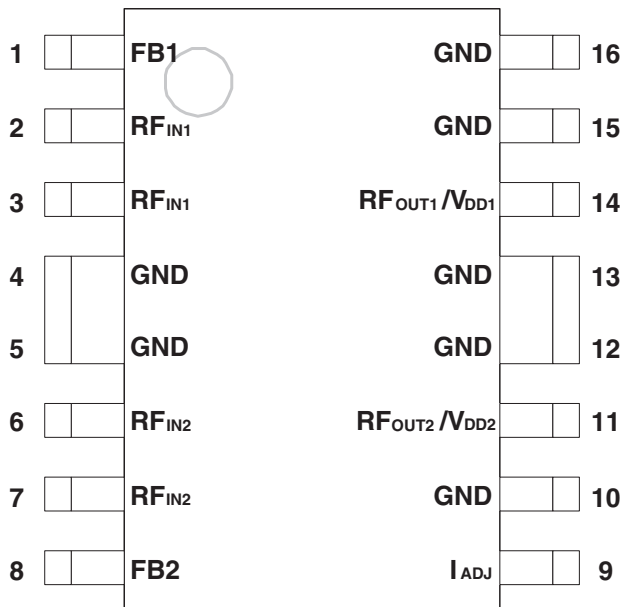


Figure 2: Pinout Diagram

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	FB1	Feedback for Amplifier A1	9	I _{ADJ}	Current Adjust
2	RF _{IN1}	RF Input of Amplifier A1	10	GND	Ground
3	RF _{IN1}	RF Input of Amplifier A1	11	RF _{OUT2} V _{DD2}	RF output and V _{DD} of Amplifier A2
4	GND	Ground	12	GND	Ground
5	GND	Ground	13	GND	Ground
6	RF _{IN2}	RF Input of Amplifier A2	14	RF _{OUT1} /V _{DD1}	RF Output and V _{DD} of Amplifier A1
7	RF _{IN2}	RF Input of Amplifier A2	15	GND	Ground
8	FB2	Feedback for Amplifier A2	16	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Analog Supply (pins 11, 14)	0	+12	V _{DC}
RF Power at Inputs (pins 2, 3, 6, 7)	-	+10	dBm
Storage Temperature	- 65	+150	°C
Soldering Temperature	-	260	°C
Soldering Time	-	5.0	Sec.

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 1, 2, 3, 6, 7 and 8 should be AC-coupled. No external DC bias should be applied.
2. Pin 9 should be AC-grounded. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNITS
RF Input / Output Frequency	50	-	1000	MHz
Analog Supply: V _{DD} (pins 11, 14)	+4.5	+5	+9	V _{DC}
Case Temperature: T _A	-40	-	+85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications
(T_A = +25 °C, V_{DD} = + 5 VDC, Test System = 75Ω)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
Gain	11	12	13	dB	
Noise Figure	-	2.5	3.0	dB	50 MHz - 350 MHz
	-	2.7	3.5	dB	350 MHz - 550 MHz
	-	3.2	4.0	dB	550 MHz - 860 MHz
Input/Output Return Loss	10	18	-	dB	
CSO ⁽¹⁾		-72		dBc	
CTB ⁽¹⁾		-75		dBc	
2nd Order Input Intercept Point (OIP2) ⁽²⁾		+60		dBm	
3rd Order Input Intercept Point (OIP3) ⁽²⁾		+35		dBm	
Thermal Resistance	-	-	33	°C/W	
Current Consumption ^(3,4)	120	150	170	mA	

Notes:

(1) 132 channels, +25 dBmV per channel (measured at the output), 6 MHz channel spacing.

(2) Two tones: 397 MHz and 403 MHz, +4 dBm per tone.

(3) Characterized with I_{ADJ} pin floating.

(4) Adding a shunt resistor from the I_{ADJ} pin to ground will lower current, but with some decrease in performance.

PERFORMANCE DATA

Figure 3: Typical Gain (S21) vs. Frequency

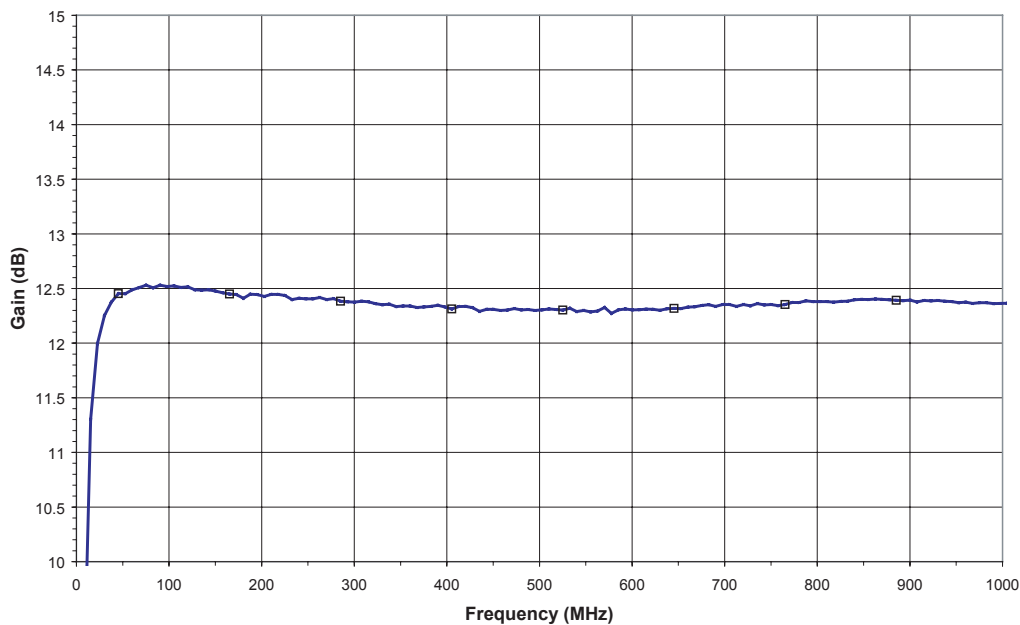


Figure 4: Typical Input Return Loss (S11) vs. Frequency

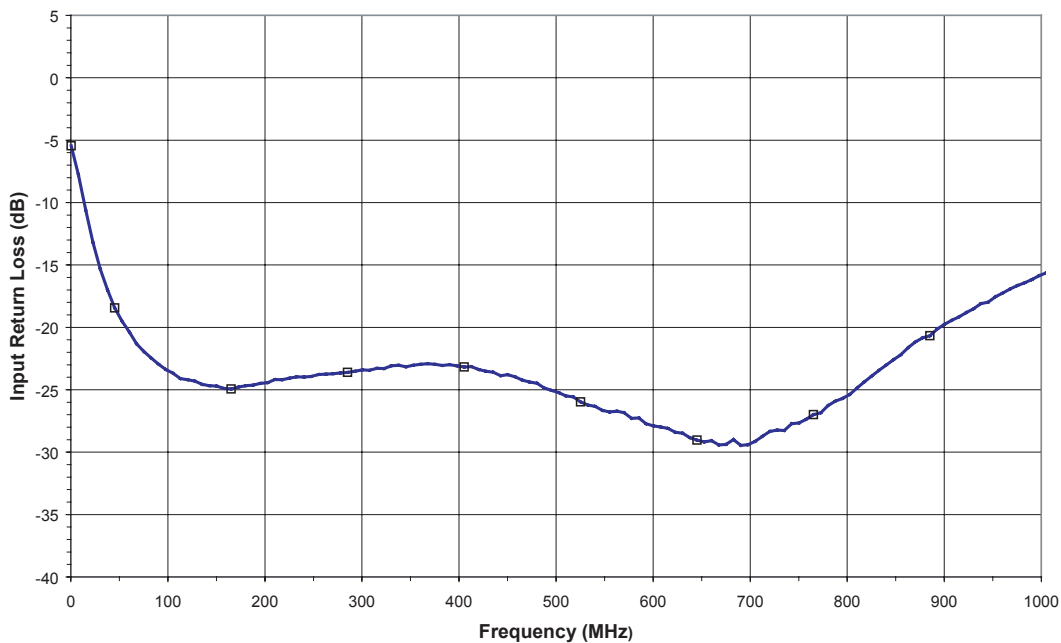


Figure 5: Typical Output Return Loss (S22) vs. Frequency

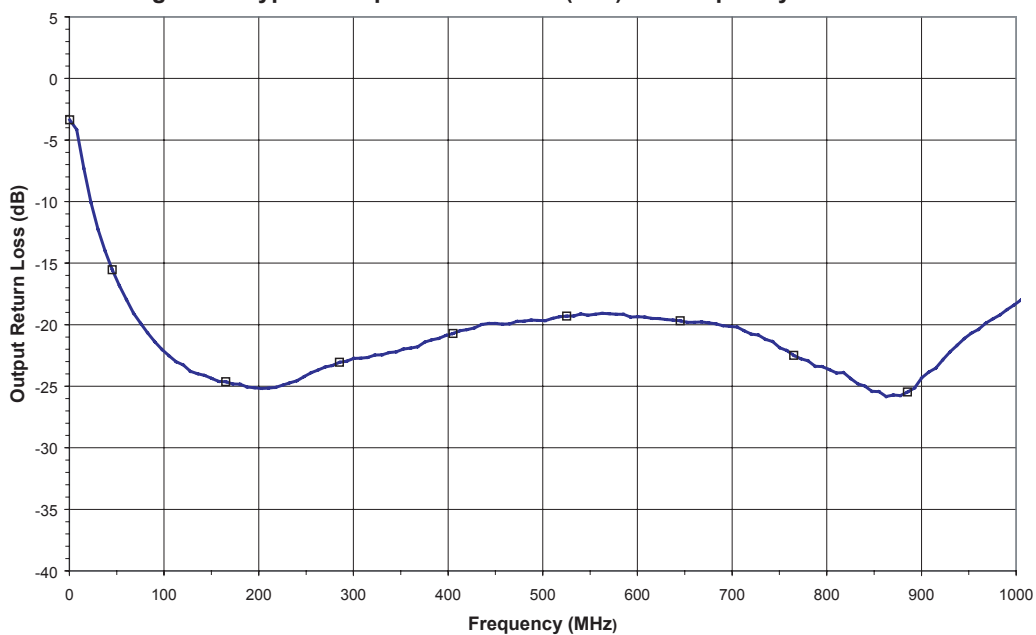


Figure 6: Typical Isolation (S12) vs. Frequency

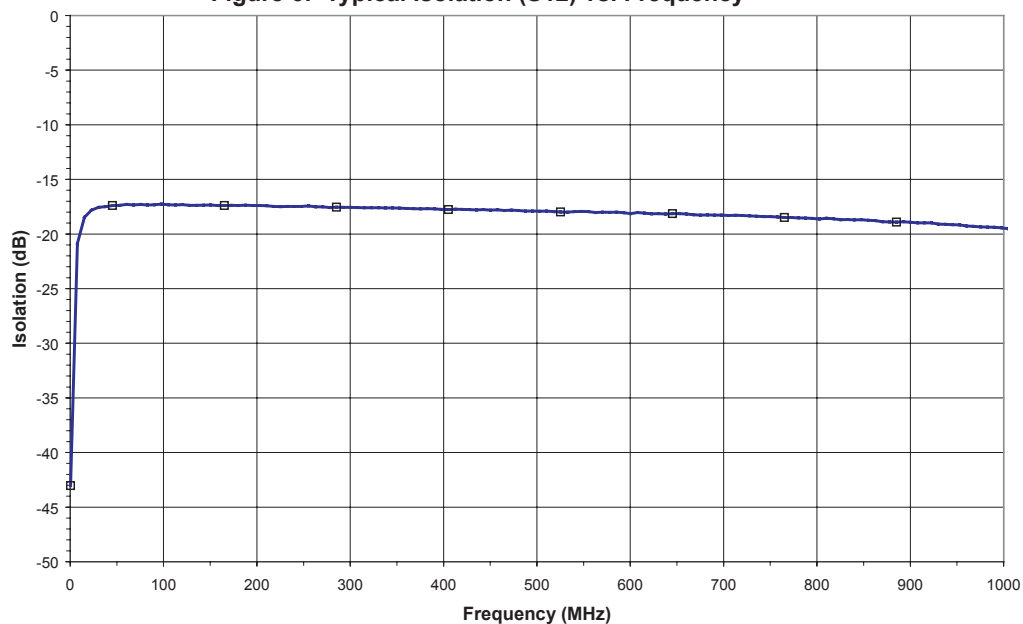
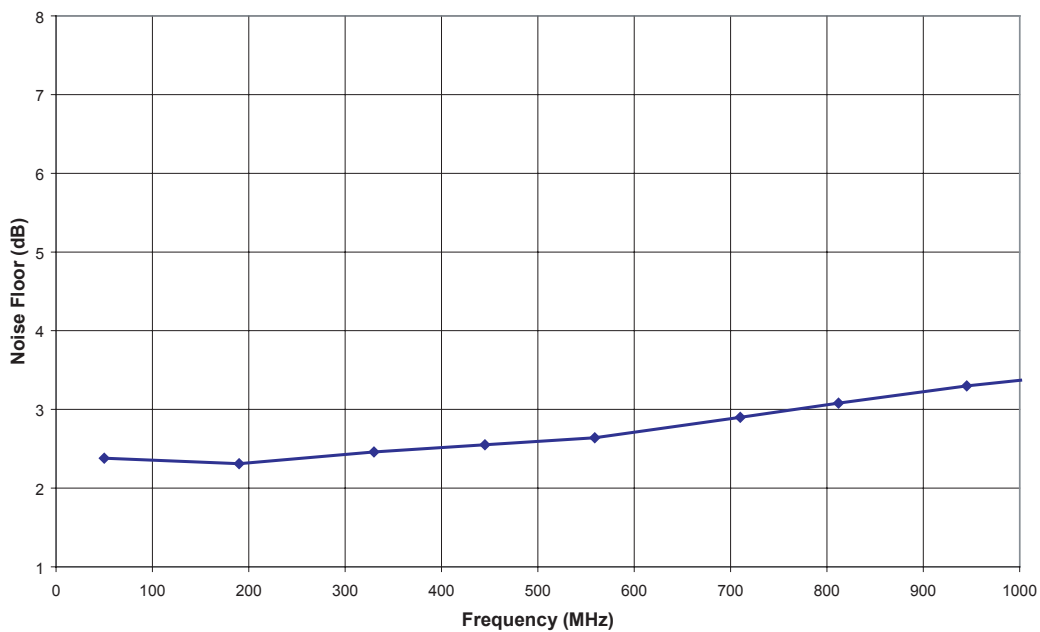


Figure 7: Typical Noise Figure vs. Frequency

APPLICATION INFORMATION

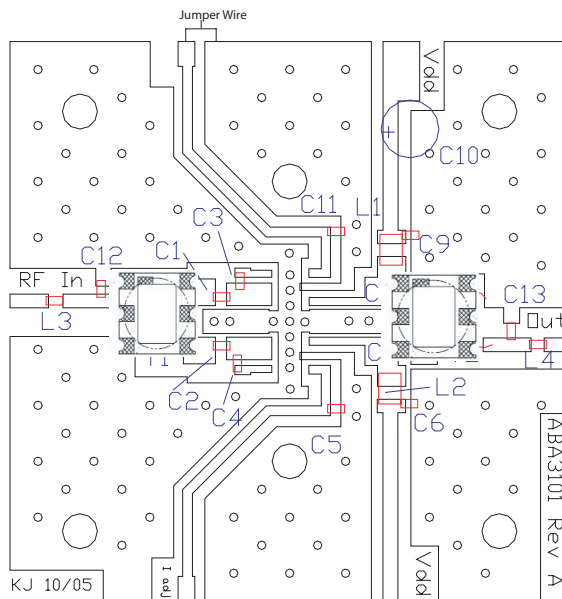
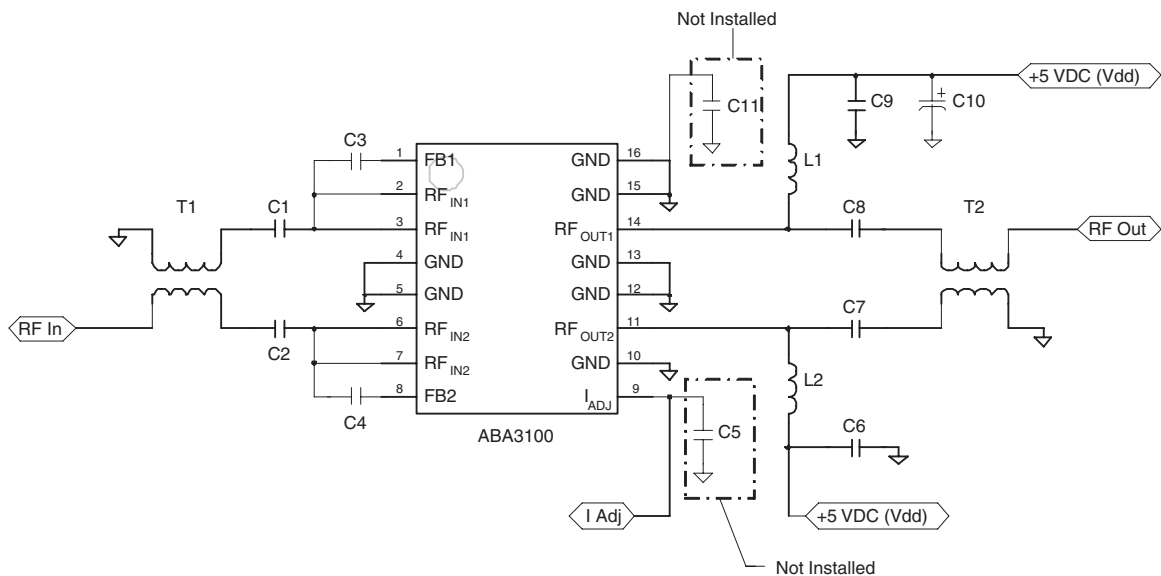


Figure 8: Evaluation Board Layout



* Connecting a resistor from I_{ADJ} to ground lowers current; normal operation is with I_{ADJ} floating.

Figure 9: Evaluation Board Schematic

Table 5: Evaluation Board Parts List

ITEM	DESCRIPTION	QTY	VENDOR	VENDOR PART NUMBER
C1-C4, C6, C9	0.01uF CHIP CAP.	6	MURATA	GRM39X7R1103K25V
C7, C8	470 pF CHIP CAP.	2	MURATA	GRM39COG471J25V
C10	47 uF ELEC. CAP.	1	DIGI-KEY CORP	P5275-ND
C5, C11	(not installed)			
L1, L2	390 nH CHIP INDUCTOR	2	COILCRAFT	1008CS-391XKBC
CONNECTORS	75 Ω N MALE PANEL MOUNT	2	PASTERNAK ENTERPRISES	PE4504
T1, T2	BALUN	2	PULSE ENGINEERING	CX2024
	PCB	1	STANDARD PRINTED CIRCUITS, INC.	EBSTA-111899

Notes:

1. "N" Connector center pin should be approximately 80 mils in length.
2. Connector tabs must be reduced by 150 mils.
3. Device must be soldered on PC board.

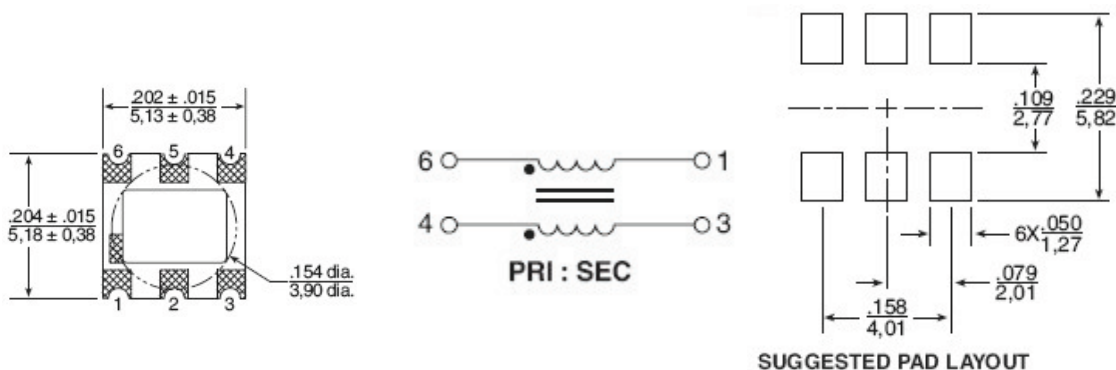
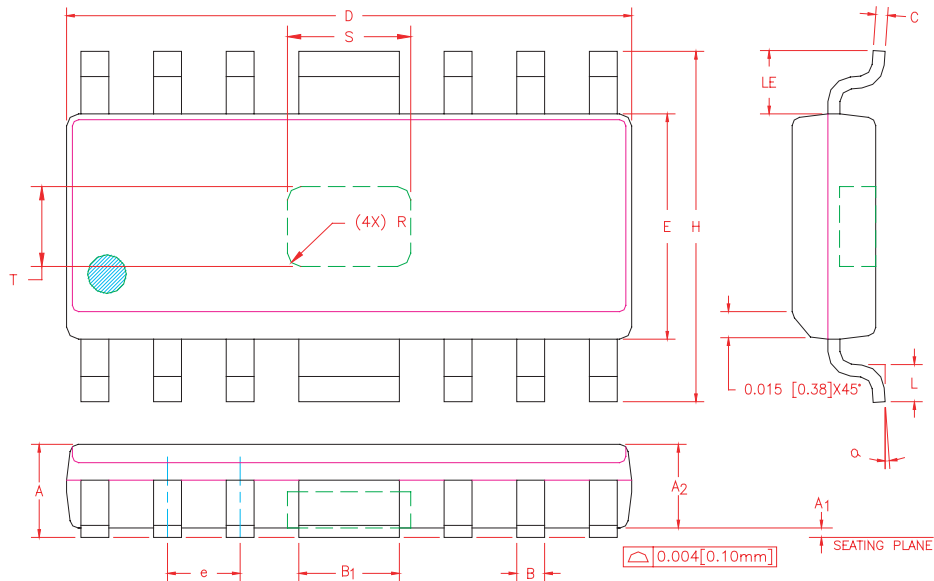


Figure 10: Pulse CX 2024 Balun

Note:

1. Consult Pulse Engineering data sheet for more details.

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A1	0.000	0.004	0.00	0.10	7
A2	0.054	0.065	1.37	1.65	
B	0.013	0.020	0.33	0.50	
B1	0.062	0.070	1.58	1.78	
C	0.008	0.010	0.20	0.25	4
D	0.380	0.400	9.66	10.16	2
E	0.150	0.160	3.81	4.06	3
e	0.050	BSC	1.27	BSC	
H	0.226	0.244	5.74	6.20	
L	0.016	0.040	0.41	1.02	
LE	0.030	—	0.76	—	
alpha	0°	8°	0°	8°	
S	0.070	0.100	1.78	2.54	6
T	0.040	0.070	1.02	1.78	6
R	0.015	REF.	0.38	REF.	6

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ± 0.005 [0.13mm].
5. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.
6. DIMENSIONS "S", "T" AND "R" INDICATE EXPOSED SLUG AREA.
7. A1 STAND OFF IS MEASURED FROM BOTTOM OF HEAT SLUG TO THE SEATING PLANE.

Figure 11: S3 Package Outline - Modified 16 Pin SOIC

NOTES

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ABA3100S3TR	-40 to +85 °C	Modified 16 Pin SOIC	3,500 piece Tape and Reel
ABA3100S3P0	-40 to +85 °C	Modified 16 Pin SOIC	Plastic tubes (50 pieces per tube)
ABA3100RS3P1	-40 to +85 °C	RoHS-Compliant Modified 16 Pin SOIC	3,500 piece Tape and Reel



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