

Vishay Semiconductors

ADD-A-PAK Generation VII Power Modules Schottky Rectifier, 200 A



PRODUCT SUMMARY	
I _{F(AV)}	200 A

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- 150 °C T_J operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- Compliant to RoHS Directive 2002/95/EC
- · Designed and qualified for industrial level

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION

The VSKDS400/045 Schottky rectifier doubler has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 150 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

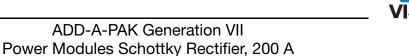
MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL	CHARACTERISTICS	VALUES	UNITS			
I _{F(AV)}	Rectangular waveform	200	А			
V _{RRM}		45	V			
I _{FSM}	t _p = 5 μs sine	29 000	А			
V _F	100 Apk, T _J = 125 °C	0.5	V			
T _J	Range	- 55 to 150	°C			

VOLTAGE RATINGS							
PARAMETER	SYMBOL	VSKDS400/045	UNITS				
Maximum DC reverse voltage	V_{R}	45	V				
Maximum working peak reverse voltage	V_{RWM}	45	V				

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VSKDS400/045

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ABSOLUTE MAXIMUM RATINGS							
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS		
Maximum average forward current	I _{F(AV)}	50 % duty cycle at T_C = 91 °C, rectangular waveform		200			
Maximum peak one cycle	l	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with	29 000	А		
non-repetitive surge current	IFSM	10 ms sine or 6 ms rect. pulse	rated V _{RRM} applied	3400			
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 19 A, L = 1 mH		180	mJ		
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical		40	А		

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
		200 A	T _{.1} = 25 °C	0.67		
Maximum fanyard valtaga dran	V	400 A	0.92	V		
Maximum forward voltage drop	V_{FM}	200 A	T _J = 125 °C	0.73	V	
		400 A		1.14		
Marinana	I _{RM}	T _J = 25 °C	V _R = Rated V _R	20	mA	
Maximum reverse leakage current		T _J = 125 °C		1.2	Α	
Maximum junction capacitance	C _T	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		10 300	pF	
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		5.0	nH	
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs	
Maximum RMS insulation voltage	V _{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V	

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction and storage temperature range		T _J , T _{Stg}		- 55 to 150	°C	
Maximum thermal resistance, junction to case per leg		R _{thJC}	DC operation	0.26	°C/W	
Typical thermal resistance, case to heatsink per module		R _{thCS}	ncs		J/VV	
Approximate weight				75	g	
Approximate weight				2.7	oz.	
Mounting torque ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the	4	Nm	
	busbar		spread of the compound.	3		
Case style			JEDEC	TO-240AA co	mpatible	



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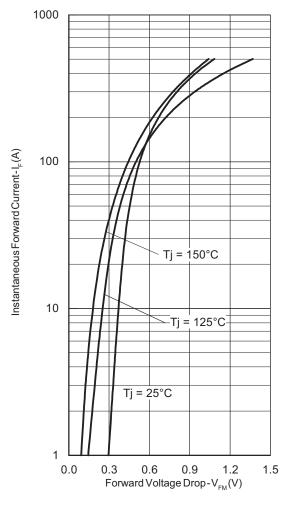


Fig. 1 - Maximum Forward Voltage Drop Characteristics

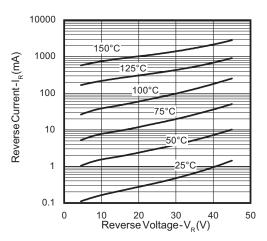


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

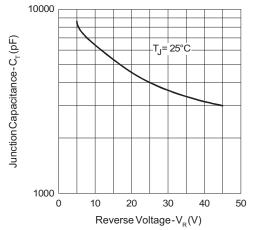


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

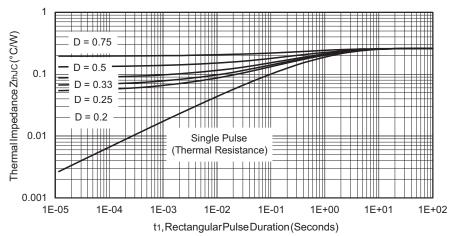


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

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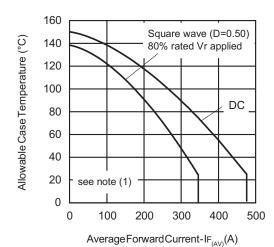
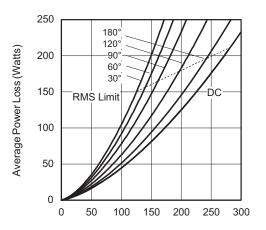
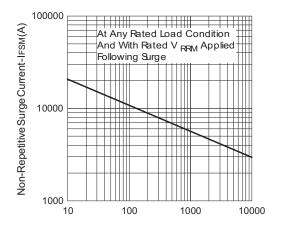


Fig. 5 - Maximum Allowable Case Temperature vs.

Average Forward Current



 $\label{eq:averageForwardCurrent-IF} Average Forward Current-IF_{(AV)}(A)$ Fig. 6 - Forward Power Loss Characteristics



SquareWavePulseDuration-t_p(microsec)
Fig. 7 - Maximum Non-Repetitive Surge Current

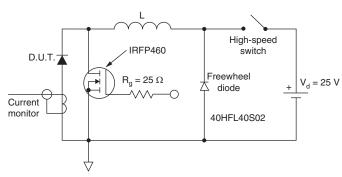


Fig. 8 - Unclamped Inductive Test Circuit

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{th,JC}$; $Pd = Forward power loss = I_{F(AV)} \times V_{FM} at (I_{F(AV)}/D)$ (see fig. 6); $Pd_{REV} = Inverse power loss = V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80 \%$ rated V_R

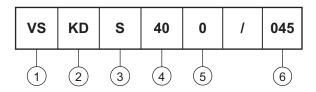


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ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product

2 - Circuit configuration:

KD = ADD-A-PAK - 2 diodes in series

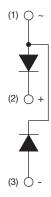
3 - S = Schottky diode

- Average rating (x 10)

- Product silicon identification

6 - Voltage rating (045 = 45 V)

CIRCUIT CONFIGURATION



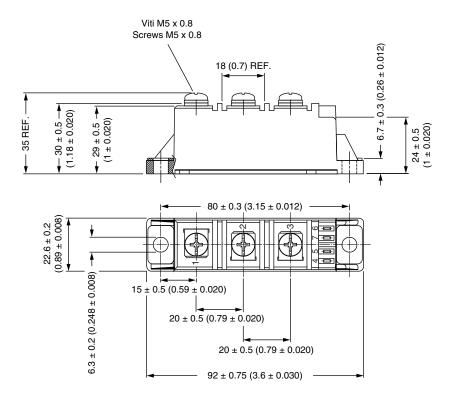
LINKS TO RELAT	ED DOCUMENTS
Dimensions	www.vishay.com/doc?95369



Vishay Semiconductors

ADD-A-PAK Generation VII - Diode

DIMENSIONS in millimeters (inches)







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