PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840004-11

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS840004-11 is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz, 18pF parallel resonant crystal, 125MHz and 62.5MHz can be generated based on one frequency select pin (F_SEL). The ICS840004-11 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The ICS840004-11 is packaged in a small 20-pin TSSOP package.

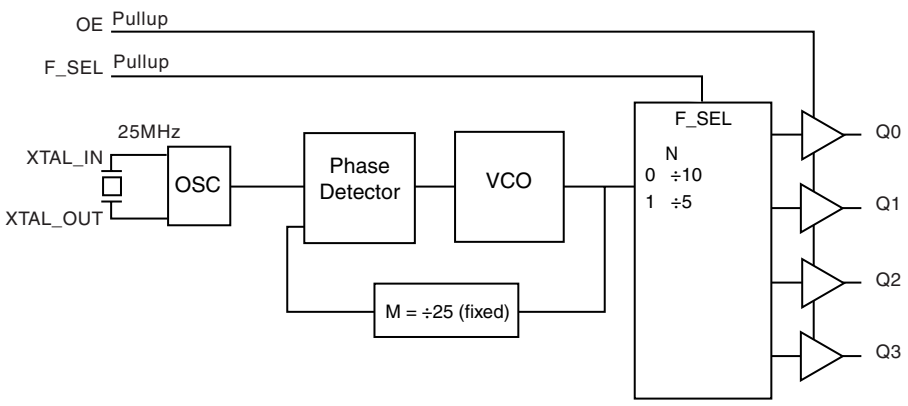
FEATURES

- Four LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Crystal oscillator interface
- Input frequency range: 22.4MHz to 28MHz
- Output frequency Range: 56MHz - 140MHz
- VCO Range: 560MHz - 700MHz
- RMS phase jitter at 125MHz (1.875MHz - 20MHz): 0.70ps (typical)
- RMS phase noise at 125MHz:
- Full 3.3V supply
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

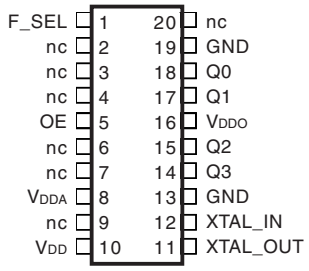
FREQUENCY SELECT FUNCTION TABLE FOR ETHERNET FREQUENCIES

Inputs				Output Frequency (25MHz Ref.)
F_SEL	M Divider Value	N Divider Value	M/N Ratio Value	
0	25	10	2.5	62.5
1	25	5	5	125

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840004-11
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	F_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
2, 3, 4, 6, 7, 9, 20	nc	Unused		No connect.
5	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
10	V_{DD}	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
13, 19	GND	Power		Power supply ground.
14, 15 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedence.
16	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA}, V_{DDO} = 3.465V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DDD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			90		mA
I_{DDA}	Analog Supply Current			8		mA
I_{DDO}	Output Supply Current			5		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DDD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE, F_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	OE, F_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$	2.6			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, 3.3V Output Load Test Circuit.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

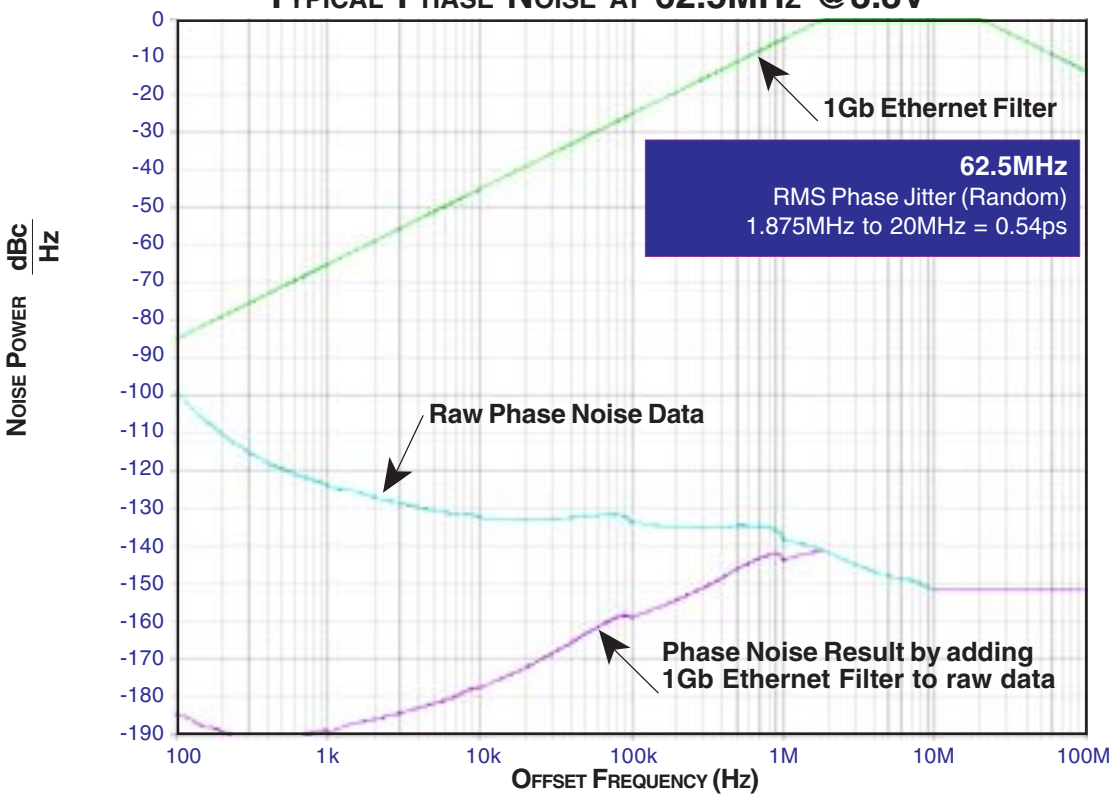
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

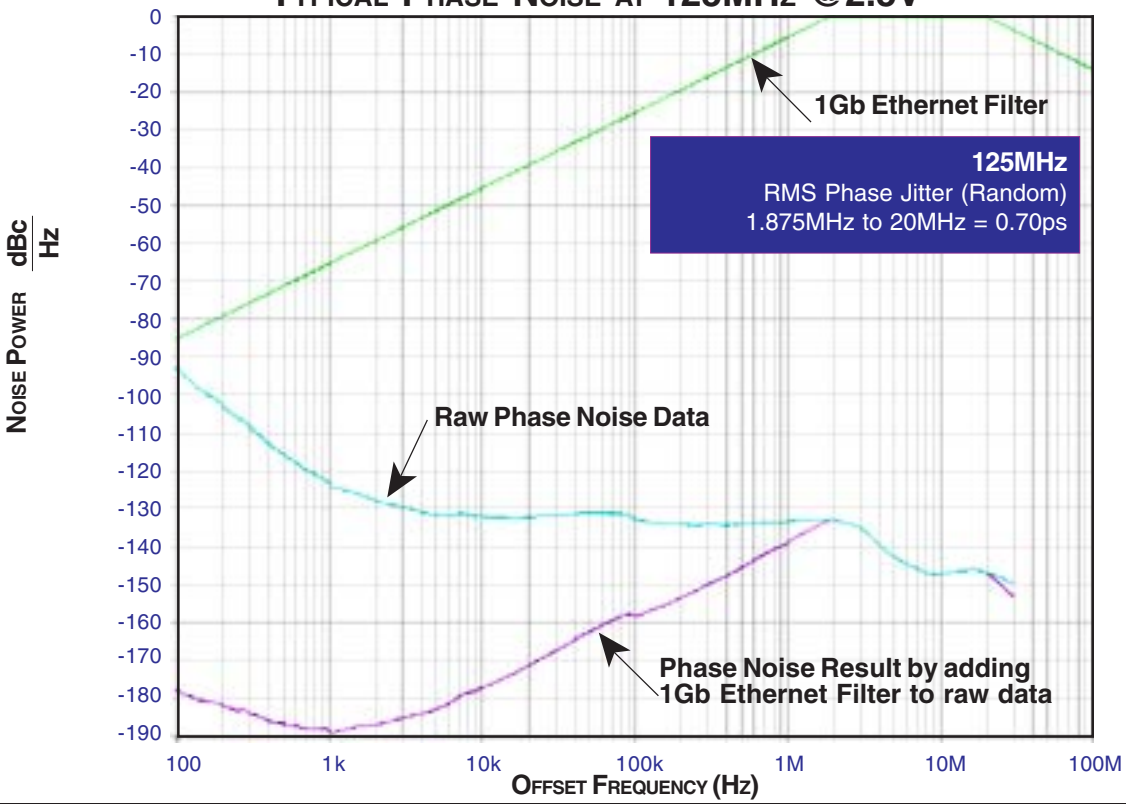
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range		56		140	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			25		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz @ Integration Range: 1.875MHz - 20MHz		0.70		ps
		62.5MHz @ Integration Range: 1.875MHz - 20MHz		0.54		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		470		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

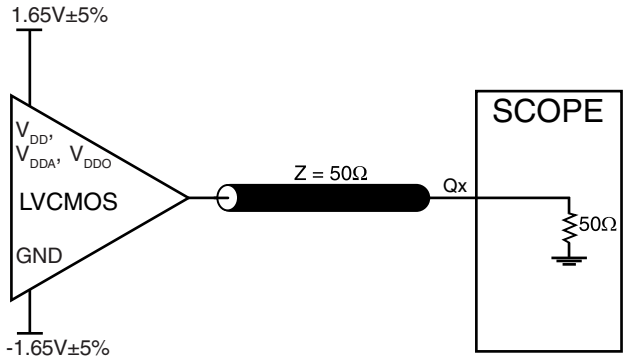
TYPICAL PHASE NOISE AT 62.5MHZ @3.3V



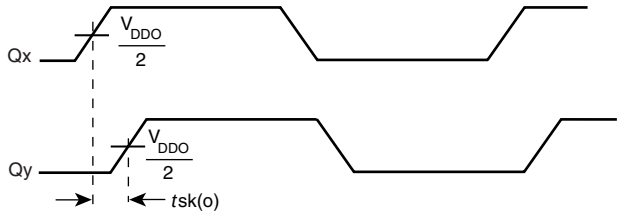
TYPICAL PHASE NOISE AT 125MHZ @2.5V



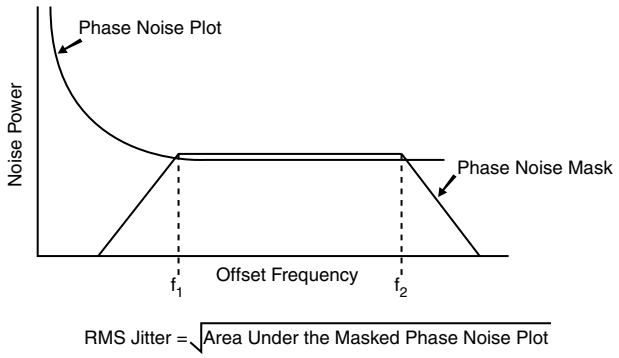
PARAMETER MEASUREMENT INFORMATION



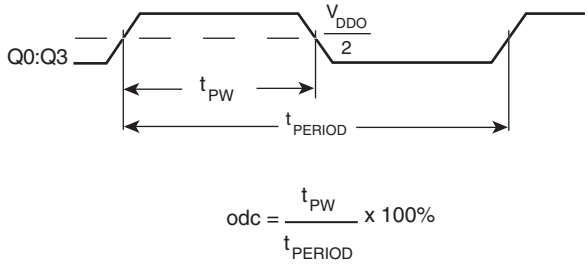
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



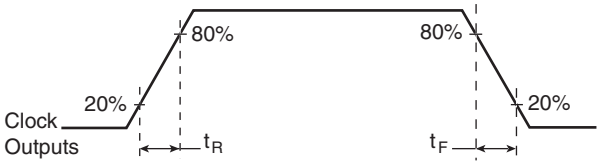
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840004-11 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

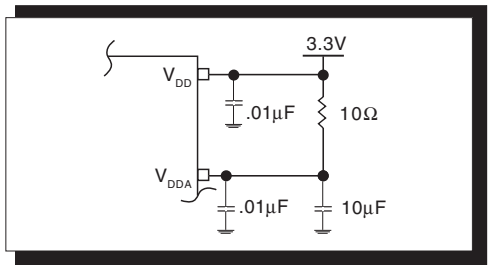


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840004-11 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

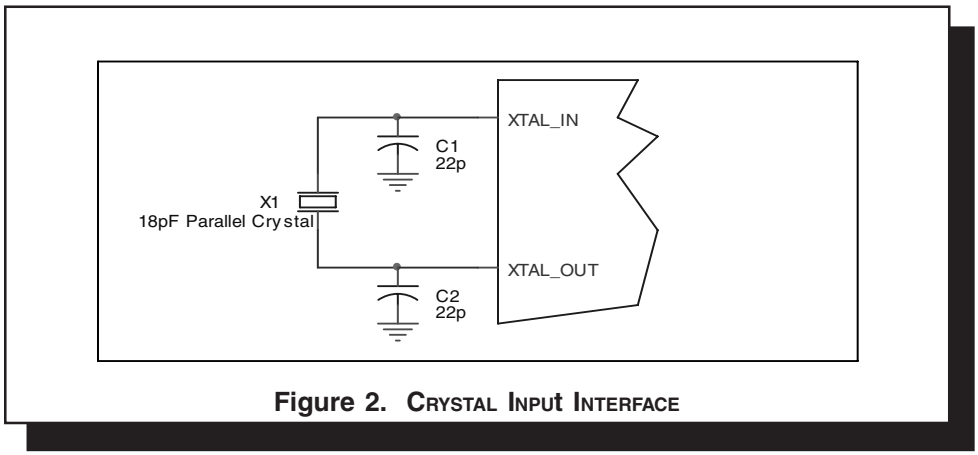


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840004-11 is: 1795

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

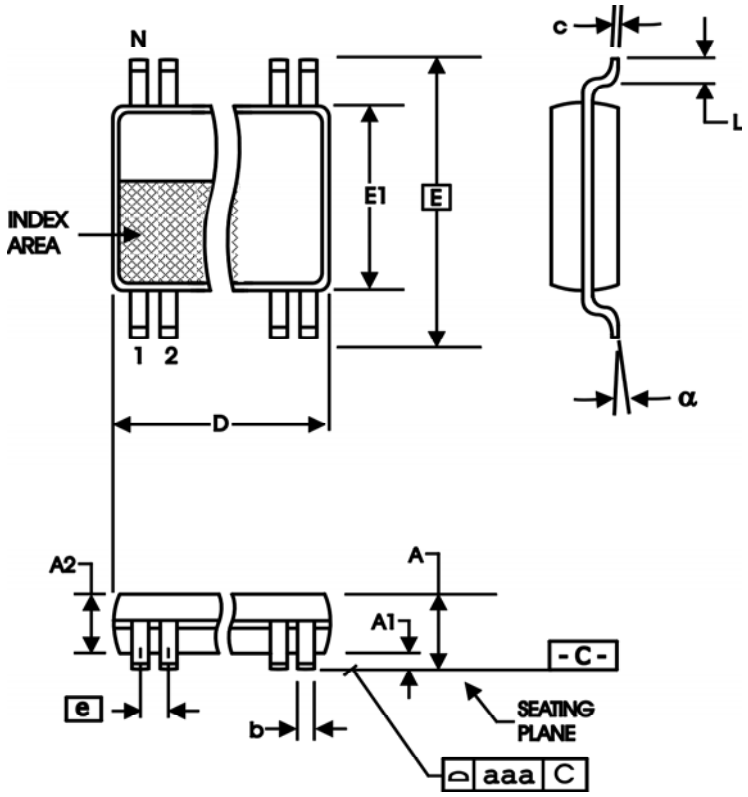


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840004AG-11	ICS840004A11	20 Lead TSSOP	tube	0°C to 70°C
ICS840004AG-11T	ICS840004A11	20 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS840004AG-11LF	ICS40004A11L	20 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS840004AG-11LFT	ICS40004A11L	20 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.