BUILT ON Power™

SAFE ASSURE™ by Freescale

Power Architecture® MCUs

PXS30 Family Built on Power Architecture® Technology

Safety with performance

Target Applications

Factory Automation

- Programmable logic control
- Input/output (I/O) control
- Process control, temperature control
- Robotic arm
- Robotic manipulator

Smart Grid and Smart Metering

- Residential solar power inverters
- Commercial solar power inverters
- Off-grid solar power inverters

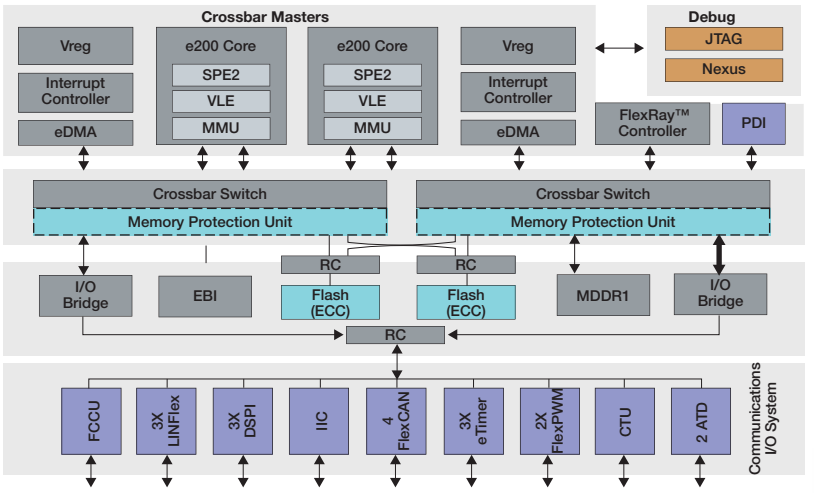
Diagnostic and Therapy

- Anesthesia unit monitors
- Ventilators and respirators

Overview

PSX30 32-bit Power Architecture® based dual-core MCUs are designed specifically for use in industrial safety applications. All devices in this family are built around a dual-core safety platform with an innovative safety concept targeting systems with International Electrotechnical Commission (IEC) 61508 SIL3 safety integrity levels. To minimize additional software and module-level features, on-chip redundancy is offered for the critical components of the MCU. Critical components include the CPU core, DMA controller, interrupt controller, crossbar bus system, memory protection unit, flash memory and RAM controllers, peripheral bus bridge, system timers and watchdog timer. Lock step redundancy checking units are implemented at each output of this sphere of replication. The performance of the PXS30 family is rarely experienced in an MCU with over 600 possible DMIPs, up to 2 MB of flash and Ethernet communication. The PXS30 family is part of the SafeAssure program, which is designed to help system manufacturers more easily achieve compliance with functional safety standards.

PXS30 Block Diagram



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The PXS30 dual-core architecture can be statically switched from lockstep mode to decoupled parallel mode (independent core operation) for applications needing maximum performance or software diversity. A wide variety of industrial applications can be supported, such as motion and power control. For example, the new cross-triggering unit allows control of up to two brushless DC motors or multiple actuators with a minimum interrupt load. Additional features include Ethernet, a fault collection unit, multiple communication modules, two 12-bit ADCs, eTimer units and a built-in hardware self test.

SafeAssure Program: Functional Safety. Simplified.

Freescale's SafeAssure functional safety program is designed to help system manufacturers more easily achieve system compliance with functional safety standards: International Standards Organization (ISO) 26262 and IEC 61508. The program highlights Freescale solutions—hardware and software—that are optimally designed to support functional safety implementations and come with a rich set of enablement collateral. For more information, visit **freescale.com/SafeAssure**.

Development Tools

- MQX™
- RAppID
- FreeMASTER
- CodeWarrior
- Green Hills Software
- Tower System

Challenges and Solutions

System Challenges	PXS30 Solutions
Reduce System Costs and Simplify Design	• Reduces design complexity and component count by putting key functional safety features on a single chip • Dual processing spheres, including CPU, DMA, interrupt controller, crossbar and MPU for logic level fault detection • Dual z7 CPU architecture provides performance to address real-time applications and cross-checking functions common in many safety strategies, which reduces hardware and software complexity used in multiple MCU designs. The architecture can be run in two statistically configurable modes of operation. • Lockstep operation provides a software environment for redundant processing and calculations • Independent core operation (dual parallel mode) provides a software environment for diverse processing and calculations to increase performance or to cross check for reliable operation • Built-in flexible hardware self-test capabilities provide diagnostic coverage both at logic and memory level • Fault collection and control unit manages MCU behavior in the event internal MCU logic faults and signals these to external system components • FlexRay™ protocol and safety ports for robust communications • Probability of undetected failure per hour (PFH) = 0.1 FIT (one failure per every 10 billion hours) • Designed to target safety requirements outlined in IEC61511 and IEC61508 (SIL3), which reduces system cost and effort
Precise Control for Real-Time Applications	• e200 z7 CPU at 180 MHz provides computational performance targeted at vector-oriented control of motor applications • Dual-core architecture provides computation ability for complex applications or cross-checking requirements of safety applications • Precise control of integrated electric motor control periphery • Advanced PWM for specialized multi-phase motor control requirements • Configurable alignment • High frequency above 100 MHz • Dead time insertion • Skew correction • Cross-triggering unit coordinates ADC, timer and PWM generation and minimizes CPU interrupt load eTimer units handle rotor position and speed acquisition and offer six dual-action IC/OC channels with incremental/quadrature encoder mode • Two 12-bit ADCs offer precise conversion for an improved driving experience • FlexRay protocol for fault-tolerant communications with other networked modules within the vehicle • Up to 2 MB flash • Up to 512 KB SRAM • Motor control library of common functions • Ability to control two three-phase motors

Selector Guide

Temperature Range: -40ºC to +105ºC: Select Parts +125°C

Product Number	Speed (MHz)	Flash/RAM	Package
PXS3010	150	1 MB/256 KB	257 MAPBGA
PXS3015	180	1.5 MB/384 KB	473 MAPBGA
PXS3020	180	2 MB/512 KB	473 MAPBGA

For current information about PXS30 family products and documentation, please visit freescale.com/PXS30 and freescale.com/Tower

Document Number: PXS30FS REV 1