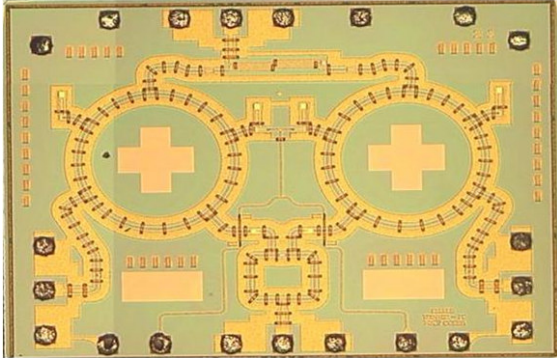
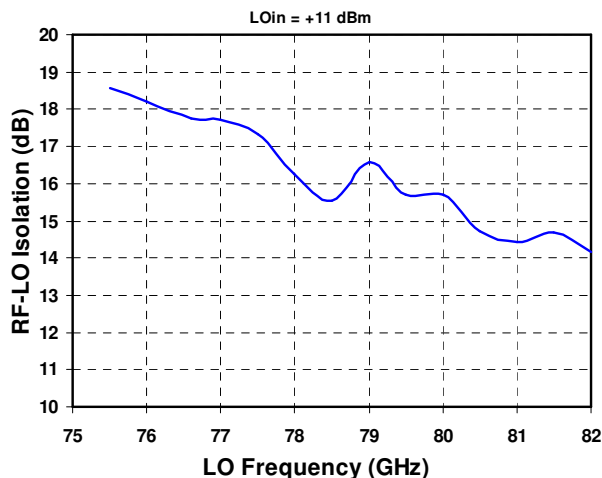
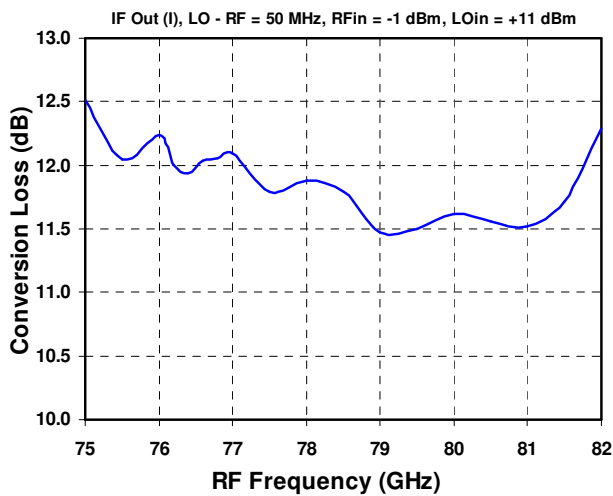


## 77 GHz Down Converting IQ Mixer



### Measured Performance

Bias conditions:  $V_b = 1.1$  V



### Key Features

- RF & LO Frequency Range: 75 - 82 GHz
- IF Frequency Range: DC - 100 MHz
- Conversion Loss: 12 dB @ 77GHz
- RF-LO Isolation: 18 dB @ 77 GHz
- Bias:  $V_b = 1.1$  V
- Technology: HBT with front-side Cu/Sn pillars
- Chip Dimensions: 2.46 x 1.89 x 0.38 mm

### Primary Applications

- Automotive Radar

### Product Description

The TriQuint TGC4702-FC is a down converting IQ mixer designed to cover the automotive radar frequency band.

The TGC4702-FC typically provides 12 dB conversion loss from 75 – 82 GHz to an IF frequency band of DC – 100 MHz. The TGC4702-FC is designed using TriQuint's proven HBT process and front-side Cu / Sn pillar technology for simplified assembly and low interconnect inductance. Die reliability is enhanced by using TriQuint's SiN passivation process.

Lead-free and RoHS compliant.

**Table I**  
**Absolute Maximum Ratings 1/**

Symbol	Parameter	Value	Notes
Vb	Bias Voltage	2 V	<u>2/</u>
Ib	Bias Current	15 mA	<u>2/</u>
Pin	Input Continuous Wave Power (RF + LO)	24 dBm	<u>2/</u>

- 1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

**Table II**  
**Recommended Operating Conditions**

Symbol	Parameter <u>1/</u>	Value
Vb	Bias Voltage	1.1 V
Ib	Quiescent Bias Current	~ 1 mA
P <sub>LO</sub>	LO Input Power	+11dBm

- 1/ See assembly diagram for bias instructions.

**Table III**  
**RF Characterization Table**

**Bias:  $I_b=6\text{mA}$ ,  $F_{LO}=76.55\text{GHz}$ ,  $F_{RF}=76.50\text{ GHz}$ ,  $P_{LO}=11\text{ dBm}$**

<b>PARAMETER</b>	<b>NOMINAL</b>	<b>MAXIMUM</b>	<b>UNITS</b>
Conversion Loss	12	16	dB
RF – LO Output Isolation	16		dB
I-Q Phase	90		Degrees

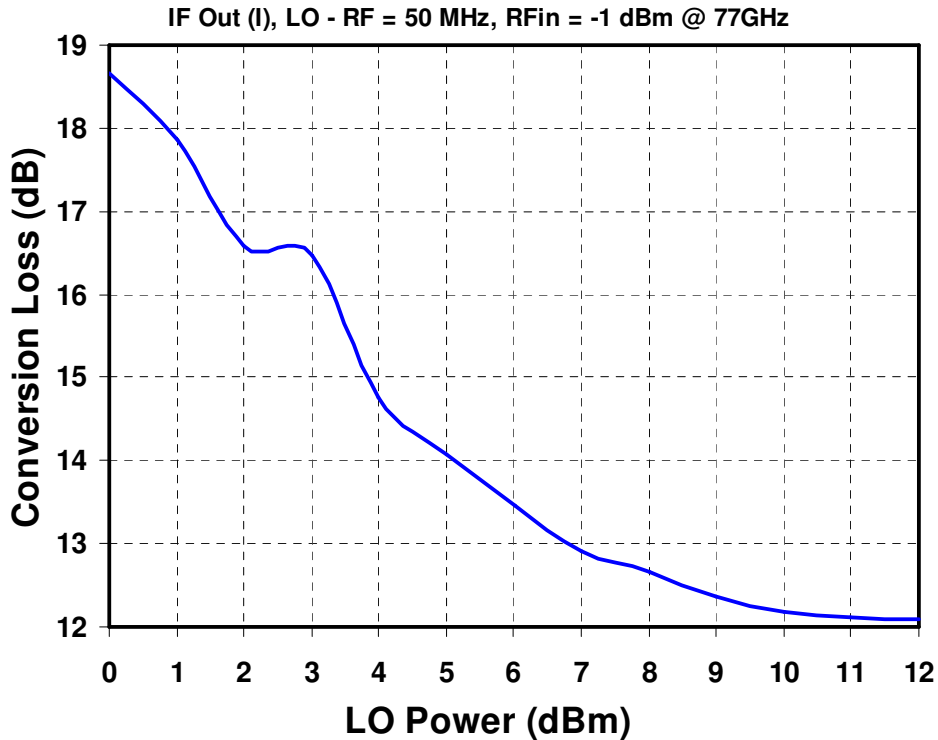
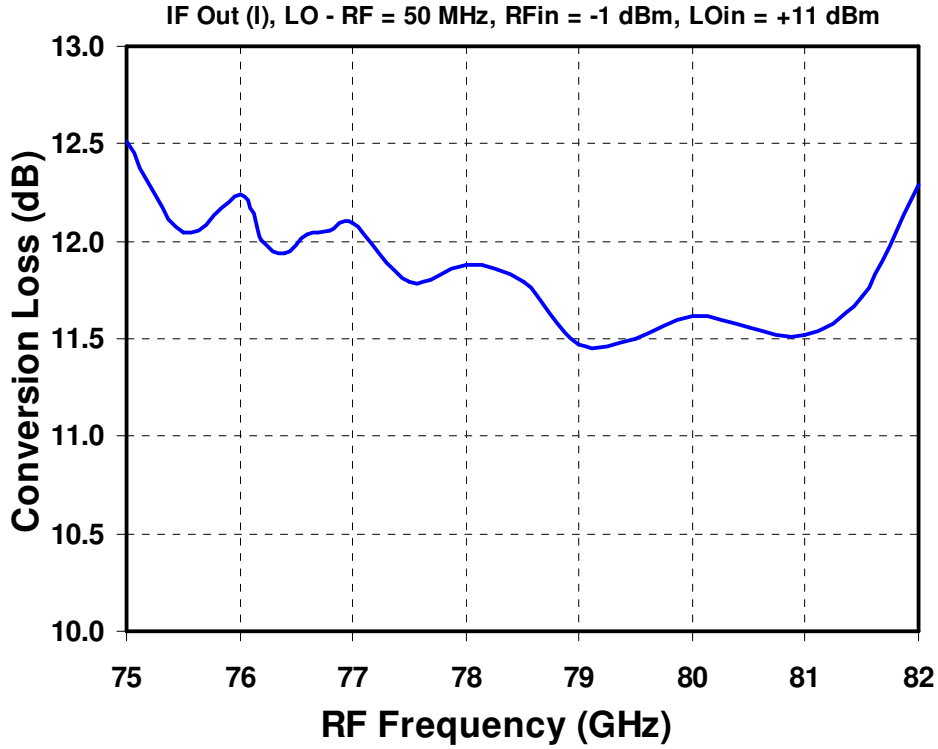
**Table IV  
Power Dissipation and Thermal Properties**

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 85 °C	Pd = 0.25 W	<u>1/</u>
Mounting Temperature		Refer to Solder Reflow Profiles (pg 13)	
Storage Temperature		-65 to 150 °C	

- 1/ Channel operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

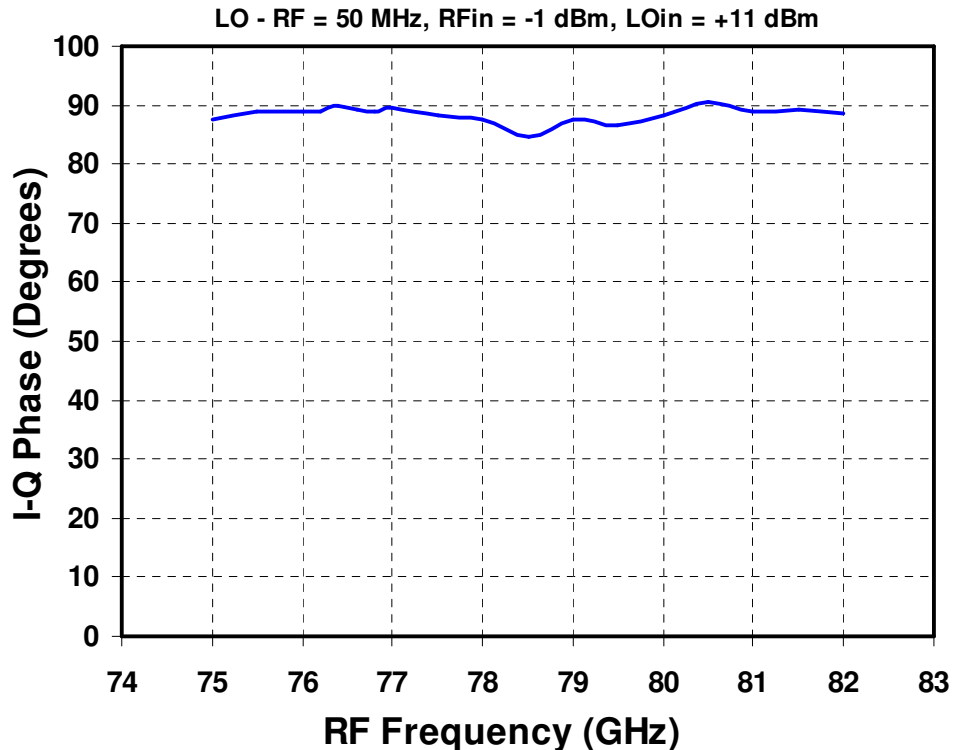
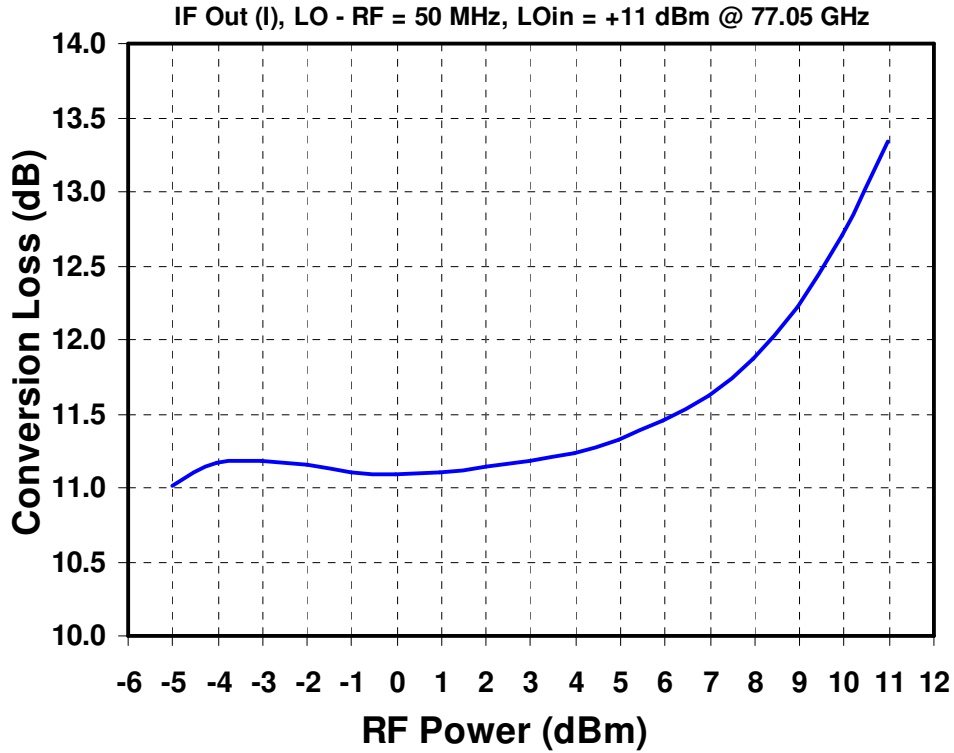
**Measured Data on Flipped Die on Carrier Board**

Bias conditions:  $V_b = 1.1\text{ V}$



**Measured Data on Flipped Die on Carrier Board**

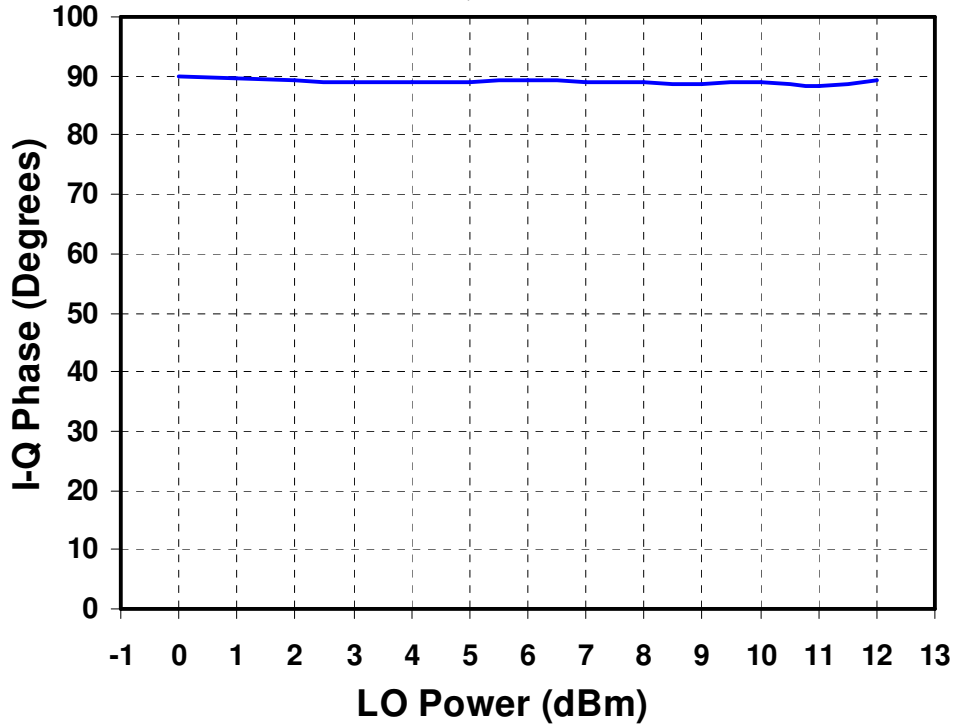
Bias conditions:  $V_b = 1.1\text{ V}$



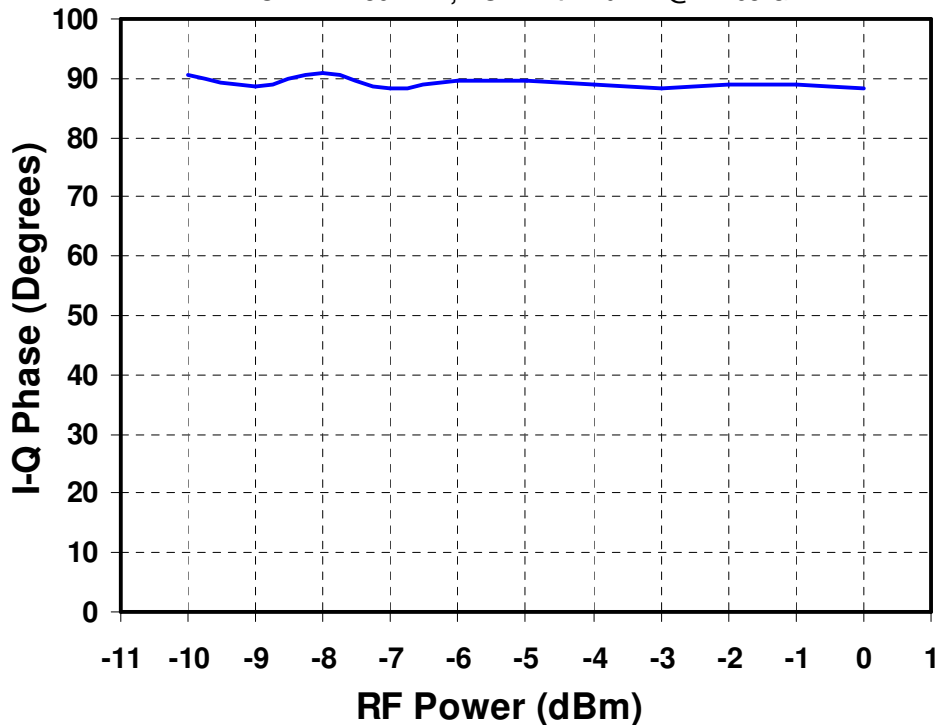
**Measured Data on Flipped Die on Carrier Board**

Bias conditions:  $V_b = 1.1\text{ V}$

LO - RF = 50 MHz, RFin = -1 dBm @ 77 GHz

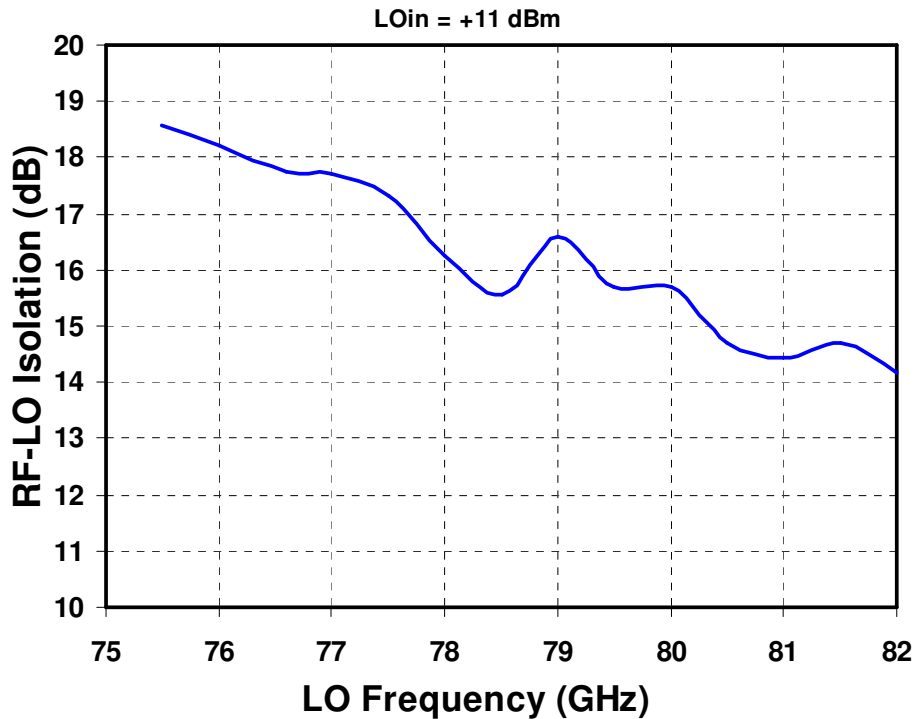
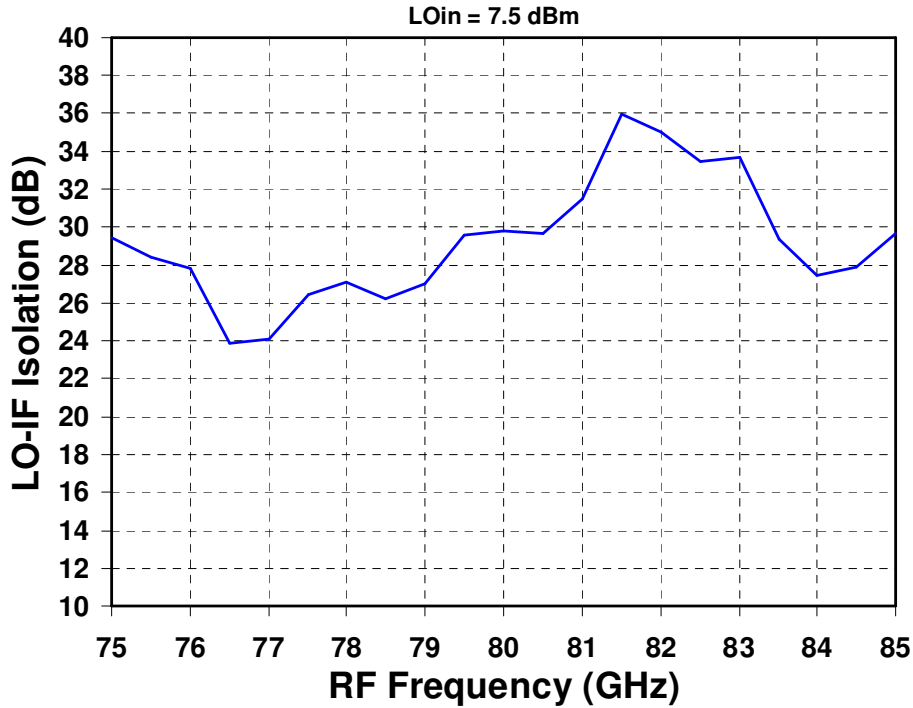


LO - RF = 50 MHz, LOin = +11 dBm @ 77.05 GHz



**Measured Data on Flipped Die on Carrier Board**

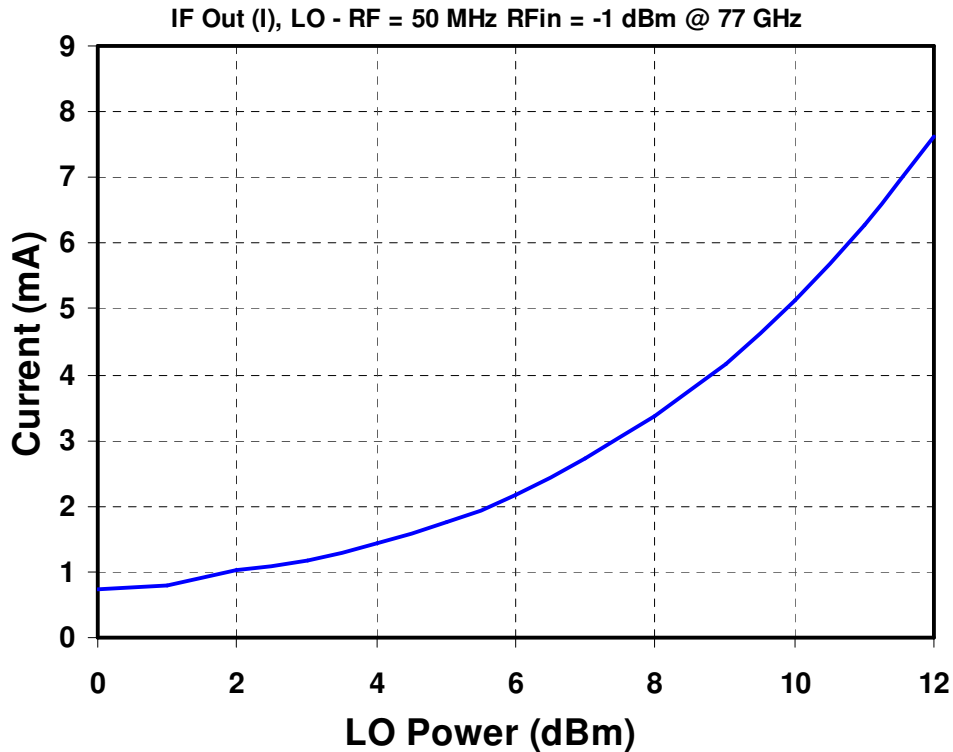
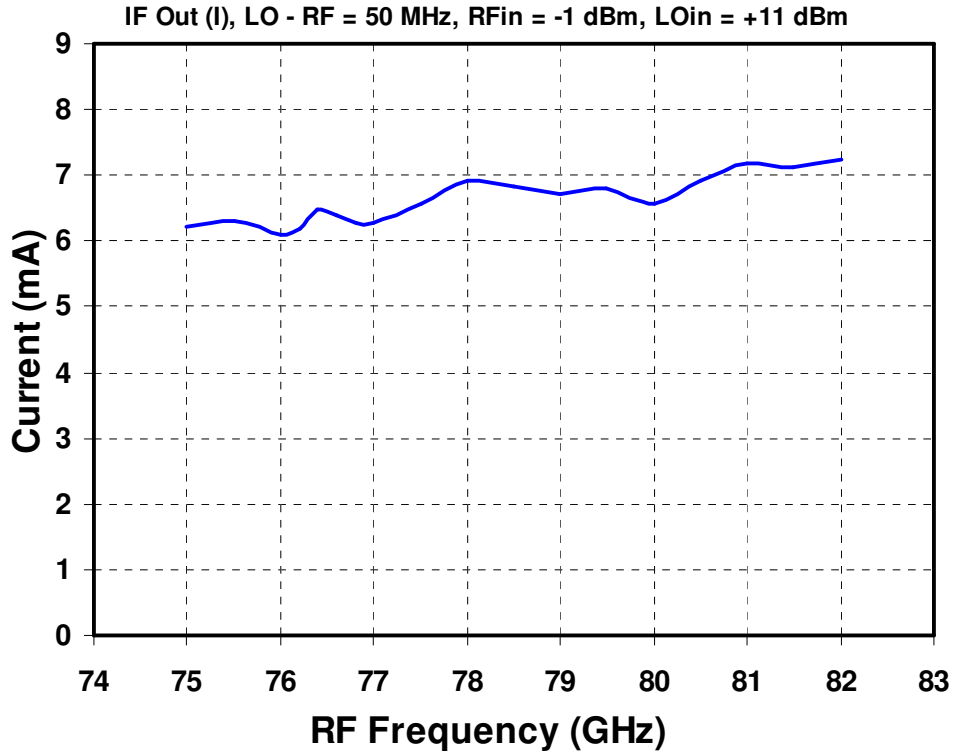
Bias conditions:  $V_b = 1.1\text{ V}$



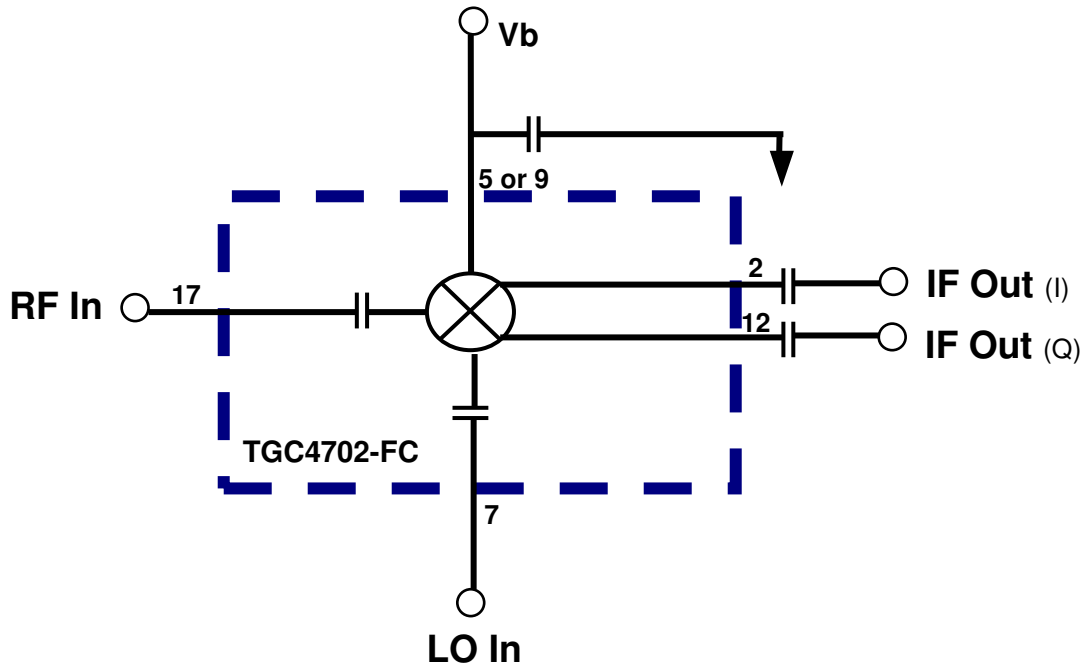


**Measured Data on Flipped Die on Carrier Board**

Bias conditions:  $V_b = 1.1\text{ V}$



**Electrical Schematic**



**Bias Procedures**

**Bias-up Procedure**

Vb set to 0 V

Adjust Vb slowly for 1.1 V (Ib will be ~ 1 mA)

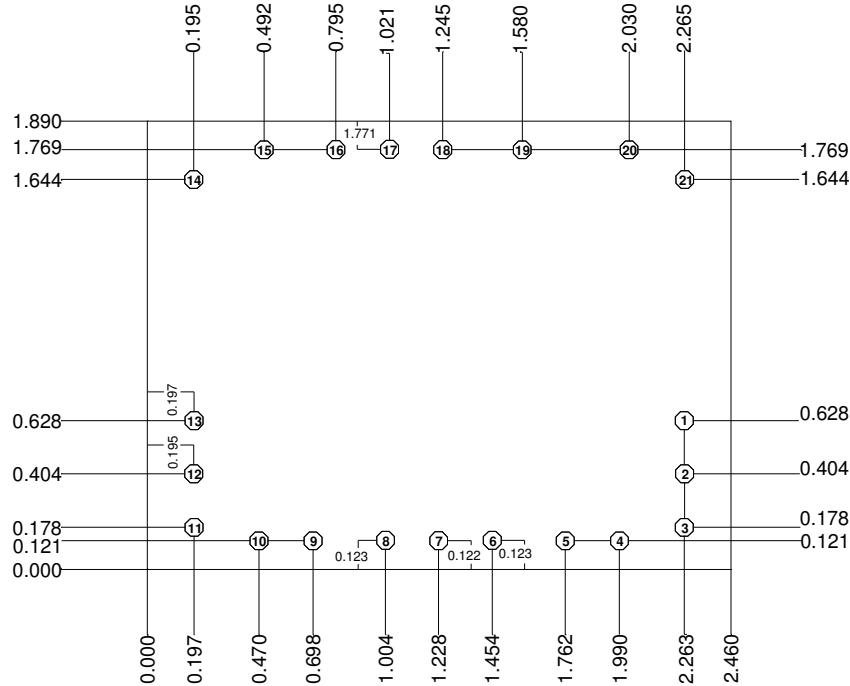
Apply signals to RF In and LO In

**Bias-down Procedure**

Turn off signals

Turn Vb to 0 V

**Mechanical Drawing**  
Drawing is for chip face-up

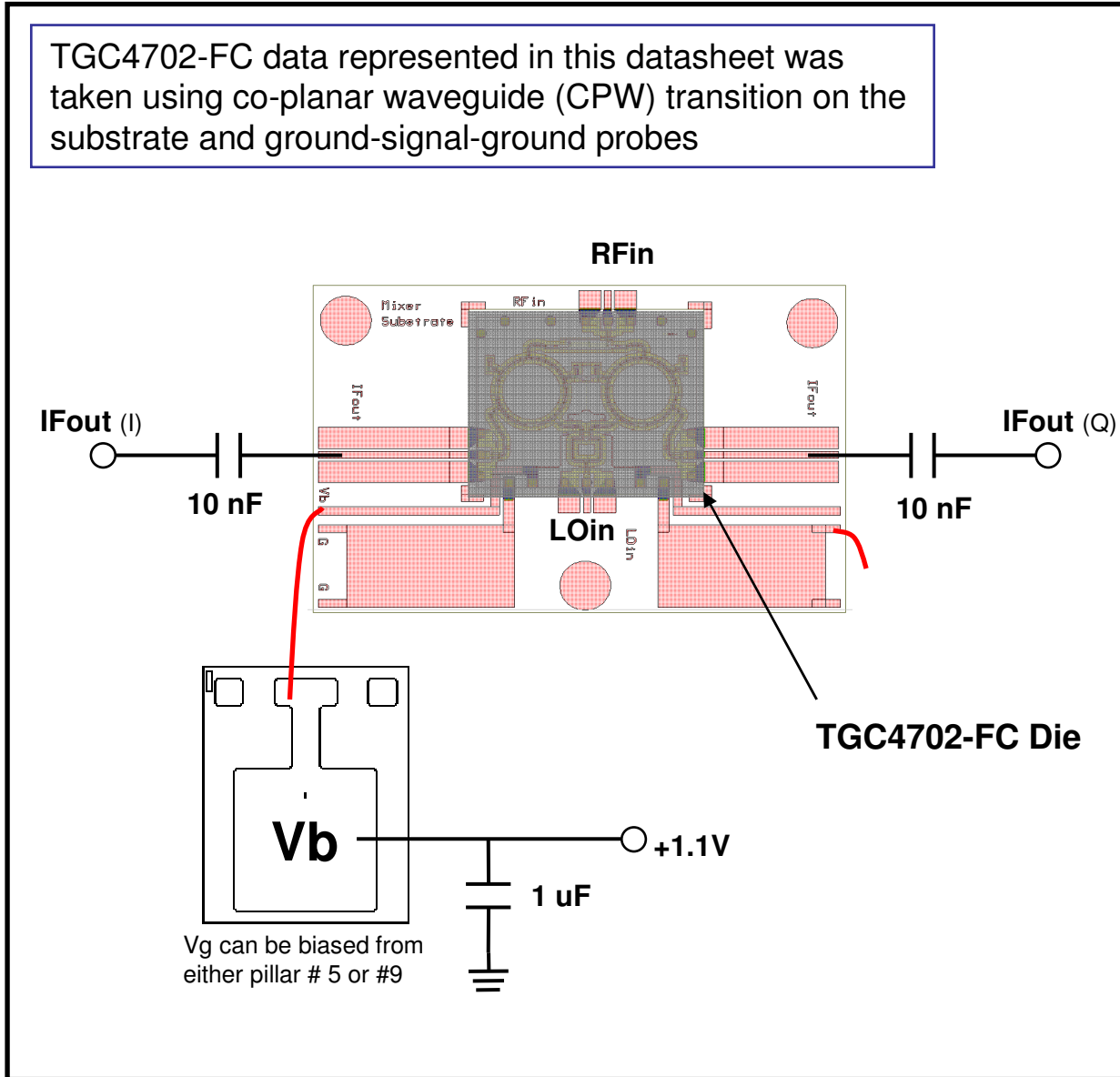


Units: millimeters  
 Thickness: 0.380  
 Die x,y size tolerance: +/- 0.050  
 Chip edge to pillar dimensions are shown to center of pillar

Pillar #1,3,6,8,10, 11,13,16,18	RF CPW Ground	0.075 Ø
Pillar #2	IF Out (I)	0.075 Ø
Pillar #4, 10	DC Ground	0.075 Ø
Pillar #5, 9	Vb	0.075 Ø
Pillar #7	LO In	0.075 Ø
Pillar #12	IF Out (Q)	0.075 Ø
Pillar #17	RF In	0.075 Ø
Pillar #14, 15, 19, 20, 21	Mech. Support Only	0.075 Ø

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

**Recommended Assembly Diagram**



Die is flip-chip soldered to a 15 mil thick alumina test substrate

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

## Assembly Notes

Component placement and die attach assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- Cu pillars on die are 65 um tall with a 22 um tall Sn solder cap.
- Recommended board metallization is evaporated TiW followed by nickel/gold at pillar attach interface. Ni is the adhesion layer for the solder and the gold keeps the Ni from oxidizing. The Au should be kept to a minimum to avoid embrittlement; suggested Au / Sn mass ratio must not exceed 8%.
- Au metallization is not recommended on traces due to solder wicking and consumption concerns. If Au traces are used, a physical solder barrier must be applied or designed into the pad area of the board. The barrier must be sufficient to keep the solder from undercutting the barrier.

Reflow process assembly notes:

- Minimum alloying temperatures 245 °C.
- Repeating reflow cycles is not recommended due to Sn consumption on the first reflow cycle.
- An alloy station or conveyor furnace with an inert atmosphere such as N2 should be used.
- Dip copper pillars in “no-clean flip chip” flux prior to solder attach. Suggest using a high temperature flux. Avoid exposing entire die to flux.
- If screen printing flux, use small apertures and minimize volume of flux applied.
- Coefficient of thermal expansion matching between the MMIC and the substrate/board is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.
- Suggested reflow will depend on board material and density.

## Typical Reflow Profiles for TriQuint Cu / Sn Pillars

Process	Sn Reflow
Ramp-up Rate	3 °C/sec
Flux Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C
Time above Melting Point (245 °C)	60 – 150 sec
Max Peak Temperature	300 °C
Time within 5 °C of Peak Temperature	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec

## Ordering Information

Part	Package Style
TGC4702-FC	GaAs MMIC Die

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***