



TO-92



Pin Definition:

1. Gate
2. Drain
3. Source

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
500	5.5 @ $V_{GS}=10V$	0.5

### General Description

The TSM1N50 is used an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain- to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

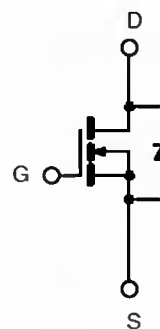
### Features

- Robust high voltage termination
- Avalanche energy specified
- Diode is characterized for use in bridge circuits
- Source to Drain diode recovery time comparable to a discrete fast recovery diode.
- $I_{DSS}$  and  $V_{DS(on)}$  specified at elevated temperature

### Ordering Information

Part No.	Package	Packing
TSM1N50CT B0	TO-92	1Kpcs / Bulk
TSM1N50CT A3	TO-92	2Kpcs / Ammo

### Block Diagram



N-Channel MOSFET

### Absolute Maximum Rating ( $T_a = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain Current	$I_D$	0.5	A
Pulsed Drain Current	$I_{DM}$	2	A
Single Pulse Drain to Source Avalanche Energy ( $V_{DD} = 100V$ , $V_{GS}=10V$ , $I_{AS}=2A$ , $L=10mH$ , $R_G=25\Omega$ )	EAS	50	mJ
Peak Diode Recovery dv/dt ( $I_{SD}\leq 1A$ , $di/dt\leq 300A/\mu S$ , $V_{DD}\leq 200V$ , Starting $T_J=25^\circ\text{C}$ )	dv/dt	4.5	V/nS
Maximum Power Dissipation @ $T_a = 25^\circ\text{C}$	$P_D$	0.625	W
Operating Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

### Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	$T_L$	10	S
Thermal Resistance - Junction to Ambient	$R_{\theta JA}$	208	$^{\circ}\text{C/W}$
Thermal Resistance - Junction to Lead	$R_{\theta JL}$	56	$^{\circ}\text{C/W}$

Notes: Surface mounted on FR4 board  $t \leq 10\text{sec}$

### Electrical Specifications (Ta=25°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	$BV_{DSS}$	500	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.5A$	$R_{DS(ON)}$	--	4.6	5.5	$\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2.0	--	4.0	V
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$	$I_{DSS}$	--	--	10	$\mu\text{A}$
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Forward Transconductance	$V_{DS} \geq 50V, I_D = 0.3A$	$g_{fs}$	--	5	--	S

#### Dynamic<sup>b</sup>

Total Gate Charge	$V_{DS} = 400V, I_D = 1A,$ $V_{GS} = 10V$	$Q_g$	--	4.5	6	nC
Gate-Source Charge		$Q_{gs}$	--	1.1	--	
Gate-Drain Charge		$Q_{gd}$	--	2	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	$C_{iss}$	--	155	200	pF
Output Capacitance		$C_{oss}$	--	20	26	
Reverse Transfer Capacitance		$C_{rss}$	--	3	4	

#### Switching<sup>c</sup>

Turn-On Delay Time	$V_{GS} = 10V, I_D = 1A,$ $V_{DS} = 300V, R_G = 6\Omega$	$t_{d(on)}$	--	10	30	nS
Turn-On Rise Time		$t_r$	--	20	50	
Turn-Off Delay Time		$t_{d(off)}$	--	25	45	
Turn-Off Fall Time		$t_f$	--	24	60	

#### Drain-Source Diode Characteristics and Maximum Rating

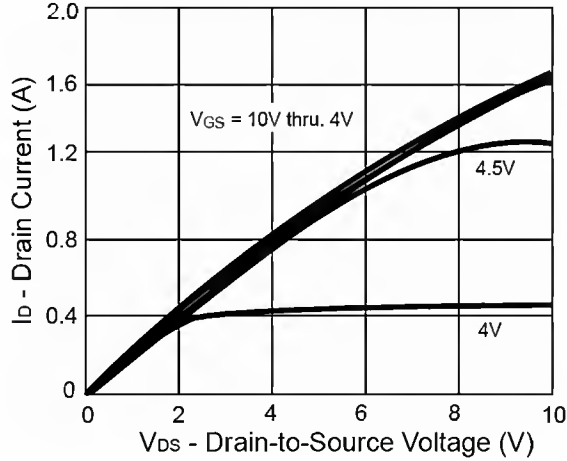
Maximum Continuous Drain-Source Diode Forward Current		$I_S$	--	--	0.5	A
Maximum Pulsed Drain-Source Diode Forward Current		$I_{SM}$	--	--	2	A
Diode Forward Voltage	$I_S = 0.5A, V_{GS} = 0V$	$V_{SD}$	--	--	1.5	V
Reverse Recovery Time	$V_{GS} = 0V, I_S = 0.5A,$ $dI_f/dt = 100A/\mu\text{S}$	$T_{rr}$	--	190	--	nS
Reverse Recovery Charge		$Q_{rr}$	--	0.48	--	$\mu\text{C}$

Notes:

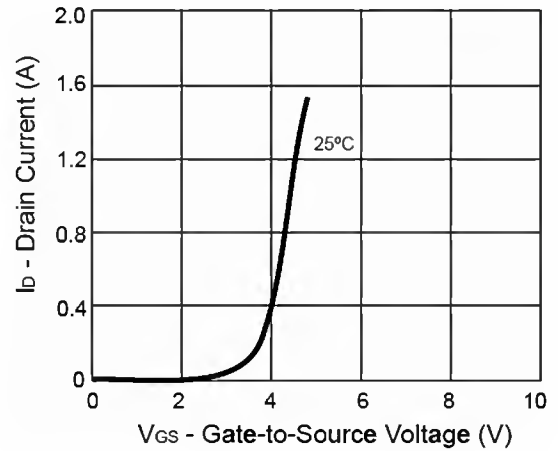
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Pulse test: pulse width  $\leq 300\mu\text{S}$ , duty cycle  $\leq 2\%$
3. For design reference only, not subject to production testing.
4. Switching time is essentially independent of operating temperature.

**Electrical Characteristics Curve** ( $T_a = 25^\circ\text{C}$ , unless otherwise noted)

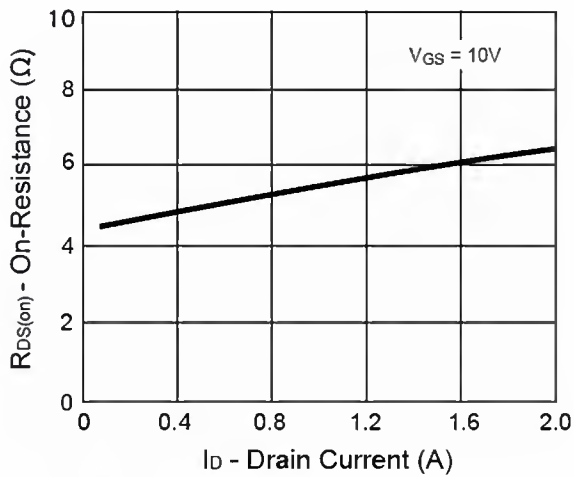
**Output Characteristics**



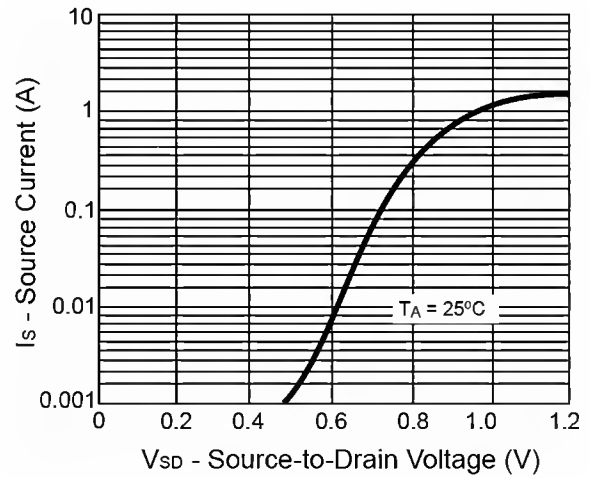
**Transfer Characteristics**



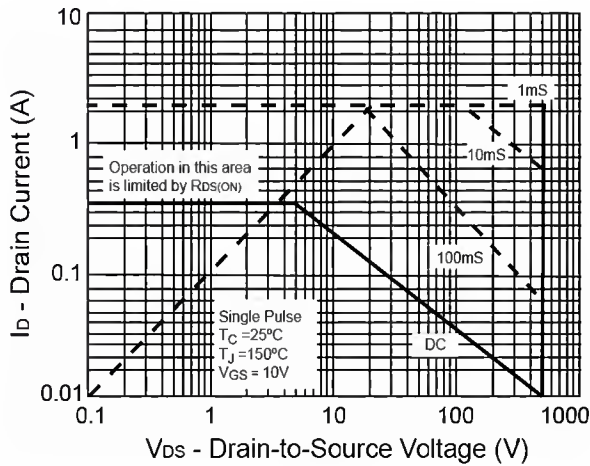
**On-Resistance vs. Drain Current**



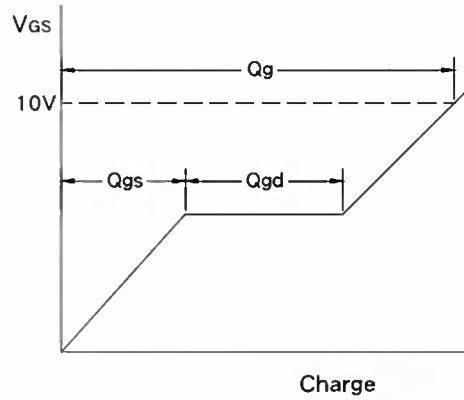
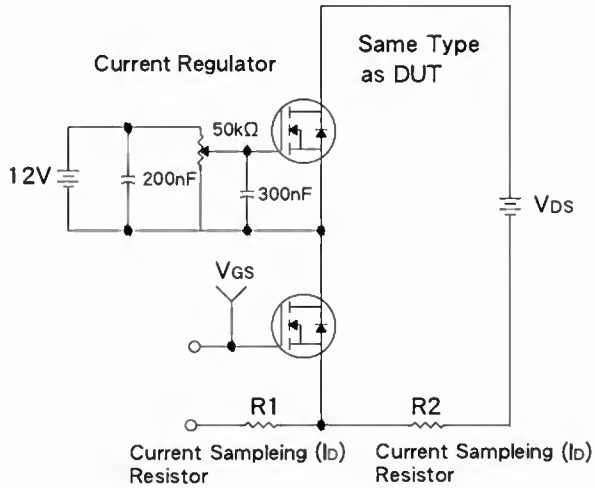
**Source-Drain Diode Forward Voltage**



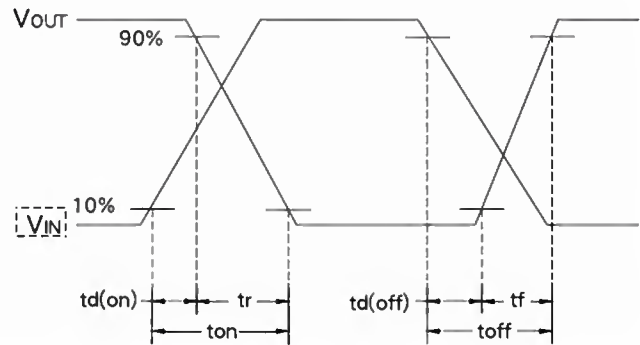
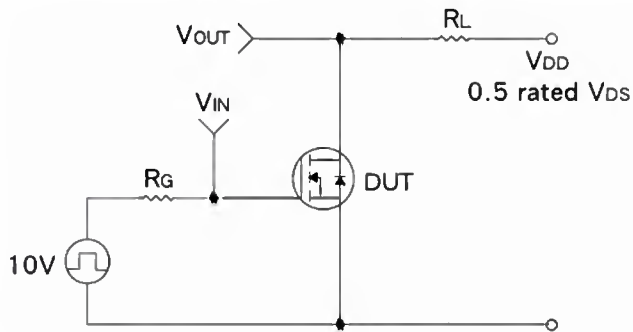
**Maximum Safe Operating Area**



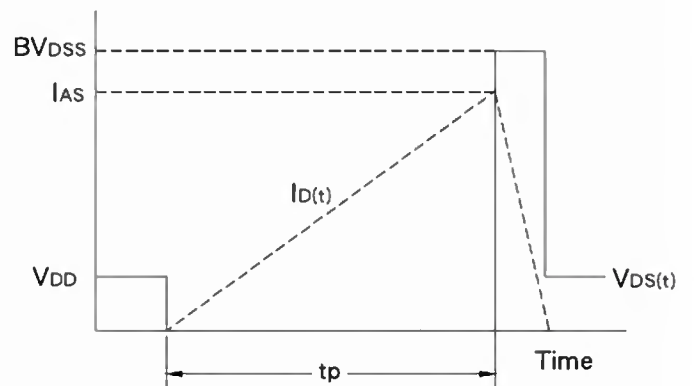
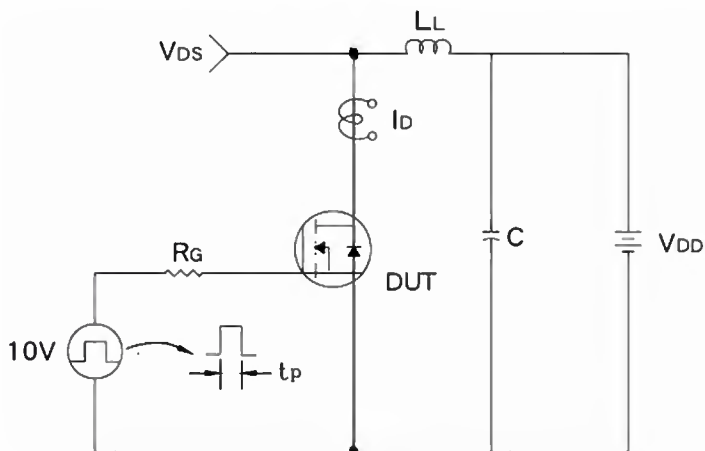
### Gate Charge Test Circuit & Waveform



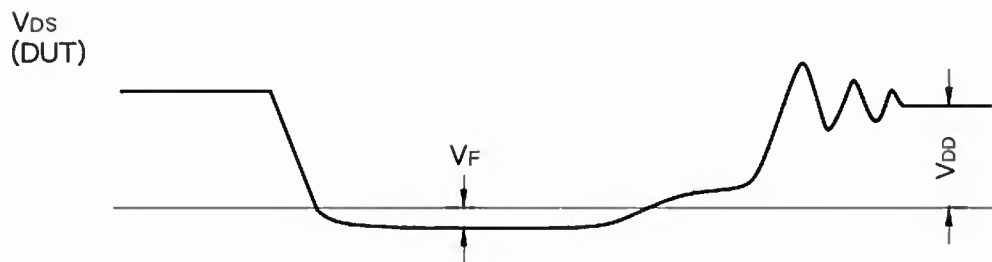
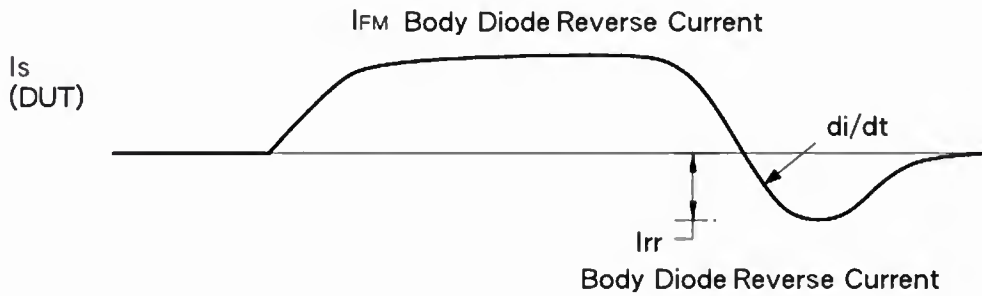
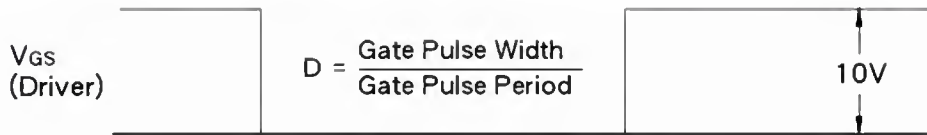
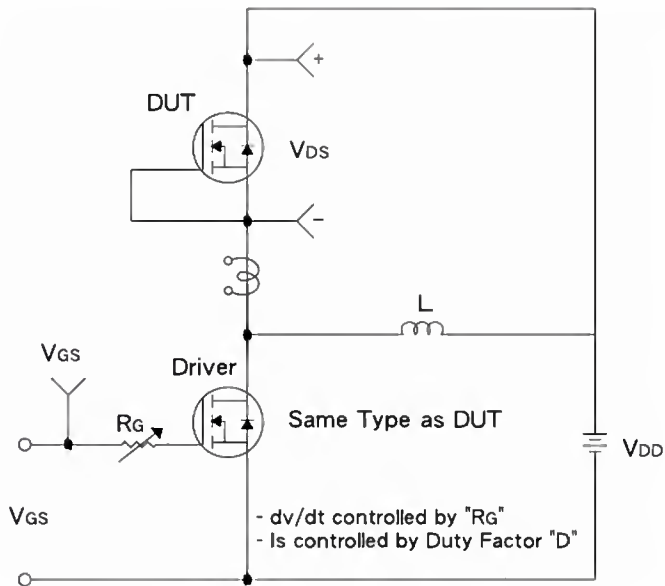
### Resistive Switching Test Circuit & Waveform



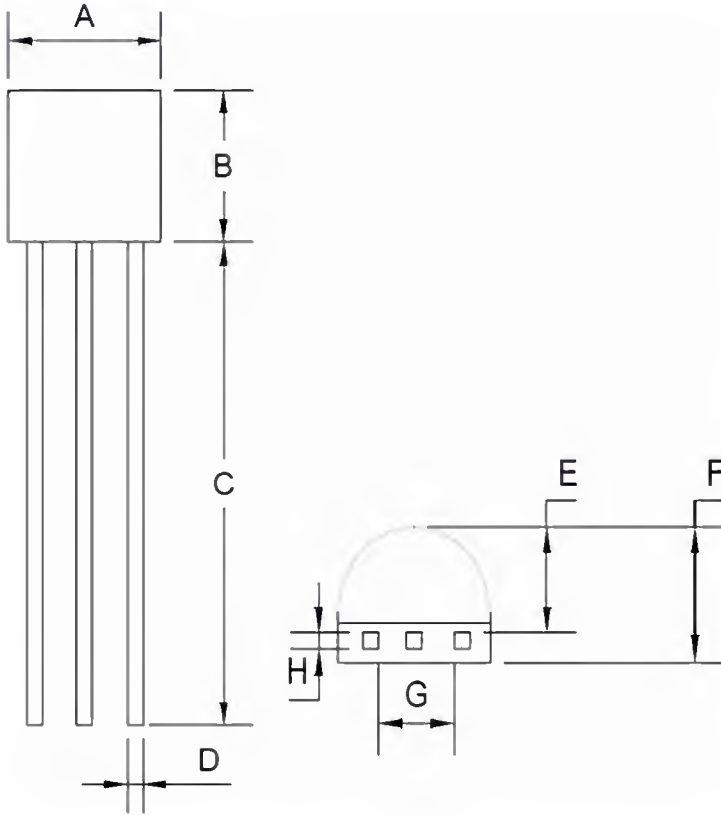
### E<sub>AS</sub> Test Circuit & Waveform



**Diode Reverse Recovery Time Test Circuit & Waveform**

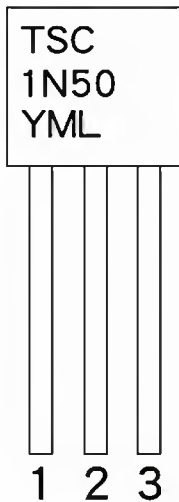


**TO-92 Mechanical Drawing**



TO-92 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.70	0.169	0.185
B	4.30	4.70	0.169	0.185
C	14.30(typ)		0.563(typ)	
D	0.43	0.49	0.017	0.019
E	2.19	2.81	0.086	0.111
F	3.30	3.70	0.130	0.146
G	2.42	2.66	0.095	0.105
H	0.37	0.43	0.015	0.017

**Marking Diagram**



- Y** = Year Code
- M** = Month Code  
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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