NEC

MOS INTEGRATED CIRCUIT

μPD161401

256-COLOR, 1/80-DUTY LCD CONTROLLER/DRIVER WITH ON-CHIP RAM

DESCRIPTION

The μPD161401 is an LCD controller/driver with RAM and is capable of driving a full-dot LCD. It can display 256 colors on an RGB-STN color LCD. This LCD controller/driver can drive a full-dot LCD of up to 101 × 80 pixel with a single chip.

FEATURES

- LCD driver with on-chip display RAM
- Logic power supply operation from +1.8 V to +3.6 V
- Internal booster circuit: x 2 to x 7 selectable
- Dot display RAM: (101 x 80) x 8 bits
- 8 (R, G)/4 (B) grayscales selectable from 17 levels
- Full-dot output: 303 segment lines and 80 common lines
- Serial interface (SI, SCL) or 8-/16-bit parallel data input (i80 or M68 system interface)
- On-chip voltage divider resistor
- Selectable bias value: 1/9 to 1/5
- Selectable duty ratio: 1/80, 1/72 and 1/64 (main duty)
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD161401W/P	Wafer/Chip (supports COF)

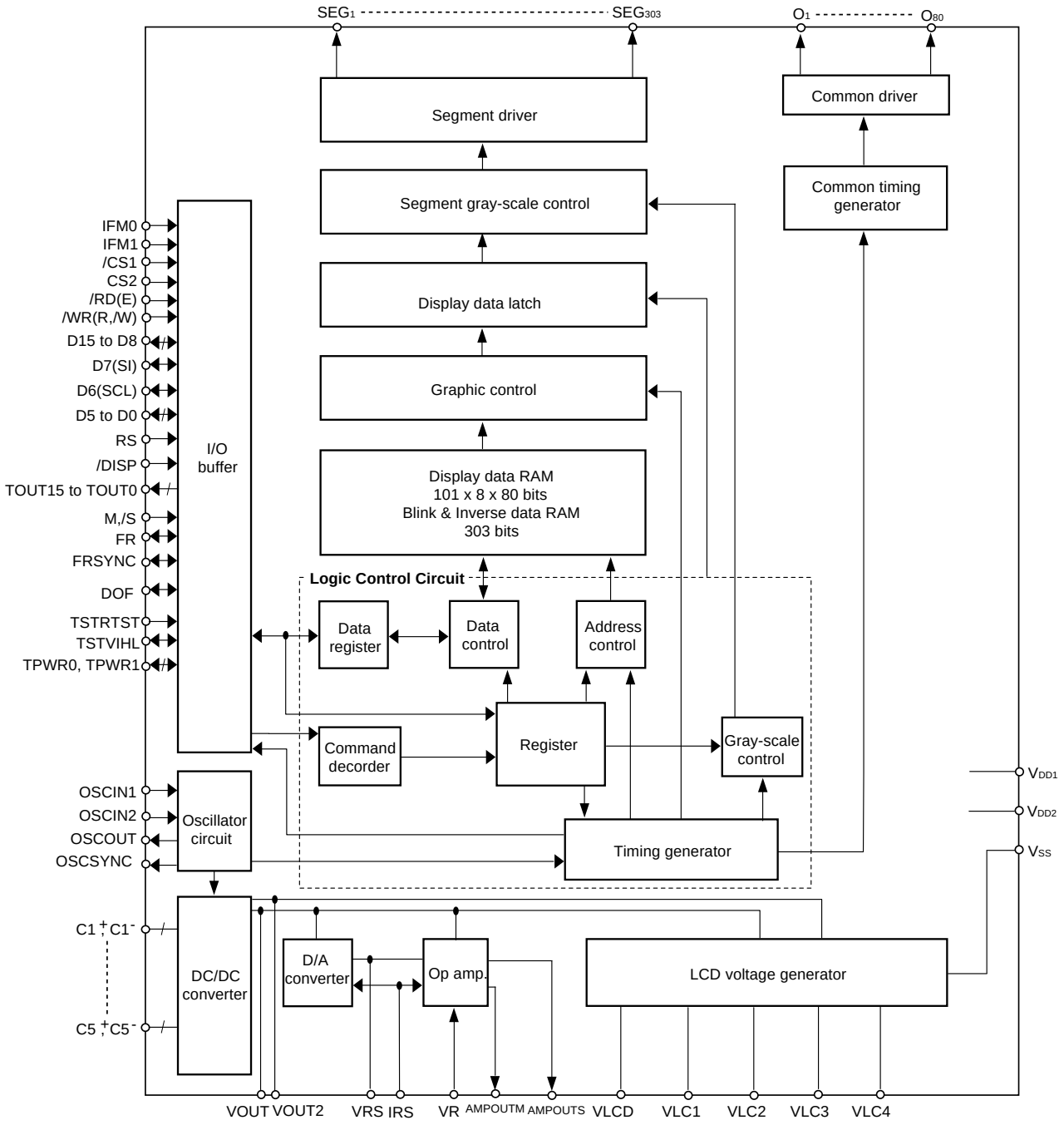
Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

Document No. S15726EJ2V0DS00 (2nd Edition)
Data Published June 2002 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

CONTENT

1. BLOCK DIAGRAM



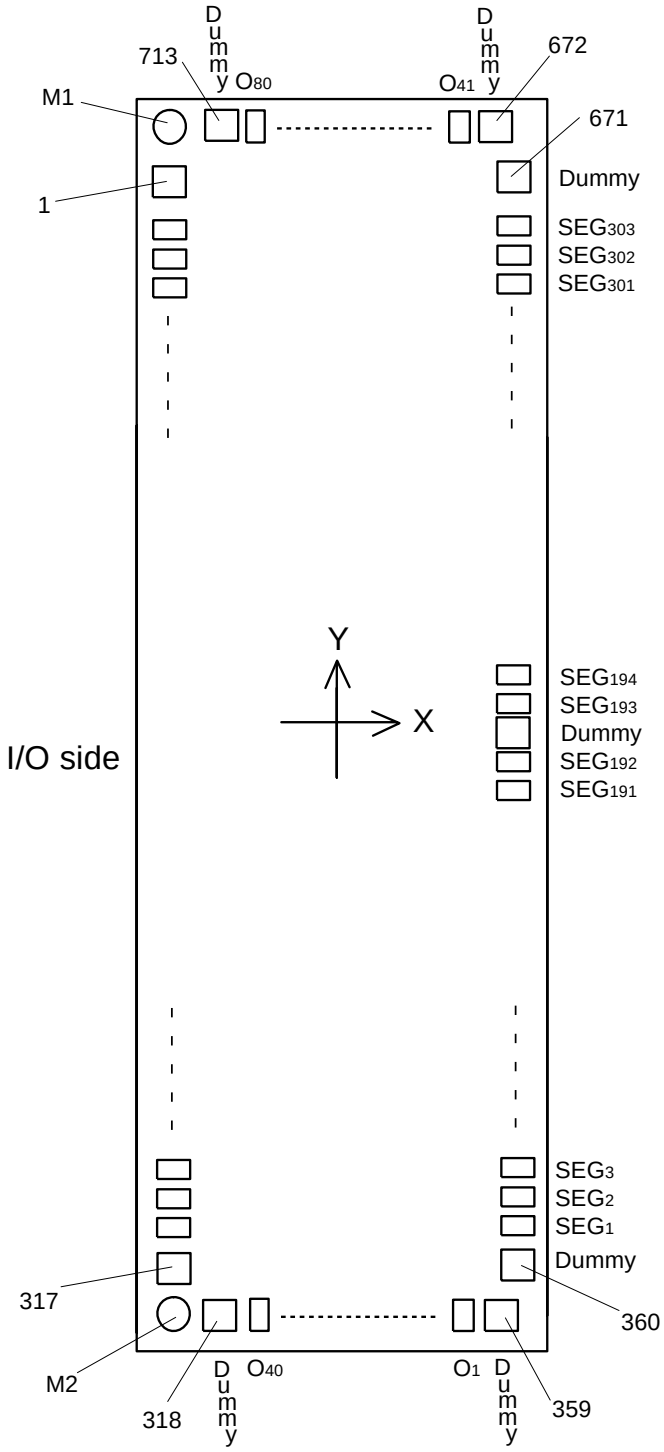
Remark /xxx is an active-low signal.

2. PIN CONFIGURATION (Pad Layout)

- **μPD161401W/P**

Chip size: 2.57 x 16.05 mm^2

Chip thickness: 485 μm (TYP.)



Details of pad and alignment mark

Pad type

A type

Pad size (Al): 39 x 71 μm^2 TYP.

Bump size : 33 x 65 μm^2 TYP.

Bump height: 17 μm TYP.

B type

Pad size (Al): 93 x 71 μm^2 TYP.

Bump size: 87 x 65 μm^2 TYP.

Bump height: 17 μm TYP.

Alignment mark (unit: μm)

	X	Y
M1	−1140.00	7560.00
M2	−1140.00	−7560.00

Shape of mark (unit: μm)

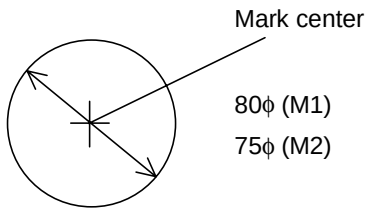


Table 2–1 Pad Layout (1/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Pad Layout [μm] Y
1	DUMMY	B	-1144.50	7230.00
2	VSS	A	-1144.50	7105.00
3	VSS	A	-1144.50	7060.00
4	VSS	A	-1144.50	7015.00
5	VOUT	A	-1144.50	6970.00
6	VOUT	A	-1144.50	6925.00
7	VOUT	A	-1144.50	6880.00
8	VOUT2	A	-1144.50	6835.00
9	VOUT2	A	-1144.50	6790.00
10	VOUT2	A	-1144.50	6745.00
11	VSS	A	-1144.50	6700.00
12	VSS	A	-1144.50	6655.00
13	VSS	A	-1144.50	6610.00
14	C5−	A	-1144.50	6565.00
15	C5−	A	-1144.50	6520.00
16	C5−	A	-1144.50	6475.00
17	C5+	A	-1144.50	6430.00
18	C5+	A	-1144.50	6385.00
19	C5+	A	-1144.50	6340.00
20	C4−	A	-1144.50	6295.00
21	C4−	A	-1144.50	6250.00
22	C4−	A	-1144.50	6205.00
23	C4+	A	-1144.50	6160.00
24	C4+	A	-1144.50	6115.00
25	C4+	A	-1144.50	6070.00
26	C3−	A	-1144.50	6025.00
27	C3−	A	-1144.50	5980.00
28	C3−	A	-1144.50	5935.00
29	C3+	A	-1144.50	5890.00
30	C3+	A	-1144.50	5845.00
31	C3+	A	-1144.50	5800.00
32	C2−	A	-1144.50	5755.00
33	C2−	A	-1144.50	5710.00
34	C2−	A	-1144.50	5665.00
35	C2+	A	-1144.50	5620.00
36	C2+	A	-1144.50	5575.00
37	C2+	A	-1144.50	5530.00
38	C1−	A	-1144.50	5485.00
39	C1−	A	-1144.50	5440.00
40	C1−	A	-1144.50	5395.00
41	C1+	A	-1144.50	5350.00
42	C1+	A	-1144.50	5305.00
43	C1+	A	-1144.50	5260.00
44	VSS	A	-1144.50	5215.00
45	VSS	A	-1144.50	5170.00
46	VSS	A	-1144.50	5125.00
47	TPWR1	A	-1144.50	5080.00
48	TPWR1	A	-1144.50	5035.00
49	TPWR1	A	-1144.50	4990.00
50	TPWR0	A	-1144.50	4945.00
51	TPWR0	A	-1144.50	4900.00
52	TPWR0	A	-1144.50	4855.00
53	VRS	A	-1144.50	4810.00
54	VRS	A	-1144.50	4765.00
55	VRS	A	-1144.50	44720.00
56	VSS	A	-1144.50	4675.00
57	VSS	A	-1144.50	4630.00
58	VSS	A	-1144.50	4585.00
59	VSS	A	-1144.50	4540.00
60	VSS	A	-1144.50	4495.00
61	VSS	A	-1144.50	4450.00
62	VDD2	A	-1144.50	4405.00
63	VDD2	A	-1144.50	4360.00
64	VDD2	A	-1144.50	4315.00
65	VDD1	A	-1144.50	4270.00
66	VDD1	A	-1144.50	4225.00
67	VDD1	A	-1144.50	4180.00
68	VSS	A	-1144.50	4135.00
69	VSS	A	-1144.50	4090.00
70	VSS	A	-1144.50	4045.00
71	VSS	A	-1144.50	4000.00
72	VSS	A	-1144.50	3955.00
73	VSS	A	-1144.50	3910.00
74	M, /S	A	-1144.50	3865.00
75	M, /S	A	-1144.50	3820.00
76	M, /S	A	-1144.50	3775.00
77	VDD1	A	-1144.50	3730.00
78	VDD1	A	-1144.50	3685.00
79	VDD1	A	-1144.50	3640.00
80	IFM0	A	-1144.50	3595.00
81	IFM0	A	-1144.50	3550.00
82	IFM0	A	-1144.50	3505.00
83	VSS	A	-1144.50	3460.00
84	VSS	A	-1144.50	3415.00
85	VSS	A	-1144.50	3370.00
86	IFM1	A	-1144.50	3325.00
87	IFM1	A	-1144.50	3280.00
88	IFM1	A	-1144.50	3235.00
89	VDD1	A	-1144.50	3190.00
90	VDD1	A	-1144.50	3145.00
91	VDD1	A	-1144.50	3100.00
92	IRS	A	-1144.50	3055.00
93	IRS	A	-1144.50	3010.00
94	IRS	A	-1144.50	2965.00
95	VSS	A	-1144.50	2920.00
96	VSS	A	-1144.50	2875.00
97	VSS	A	-1144.50	2830.00
98	/CS1	A	-1144.50	2785.00
99	/CS1	A	-1144.50	2740.00
100	/CS1	A	-1144.50	2695.00
101	CS2	A	-1144.50	2650.00
102	CS2	A	-1144.50	2605.00
103	CS2	A	-1144.50	2560.00
104	VDD1	A	-1144.50	2515.00
105	VDD1	A	-1144.50	2470.00
106	VDD1	A	-1144.50	2425.00
107	/DISP	A	-1144.50	2380.00
108	/DISP	A	-1144.50	2335.00
109	/DISP	A	-1144.50	2290.00
110	RS	A	-1144.50	2245.00
111	RS	A	-1144.50	2200.00
112	RS	A	-1144.50	2155.00
113	VSS	A	-1144.50	2110.00
114	VSS	A	-1144.50	2065.00
115	VSS	A	-1144.50	2020.00
116	/WR (R, /W)	A	-1144.50	1975.00
117	/WR (R, /W)	A	-1144.50	1930.00
118	/WR (R, /W)	A	-1144.50	1885.00
119	/RD (E)	A	-1144.50	1840.00
120	/RD (E)	A	-1144.50	1795.00
121	/RD (E)	A	-1144.50	1750.00
122	VDD1	A	-1144.50	1705.00
123	VDD1	A	-1144.50	1660.00
124	VDD1	A	-1144.50	1615.00
125	D15	A	-1144.50	1570.00
126	D15	A	-1144.50	1525.00
127	D15	A	-1144.50	1480.00
128	D14	A	-1144.50	1435.00
129	D14	A	-1144.50	1390.00
130	D14	A	-1144.50	1345.00
131	D13	A	-1144.50	1300.00
132	D13	A	-1144.50	1255.00
133	D13	A	-1144.50	1210.00
134	VSS	A	-1144.50	1165.00
135	VSS	A	-1144.50	1120.00
136	VSS	A	-1144.50	1075.00
137	D12	A	-1144.50	1030.00
138	D12	A	-1144.50	985.00
139	D12	A	-1144.50	940.00
140	D11	A	-1144.50	895.00
141	D11	A	-1144.50	850.00
142	D11	A	-1144.50	805.00
143	D10	A	-1144.50	760.00
144	D10	A	-1144.50	715.00
145	D10	A	-1144.50	670.00
146	VSS	A	-1144.50	625.00
147	VSS	A	-1144.50	580.00
148	VSS	A	-1144.50	535.00
149	D9	A	-1144.50	490.00
150	D9	A	-1144.50	445.00
151	D9	A	-1144.50	400.00
152	D8	A	-1144.50	355.00
153	D8	A	-1144.50	310.00
154	D8	A	-1144.50	265.00
155	VSS	A	-1144.50	220.00
156	VSS	A	-1144.50	175.00
157	VSS	A	-1144.50	130.00
158	D7	A	-1144.50	85.00
159	D7	A	-1144.50	40.00
160	D7	A	-1144.50	-5.00
161	D6	A	-1144.50	-50.00
162	D6	A	-1144.50	-95.00
163	D6	A	-1144.50	-140.00
164	D5	A	-1144.50	-185.00
165	D5	A	-1144.50	-230.00
166	D5	A	-1144.50	-275.00
167	VSS	A	-1144.50	-320.00
168	VSS	A	-1144.50	-365.00
169	VSS	A	-1144.50	-410.00
170	D4	A	-1144.50	-455.00
171	D4	A	-1144.50	-500.00
172	D4	A	-1144.50	-545.00
173	D3	A	-1144.50	-590.00
174	D3	A	-1144.50	-635.00
175	D3	A	-1144.50	-680.00
176	D2	A	-1144.50	-725.00
177	D2	A	-1144.50	-770.00
178	D2	A	-1144.50	-815.00
179	VSS	A	-1144.50	-860.00
180	VSS	A	-1144.50	-905.00
181	VSS	A	-1144.50	-950.00
182	D1	A	-1144.50	-995.00
183	D1	A	-1144.50	-1040.00
184	D1	A	-1144.50	-1085.00
185	D0	A	-1144.50	-1130.00
186	D0	A	-1144.50	-1175.00
187	D0	A	-1144.50	-1220.00
188	VSS	A	-1144.50	-1265.00
189	VSS	A	-1144.50	-1310.00
190	VSS	A	-1144.50	-1355.00
191	FRSYNC	A	-1144.50	-1400.00
192	FRSYNC	A	-1144.50	-1445.00
193	FRSYNC	A	-1144.50	-1490.00
194	FR	A	-1144.50	-1535.00
195	FR	A	-1144.50	-1580.00
196	FR	A	-1144.50	-1625.00
197	DOF	A	-1144.50	-1670.00
198	DOF	A	-1144.50	-1715.00
199	DOF	A	-1144.50	-1760.00
200	OSCSYNC	A	-1144.50	-1805.00
201	OSCSYNC	A	-1144.50	-1850.00
202	OSCSYNC	A	-1144.50	-1895.00
203	VSS	A	-1144.50	-1940.00
204	VSS	A	-1144.50	-1985.00
205	VSS	A	-1144.50	-2030.00
206	OSCIN1	A	-1144.50	-2075.00
207	OSCIN1	A	-1144.50	-2120.00
208	OSCIN1	A	-1144.50	-2165.00
209	VSS	A	-1144.50	-2210.00
210	VSS	A	-1144.50	-2255.00

Table 2–1 Pad Layout (2/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Pad Layout [μm] Y
211	VSS	A	-1144.50	-2300.00
212	OSCIN2	A	-1144.50	-2345.00
213	OSCIN2	A	-1144.50	-2390.00
214	OSCIN2	A	-1144.50	-2435.00
215	VSS	A	-1144.50	-2480.00
216	VSS	A	-1144.50	-2525.00
217	VSS	A	-1144.50	-2570.00
218	OSCOUT	A	-1144.50	-2615.00
219	OSCOUT	A	-1144.50	-2660.00
220	OSCOUT	A	-1144.50	-2705.00
221	VSS	A	-1144.50	-2750.00
222	VSS	A	-1144.50	-2795.00
223	VSS	A	-1144.50	-2840.00
224	TSTRTST	A	-1144.50	-2885.00
225	TSTRTST	A	-1144.50	-2930.00
226	TSTRTST	A	-1144.50	-2975.00
227	TSTVIHL	A	-1144.50	-3020.00
228	TSTVIHL	A	-1144.50	-3065.00
229	TSTVIHL	A	-1144.50	-3110.00
230	TOUT15	A	-1144.50	-3155.00
231	TOUT15	A	-1144.50	-3200.00
232	TOUT15	A	-1144.50	-3245.00
233	TOUT14	A	-1144.50	-3290.00
234	TOUT14	A	-1144.50	-3335.00
235	TOUT14	A	-1144.50	-3380.00
236	TOUT13	A	-1144.50	-3425.00
237	TOUT13	A	-1144.50	-3470.00
238	TOUT13	A	-1144.50	-3515.00
239	TOUT12	A	-1144.50	-3560.00
240	TOUT12	A	-1144.50	-3605.00
241	TOUT12	A	-1144.50	-3650.00
242	TOUT11	A	-1144.50	-3695.00
243	TOUT11	A	-1144.50	-3740.00
244	TOUT11	A	-1144.50	-3785.00
245	TOUT10	A	-1144.50	-3830.00
246	TOUT10	A	-1144.50	-3875.00
247	TOUT10	A	-1144.50	-3920.00
248	TOUT9	A	-1144.50	-3965.00
249	TOUT9	A	-1144.50	-4010.00
250	TOUT9	A	-1144.50	-4055.00
251	TOUT8	A	-1144.50	-4100.00
252	TOUT8	A	-1144.50	-4145.00
253	TOUT8	A	-1144.50	-4190.00
254	TOUT7	A	-1144.50	-4235.00
255	TOUT7	A	-1144.50	-4280.00
256	TOUT7	A	-1144.50	-4325.00
257	TOUT6	A	-1144.50	-4370.00
258	TOUT6	A	-1144.50	-4415.00
259	TOUT6	A	-1144.50	-4460.00
260	TOUT5	A	-1144.50	-4505.00
261	TOUT5	A	-1144.50	-4550.00
262	TOUT5	A	-1144.50	-4595.00
263	TOUT4	A	-1144.50	-4640.00
264	TOUT4	A	-1144.50	-4685.00
265	TOUT4	A	-1144.50	-4730.00
266	TOUT3	A	-1144.50	-4775.00
267	TOUT3	A	-1144.50	-4820.00
268	TOUT3	A	-1144.50	-4865.00
269	TOUT2	A	-1144.50	-4910.00
270	TOUT2	A	-1144.50	-4955.00
271	TOUT2	A	-1144.50	-5000.00
272	TOUT1	A	-1144.50	-5045.00
273	TOUT1	A	-1144.50	-5090.00
274	TOUT1	A	-1144.50	-5135.00
275	TOUT0	A	-1144.50	-5180.00
276	TOUT0	A	-1144.50	-5225.00
277	TOUT0	A	-1144.50	-5270.00
278	VSS	A	-1144.50	-5315.00
279	VSS	A	-1144.50	-5360.00
280	VSS	A	-1144.50	-5405.00
281	VSS	A	-1144.50	-5450.00
282	VSS	A	-1144.50	-5495.00
283	VSS	A	-1144.50	-5540.00
284	VSS	A	-1144.50	-5585.00
285	VSS	A	-1144.50	-5630.00
286	VSS	A	-1144.50	-5675.00
287	VR	A	-1144.50	-5720.00
288	VR	A	-1144.50	-5765.00
289	VR	A	-1144.50	-5810.00
290	AMPOUTM	A	-1144.50	-5855.00
291	AMPOUTM	A	-1144.50	-5900.00
292	AMPOUTM	A	-1144.50	-5945.00
293	VSS	A	-1144.50	-5990.00
294	VSS	A	-1144.50	-6035.00
295	VSS	A	-1144.50	-6080.00
296	AMPOUTS	A	-1144.50	-6125.00
297	AMPOUTS	A	-1144.50	-6170.00
298	AMPOUTS	A	-1144.50	-6215.00
299	VSS	A	-1144.50	-6260.00
300	VSS	A	-1144.50	-6305.00
301	VSS	A	-1144.50	-6350.00
302	VLCD	A	-1144.50	-6395.00
303	VLCD	A	-1144.50	-6440.00
304	VLCD	A	-1144.50	-6485.00
305	VLC1	A	-1144.50	-6530.00
306	VLC1	A	-1144.50	-6575.00
307	VLC1	A	-1144.50	-6620.00
308	VLC2	A	-1144.50	-6665.00
309	VLC2	A	-1144.50	-6710.00
310	VLC2	A	-1144.50	-6755.00
311	VLC3	A	-1144.50	-6800.00
312	VLC3	A	-1144.50	-6845.00
313	VLC3	A	-1144.50	-6890.00
314	VLC4	A	-1144.50	-6935.00
315	VLC4	A	-1144.50	-6980.00
316	VLC4	A	-1144.50	-7025.00
317	DUMMY	B	-1144.50	-7150.00
318	DUMMY	B	-1060.00	-7773.00
319	O40	A	-935.00	-7773.00
320	O39	A	-890.00	-7773.00
321	O38	A	-845.00	-7773.00
322	O37	A	-800.00	-7773.00
323	O36	A	-755.00	-7773.00
324	O35	A	-710.00	-7773.00
325	O34	A	-665.00	-7773.00
326	O33	A	-620.00	-7773.00
327	O32	A	-575.00	-7773.00
328	O31	A	-530.00	-7773.00
329	O30	A	-485.00	-7773.00
330	O29	A	-440.00	-7773.00
331	O28	A	-395.00	-7773.00
332	O27	A	-350.00	-7773.00
333	O26	A	-305.00	-7773.00
334	O25	A	-260.00	-7773.00
335	O24	A	-215.00	-7773.00
336	O23	A	-170.00	-7773.00
337	O22	A	-125.00	-7773.00
338	O21	A	-80.00	-7773.00
339	O20	A	-35.00	-7773.00
340	O19	A	10.00	-7773.00
341	O18	A	55.00	-7773.00
342	O17	A	100.00	-7773.00
343	O16	A	145.00	-7773.00
344	O15	A	190.00	-7773.00
345	O14	A	235.00	-7773.00
346	O13	A	280.00	-7773.00
347	O12	A	325.00	-7773.00
348	O11	A	370.00	-7773.00
349	O10	A	415.00	-7773.00
350	O9	A	460.00	-7773.00
351	O8	A	505.00	-7773.00
352	O7	A	550.00	-7773.00
353	O6	A	595.00	-7773.00
354	O5	A	640.00	-7773.00
355	O4	A	685.00	-7773.00
356	O3	A	730.00	-7773.00
357	O2	A	775.00	-7773.00
358	O1	A	820.00	-7773.00
359	DUMMY	B	945.00	-7773.00
360	DUMMY	B	1033.00	-7080.00
361	SEG1	A	1033.00	-6955.00
362	SEG2	A	1033.00	-6910.00
363	SEG3	A	1033.00	-6865.00
364	SEG4	A	1033.00	-6820.00
365	SEG5	A	1033.00	-6775.00
366	SEG6	A	1033.00	-6730.00
367	SEG7	A	1033.00	-6685.00
368	SEG8	A	1033.00	-6640.00
369	SEG9	A	1033.00	-6595.00
370	SEG10	A	1033.00	-6550.00
371	SEG11	A	1033.00	-6505.00
372	SEG12	A	1033.00	-6460.00
373	SEG13	A	1033.00	-6415.00
374	SEG14	A	1033.00	-6370.00
375	SEG15	A	1033.00	-6325.00
376	SEG16	A	1033.00	-6280.00
377	SEG17	A	1033.00	-6235.00
378	SEG18	A	1033.00	-6190.00
379	SEG19	A	1033.00	-6145.00
380	SEG20	A	1033.00	-6100.00
381	SEG21	A	1033.00	-6055.00
382	SEG22	A	1033.00	-6010.00
383	SEG23	A	1033.00	-5965.00
384	SEG24	A	1033.00	-5920.00
385	SEG25	A	1033.00	-5875.00
386	SEG26	A	1033.00	-5830.00
387	SEG27	A	1033.00	-5785.00
388	SEG28	A	1033.00	-5740.00
389	SEG29	A	1033.00	-5695.00
390	SEG30	A	1033.00	-5650.00
391	SEG31	A	1033.00	-5605.00
392	SEG32	A	1033.00	-5560.00
393	SEG33	A	1033.00	-5515.00
394	SEG34	A	1033.00	-5470.00
395	SEG35	A	1033.00	-5425.00
396	SEG36	A	1033.00	-5380.00
397	SEG37	A	1033.00	-5335.00
398	SEG38	A	1033.00	-5290.00
399	SEG39	A	1033.00	-5245.00
400	SEG40	A	1033.00	-5200.00
401	SEG41	A	1033.00	-5155.00
402	SEG42	A	1033.00	-5110.00
403	SEG43	A	1033.00	-5065.00
404	SEG44	A	1033.00	-5020.00
405	SEG45	A	1033.00	-4975.00
406	SEG46	A	1033.00	-4930.00
407	SEG47	A	1033.00	-4885.00
408	SEG48	A	1033.00	-4840.00
409	SEG49	A	1033.00	-4795.00
410	SEG50	A	1033.00	-4750.00
411	SEG51	A	1033.00	-4705.00
412	SEG52	A	1033.00	-4660.00
413	SEG53	A	1033.00	-4615.00
414	SEG54	A	1033.00	-4570.00
415	SEG55	A	1033.00	-4525.00
416	SEG56	A	1033.00	-4480.00
417	SEG57	A	1033.00	-4435.00
418	SEG58	A	1033.00	-4390.00
419	SEG59	A	1033.00	-4345.00
420	SEG60	A	1033.00	-4300.00

Table 2–1 Pad Layout (3/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Y
421	SEG61	A	1033.00	-4255.00
422	SEG62	A	1033.00	-4210.00
423	SEG63	A	1033.00	-4165.00
424	SEG64	A	1033.00	-4120.00
425	SEG65	A	1033.00	-4075.00
426	SEG66	A	1033.00	-4030.00
427	SEG67	A	1033.00	-3985.00
428	SEG68	A	1033.00	-3940.00
429	SEG69	A	1033.00	-3895.00
430	SEG70	A	1033.00	-3850.00
431	SEG71	A	1033.00	-3805.00
432	SEG72	A	1033.00	-3760.00
433	SEG73	A	1033.00	-3715.00
434	SEG74	A	1033.00	-3670.00
435	SEG75	A	1033.00	-3625.00
436	SEG76	A	1033.00	-3580.00
437	SEG77	A	1033.00	-3535.00
438	SEG78	A	1033.00	-3490.00
439	SEG79	A	1033.00	-3445.00
440	SEG80	A	1033.00	-3400.00
441	SEG81	A	1033.00	-3355.00
442	SEG82	A	1033.00	-3310.00
443	SEG83	A	1033.00	-3265.00
444	SEG84	A	1033.00	-3220.00
445	SEG85	A	1033.00	-3175.00
446	SEG86	A	1033.00	-3130.00
447	SEG87	A	1033.00	-3085.00
448	SEG88	A	1033.00	-3040.00
449	SEG89	A	1033.00	-2995.00
450	SEG90	A	1033.00	-2950.00
451	SEG91	A	1033.00	-2905.00
452	SEG92	A	1033.00	-2860.00
453	SEG93	A	1033.00	-2815.00
454	SEG94	A	1033.00	-2770.00
455	SEG95	A	1033.00	-2725.00
456	SEG96	A	1033.00	-2680.00
457	SEG97	A	1033.00	-2635.00
458	SEG98	A	1033.00	-2590.00
459	SEG99	A	1033.00	-2545.00
460	SEG100	A	1033.00	-2500.00
461	SEG101	A	1033.00	-2455.00
462	SEG102	A	1033.00	-2410.00
463	SEG103	A	1033.00	-2365.00
464	SEG104	A	1033.00	-2320.00
465	SEG105	A	1033.00	-2275.00
466	SEG106	A	1033.00	-2230.00
467	SEG107	A	1033.00	-2185.00
468	SEG108	A	1033.00	-2140.00
469	SEG109	A	1033.00	-2095.00
470	SEG110	A	1033.00	-2050.00
471	SEG111	A	1033.00	-2005.00
472	SEG112	A	1033.00	-1960.00
473	SEG113	A	1033.00	-1915.00
474	SEG114	A	1033.00	-1870.00
475	SEG115	A	1033.00	-1825.00
476	SEG116	A	1033.00	-1780.00
477	SEG117	A	1033.00	-1735.00
478	SEG118	A	1033.00	-1690.00
479	SEG119	A	1033.00	-1645.00
480	SEG120	A	1033.00	-1600.00
481	SEG121	A	1033.00	-1555.00
482	SEG122	A	1033.00	-1510.00
483	SEG123	A	1033.00	-1465.00
484	SEG124	A	1033.00	-1420.00
485	SEG125	A	1033.00	-1375.00
486	SEG126	A	1033.00	-1330.00
487	SEG127	A	1033.00	1285.00
488	SEG128	A	1033.00	-1240.00
489	SEG129	A	1033.00	-1195.00
490	SEG130	A	1033.00	-1150.00
491	SEG131	A	1033.00	-1105.00
492	SEG132	A	1033.00	-1060.00
493	SEG133	A	1033.00	-1015.00
494	SEG134	A	1033.00	-970.00
495	SEG135	A	1033.00	-925.00
496	SEG136	A	1033.00	-880.00
497	SEG137	A	1033.00	-835.00
498	SEG138	A	1033.00	-790.00
499	SEG139	A	1033.00	-745.00
500	SEG140	A	1033.00	-700.00
501	SEG141	A	1033.00	-655.00
502	SEG142	A	1033.00	-610.00
503	SEG143	A	1033.00	-565.00
504	SEG144	A	1033.00	-520.00
505	SEG145	A	1033.00	-475.00
506	SEG146	A	1033.00	-430.00
507	SEG147	A	1033.00	-385.00
508	SEG148	A	1033.00	-340.00
509	SEG149	A	1033.00	-295.00
510	SEG150	A	1033.00	-250.00
511	SEG151	A	1033.00	-205.00
512	SEG152	A	1033.00	-160.00
513	SEG153	A	1033.00	-115.00
514	SEG154	A	1033.00	-70.00
515	SEG155	A	1033.00	-25.00
516	SEG156	A	1033.00	20.00
517	SEG157	A	1033.00	65.00
518	SEG158	A	1033.00	110.00
519	SEG159	A	1033.00	155.00
520	SEG160	A	1033.00	200.00
521	SEG161	A	1033.00	245.00
522	SEG162	A	1033.00	290.00
523	SEG163	A	1033.00	335.00
524	SEG164	A	1033.00	380.00
525	SEG165	A	1033.00	425.00
526	SEG166	A	1033.00	470.00
527	SEG167	A	1033.00	515.00
528	SEG168	A	1033.00	560.00
529	SEG169	A	1033.00	605.00
530	SEG170	A	1033.00	650.00
531	SEG171	A	1033.00	695.00
532	SEG172	A	1033.00	740.00
533	SEG173	A	1033.00	785.00
534	SEG174	A	1033.00	830.00
535	SEG175	A	1033.00	875.00
536	SEG176	A	1033.00	920.00
537	SEG177	A	1033.00	965.00
538	SEG178	A	1033.00	1010.00
539	SEG179	A	1033.00	1055.00
540	SEG180	A	1033.00	1100.00
541	SEG181	A	1033.00	1145.00
542	SEG182	A	1033.00	1190.00
543	SEG183	A	1033.00	1235.00
544	SEG184	A	1033.00	1280.00
545	SEG185	A	1033.00	1325.00
546	SEG186	A	1033.00	1370.00
547	SEG187	A	1033.00	1415.00
548	SEG188	A	1033.00	1460.00
549	SEG189	A	1033.00	1505.00
550	SEG190	A	1033.00	1550.00
551	SEG191	A	1033.00	1595.00
552	SEG192	A	1033.00	1640.00
553	DUMMY	A	1033.00	1685.00
554	DUMMY	A	1033.00	1730.00
555	DUMMY	A	1033.00	1775.00
556	DUMMY	A	1033.00	1820.00
557	DUMMY	A	1033.00	1865.00
558	DUMMY	A	1033.00	1910.00
559	DUMMY	A	1033.00	1955.00
560	SEG193	A	1033.00	2000.00
561	SEG194	A	1033.00	2045.00
562	SEG195	A	1033.00	2090.00
563	SEG196	A	1033.00	2135.00
564	SEG197	A	1033.00	2180.00
565	SEG198	A	1033.00	2225.00
566	SEG199	A	1033.00	2270.00
567	SEG200	A	1033.00	2315.00
568	SEG201	A	1033.00	2360.00
569	SEG202	A	1033.00	2405.00
570	SEG203	A	1033.00	2450.00
571	SEG204	A	1033.00	2495.00
572	SEG205	A	1033.00	2540.00
573	SEG206	A	1033.00	2585.00
574	SEG207	A	1033.00	2630.00
575	SEG208	A	1033.00	2675.00
576	SEG209	A	1033.00	2720.00
577	SEG210	A	1033.00	2765.00
578	SEG211	A	1033.00	2810.00
579	SEG212	A	1033.00	2855.00
580	SEG213	A	1033.00	2900.00
581	SEG214	A	1033.00	2945.00
582	SEG215	A	1033.00	2990.00
583	SEG216	A	1033.00	3035.00
584	SEG217	A	1033.00	3080.00
585	SEG218	A	1033.00	3125.00
586	SEG219	A	1033.00	3170.00
587	SEG220	A	1033.00	3215.00
588	SEG221	A	1033.00	3260.00
589	SEG222	A	1033.00	3305.00
590	SEG223	A	1033.00	3350.00
591	SEG224	A	1033.00	3395.00
592	SEG225	A	1033.00	3440.00
593	SEG226	A	1033.00	3485.00
594	SEG227	A	1033.00	3530.00
595	SEG228	A	1033.00	3575.00
596	SEG229	A	1033.00	3620.00
597	SEG230	A	1033.00	3665.00
598	SEG231	A	1033.00	3710.00
599	SEG232	A	1033.00	3755.00
600	SEG233	A	1033.00	3800.00
601	SEG234	A	1033.00	3845.00
602	SEG235	A	1033.00	3890.00
603	SEG236	A	1033.00	3935.00
604	SEG237	A	1033.00	3980.00
605	SEG238	A	1033.00	4025.00
606	SEG239	A	1033.00	4070.00
607	SEG240	A	1033.00	4115.00
608	SEG241	A	1033.00	4160.00
609	SEG242	A	1033.00	4205.00
610	SEG243	A	1033.00	4250.00
611	SEG244	A	1033.00	4295.00
612	SEG245	A	1033.00	4340.00
613	SEG246	A	1033.00	4385.00
614	SEG247	A	1033.00	4430.00
615	SEG248	A	1033.00	4475.00
616	SEG249	A	1033.00	4520.00
617	SEG250	A	1033.00	4565.00
618	SEG251	A	1033.00	4610.00
619	SEG252	A	1033.00	4655.00
620	SEG253	A	1033.00	4700.00
621	SEG254	A	1033.00	4745.00
622	SEG255	A	1033.00	4790.00
623	SEG256	A	1033.00	4835.00
624	SEG257	A	1033.00	4880.00
625	SEG258	A	1033.00	4925.00
626	SEG259	A	1033.00	4970.00
627	SEG260	A	1033.00	5015.00
628	SEG261	A	1033.00	5060.00
629	SEG262	A	1033.00	5105.00
630	SEG263	A	1033.00	5150.00

Table 2–1 Pad Layout (4/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Pad Layout [μm] Y
631	SEG264	A	1033.00	5195.00
632	SEG265	A	1033.00	5240.00
633	SEG266	A	1033.00	5285.00
634	SEG267	A	1033.00	5330.00
635	SEG268	A	1033.00	5375.00
636	SEG269	A	1033.00	5420.00
637	SEG270	A	1033.00	5465.00
638	SEG271	A	1033.00	5510.00
639	SEG272	A	1033.00	5555.00
640	SEG273	A	1033.00	5600.00
641	SEG274	A	1033.00	5645.00
642	SEG275	A	1033.00	5690.00
643	SEG276	A	1033.00	5735.00
644	SEG277	A	1033.00	5780.00
645	SEG278	A	1033.00	5825.00
646	SEG279	A	1033.00	5870.00
647	SEG280	A	1033.00	5915.00
648	SEG281	A	1033.00	5960.00
649	SEG282	A	1033.00	6005.00
650	SEG283	A	1033.00	6050.00
651	SEG284	A	1033.00	6095.00
652	SEG285	A	1033.00	6140.00
653	SEG286	A	1033.00	6185.00
654	SEG287	A	1033.00	6230.00
655	SEG288	A	1033.00	6275.00
656	SEG289	A	1033.00	6320.00
657	SEG290	A	1033.00	6365.00
658	SEG291	A	1033.00	6410.00
659	SEG292	A	1033.00	6455.00
660	SEG293	A	1033.00	6500.00
661	SEG294	A	1033.00	6545.00
662	SEG295	A	1033.00	6590.00
663	SEG296	A	1033.00	6635.00
664	SEG297	A	1033.00	6680.00
665	SEG298	A	1033.00	6725.00
666	SEG299	A	1033.00	6770.00
667	SEG300	A	1033.00	6815.00
668	SEG301	A	1033.00	6860.00
669	SEG302	A	1033.00	6905.00
670	SEG303	A	1033.00	6950.00
671	DUMMY	A	1033.00	7075.00
672	DUMMY	A	950.00	7773.00
673	O41	A	825.00	7773.00
674	O42	A	780.00	7773.00
675	O43	A	735.00	7773.00
676	O44	A	690.00	7773.00
677	O45	A	645.00	7773.00
678	O46	A	600.00	7773.00
679	O47	A	555.00	7773.00
680	O48	A	510.00	7773.00
681	O49	A	465.00	7773.00
682	O50	A	420.00	7773.00
683	O51	A	375.00	7773.00
684	O52	A	330.00	7773.00
685	O53	A	285.00	7773.00
686	O54	A	240.00	7773.00
687	O55	A	195.00	7773.00
688	O56	A	150.00	7773.00
689	O57	A	105.00	7773.00
690	O58	A	60.00	7773.00
691	O59	A	15.00	7773.00
692	O60	A	-30.00	7773.00
693	O61	A	-75.00	7773.00
694	O62	A	-120.00	7773.00
695	O63	A	-165.00	7773.00
696	O64	A	-210.00	7773.00
697	O65	A	-255.00	7773.00
698	O66	A	-300.00	7773.00
699	O67	A	-345.00	7773.00
700	O68	A	-390.00	7773.00
701	O69	A	-435.00	7773.00
702	O70	A	-480.00	7773.00
703	O71	A	-525.00	7773.00
704	O72	A	-570.00	7773.00
705	O73	A	-615.00	7773.00
706	O74	A	-660.00	7773.00
707	O75	A	-705.00	7773.00
708	O76	A	-750.00	7773.00
709	O77	A	-795.00	7773.00
710	O78	A	-840.00	7773.00
711	O79	A	-885.00	7773.00
712	O80	A	-930.00	7773.00
713	DUMMY	B	-1055.00	7773.00

3. PIN FUNCTIONS

3.1 Power Supply Pins

Symbol	Pin Name	Pin No.	I/O	Description
V_{DD1}	Logic power supply	65 to 67, 77 to 79, 89 to 91,104 to 106, 122 to 124	–	Supplies power to the logic circuit.
V_{DD2}	Booster circuit power supply	62 to 64	–	Supplies power to the booster circuit.
V_{SS}	Logic and driver ground pin	2 to 4, 11 to 13, 44 to 46, 56 to 61, 68 to 73, 83 to 85, 95 to 97, 113 to 115, 134 to 136, 146 to 148, 155 to 157, 167 to 169, 179 to 181, 188 to 190, 203 to 205, 209 to 211, 215 to 217, 221 to 223, 278 to 286, 293 to 295, 299 to 301	–	Ground pin for the logic and driver circuits.
V_{OUT}, V_{OUT2}	Driver power supply	5 to 7, 8 to 10	–	Supply power to the driver (output pins of the internal booster circuit). Connect a 1 μF capacitor between GND and these pins. When the internal booster circuit is not used, the driver power can be directly input to the V_{OUT} pin. At this time, leave V_{OUT2} open.
V_{LCD}, V_{LC1} to V_{LC4}	Driver reference power supply	302 to 304, 305 to 316	–	Supply the reference power for driving the LCD. Connect a capacitor between GND and these pins when an internal bias is selected.
C_1^+, C_1^- C_2^+, C_2^- C_3^+, C_3^- C_4^+, C_4^- C_5^+, C_5^-	Booster capacitor connection pin	43 to 14	–	These pins are used to connect capacitors for the internal booster circuit. Connect a 1 μF capacitor between the corresponding (+) and (–) pins.

3.2 Logic Circuit Pins (1/3)

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>/CS1,
CS2</td><td>Chip select</td><td>98 to 100,
101 to 103</td><td>Input</td><td>These pins are chip select signal pins.
When /CS1 = L (CS2 = H), the chip is active, and data/command can be input or output and I/O manipulated.</td></tr>
<tr><td>/RD (E)</td><td>Read (enable)</td><td>119 to 121</td><td>Input</td><td>When i80 system parallel data transfer is selected (/RD), read is enabled by this signal. When this pin is L, data is output to the data bus. When M68 system parallel data transfer is selected (E), this pin inputs an enable signal that triggers data write or read.
But in the μPD161401, the data of the display access memory register, the complementary color blink data memory register, the specified color blink data memory register and the reverse data memory access register (R12, R41, R45, R50) cannot be read.</td></tr>
<tr><td>/WR (R,/W)</td><td>Write (read/write)</td><td>116 to 118</td><td>Input</td><td>When i80 system parallel data transfer is selected (/WR), write is enabled by this signal. Data is written at the rising edge of this signal. When M68 system parallel data transfer is selected (R, /W), this pin determines the data transfer direction, as follows:
0: Write
1: Read</td></tr>
<tr><td>IFM0,
IFM1</td><td>Interface selection</td><td>86 to 88,
80 to 82</td><td>Input</td><td>Selects an interface mode
<table>
<tr><th>IFM1</th><th>IFM0</th><th>Interface Mode</th></tr>
<tr><td>L</td><td>L</td><td>Serial</td></tr>
<tr><td>L</td><td>H</td><td>Setting prohibited</td></tr>
<tr><td>H</td><td>L</td><td>i80 series parallel</td></tr>
<tr><td>H</td><td>H</td><td>M68 series parallel</td></tr>
</table></td></tr>
<tr><td>D_0 to D_{15}
(SI)
(SCL)</td><td>Data bus
(serial input)
(serial clock)</td><td>187 to 182,
178 to 170,
166 to 158,
154 to 149,
145 to 137,
133 to 125</td><td>I/O</td><td>This is a bi-directional data bus connected to an 8- or 16-bit standard CPU bus.
When the serial interface mode is selected (IFM1, IFM0 = L, L), D_7 functions as a serial data input pin (SI), and D_6 serves as a serial clock input pin (SCL). At this time, D_0 to D_5 and D_8 to D_{15} go into a high-impedance state.
When the 8-bit data bus is selected, only D_0 to D_7 are used, and D_8 to D_{15} go into a high-impedance state. Data is input starting from its higher byte, followed by the lower byte. If the chip is not selected, all D_0 to D_{15} go into a high-impedance state.</td></tr>
<tr><td>RS</td><td>Index register/data command selection</td><td>110 to 112</td><td>Input</td><td>This pin is usually connected to the least significant bit of a standard CPU address bus to identify whether data is an index register or data/command.
RS = H: Indicates that D_0 to D_{15} are data/command.
RS = L: Indicates that D_0 to D_{15} are an index register.</td></tr>
</table>

(2/3)

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>/DISP</td><td>Reset</td><td>107 to 109</td><td>Input</td><td>Making /DISP low initializes the DISP flag in the control register 1 (R0) and turns OFF the display. When the serial interface is used, the write counter is also initialized. Making /DISP high enables writing. To light the display after it has been turned OFF by this pin, make /DISP high and set the DISP flag to 1.</td></tr>
<tr><td>FR</td><td>Frame signal</td><td>194 to 196</td><td>I/O</td><td>This pin inputs or outputs a liquid crystal AC signal.
M,/S = H : Output
M,/S = L : Input
When two or more μPD161401s are used in master/slave mode, the respective FR pins must be connected to each other.</td></tr>
<tr><td>FR_{SYNC}</td><td>Frame sync signal</td><td>191 to 193</td><td>I/O</td><td>This pin inputs or outputs a liquid crystal AC sync signal.
M,/S = H : Output
M,/S = L : Input
When two or more μPD161401s are used in master/slave mode, the respective FR_{SYNC} pins must be connected to each other.</td></tr>
<tr><td>DOF</td><td>Display blink</td><td>197 to 199</td><td>I/O</td><td>This pin controls blinking of the LCD.
M,/S = H : Output
M,/S = L : Input
When two or more μPD161401s are used in master/slave mode, the respective DOF pins must be connected to each other.</td></tr>
<tr><td>M,/S</td><td>Master/slave</td><td>74 to 76</td><td>Input</td><td>This pin selects master or slave mode. In the master mode, it outputs a timing signal necessary for driving the LCD. In the slave mode, this timing signal is input from an external source to synchronize the LCD. M,/S = H : Master mode
M,/S = L : Slave mode
The status of each pin, including this pin, and the power circuit is as follows depending on the status of the M,/S pin.
<table>
<tr><th>M,/S</th><th>Power Circuit</th><th>FR</th><th>FR_{SYNC}</th><th>DOF</th></tr>
<tr><td>H</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td></tr>
<tr><td>IRS</td><td>V_{LCD} adjustment</td><td>92 to 94</td><td>Input</td><td>This pin selects the resistor used to adjust the V_{LCD} voltage level.
IRS = H: The internal resistor is used.
IRS = L: The internal resistor is not used.
The V_{LCD} voltage level is adjusted by an external voltage divider resistor connected to the V_R pin.
This pin is enabled only when the master operation mode is selected. If the slave mode is selected, this pin is fixed to H or L.</td></tr>
</table>

(3/3)

Symbol	Pin Name	Pin No.	I/O	Description
OSC_{IN1}	Oscillation signal pin	206 to 208	Input	These pins are connected with a resistor inserted between OSC_{IN1} and OSC_{OUT}, and between OSC_{IN2} and OSC_{OUT}. When an external oscillator is used, input a clock signal to the OSC_{IN} pin and leave the OSC_{OUT} pin open.
OSC_{IN2}		212 to 214	Input	
OSC_{OUT}		218 to 220	Output	
OSC_{SYNC}	Display clock output	200 to 202	Output	This pin outputs a clock for display. When using the μPD161401 in the master or slave mode, refer to **5.4 Oscillator**.
T_{OUT0} to T_{OUT15}	Test output	230 to 277	Output	These pins are used when the μPD161401 is in the test mode. Usually, leave these pins open.
TSTRTST, TSTVIHL	Test input pin	224 to 226, 227 to 229	Input	These pins are used to set the μPD161401 in the test mode. Usually, connect these pins to V_{SS}.
$TPWR_0$, $TPWR_1$	Test input/output pin	50 to 52, 47 to 49	I/O	These pins are used to input/output test signals when the μPD161401 is in the test mode. Usually, leave these pins open.

3.3 Driver Pins

Symbol	Pin Name	Pin No.	I/O	Description
SEG_1 to SEG_{303}	Segment	361 to 670	Output	These pins output segment signals.
O_1 to O_{80}	Common	319 to 358, 673 to 712	Output	These pins output common signals.
V_{RS}	Operational amplifier input	53 to 55	Input	These are the input pins of the operational amplifier that adjusts the LCD driving voltage. V_{RS} is used to input the reference voltage of the amplifier for LCD voltage adjustment. V_R is used to connect a feedback resistor for the operational amplifier. The feedback resistor is connected between this pin and GND, AMP_{OUTM}, or AMP_{OUTS}. This pin is enabled only when the internal divider resistor for V_{LCD} voltage adjustment is not used (IRS = L). When the internal divider resistor is used (IRS = H), this pin is not used.
V_R		287 to 289		
AMP_{OUTM}	Operational amplifier output	290 to 292	Output	These pins are the output pins of the operational amplifier that adjusts the LCD driving voltage. The signals output by these pins are connected to the LCD driving voltage adjuster resistor (refer to **5.6.3 Voltage regulator circuit**) only when the internal resistor for LCD voltage adjustment is not used (IRS = L). It is recommended to connect a capacitor of 0.01 to 0.1 μF to these pins to stabilize the output of the internal operational amplifier.
AMP_{OUTS}		296 to 298		
DUMMY	Dummy pin	1, 317, 318, 359, 360, 553 to 559, 671, 672, 713	–	These pins are not connected to the internal circuit.

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit type of each pin and recommended connection of unused pins are shown in the table below.

Symbol	Input Type	I/O	Recommended of Unused Pins	Note
/CS1	Schmitt-trigger A	Input	Connect this pin to V_{SS}.	–
CS2	Schmitt-trigger A	Input	Connect this pin to V_{DD1}.	–
/RD(E)	Schmitt-trigger A	Input	Connect to V_{DD1} (i80 system interface), or to V_{DD1} or V_{SS} (serial interface).	–
/WR(R,/W)	Schmitt-trigger A	Input	Connect to V_{DD1} or V_{SS} (serial interface).	–
IFM1, IFM0	Schmitt-trigger A	Input	Mode setting pin	1
D_0 to D_5	Schmitt-trigger B	I/O	Leave open.	–
D_6(SCL)	Schmitt-trigger B	I/O	–	–
D_7(SI)	Schmitt-trigger B	I/O	–	–
D_8 to D_{15}	Schmitt-trigger B	I/O	Leave open.	–
RS	Schmitt-trigger A	Input	Register setting pin	2
/DISP	Schmitt-trigger C	Input	Connect to V_{DD1}.	–
FR	Schmitt-trigger A	I/O	Leave open (in master mode, M,/S = H).	–
FR_{SYNC}	Schmitt-trigger A	I/O	Leave open (in master mode, M,/S = H).	–
DOF	Schmitt-trigger A	I/O	Leave open (in master mode, M,/S = H).	–
M,/S	Schmitt-trigger A	Input	Mode setting pin	1
IRS	Schmitt-trigger A	Input	Mode setting pin	1
OSC_{IN1}	Schmitt-trigger A	Input	Connect to V_{DD1} or V_{SS}.	–
OSC_{IN2}	Schmitt-trigger A	Input	Connect to V_{DD1} or V_{SS}.	–
OSC_{OUT}	–	Output	Leave open (when an external clock is used).	–
OSC_{SYNC}	–	Output	Leave open.	–
T_{OUT0} to T_{OUT15}	–	Output	Leave open.	–
TSTRTST	Schmitt-trigger A	Input	Connect this pin to V_{SS} (in normal operation mode).	–
TSTVIHL	Schmitt-trigger A	Input	Connect this pin to V_{SS} (in normal operation mode).	–
TPWR	–	I/O	Leave open.	–

Notes 1. Connect this pin to V_{DD1} or V_{SS} depending on the mode selected.

2. Input V_{DD1} or V_{SS} output from the CPU to this pin depending on the mode selected.

Remark Schmitt-trigger A : Schmitt inverter

Schmitt-trigger B : Schmitt NAND

Schmitt-trigger C : Schmitt inverter (with delay circuit)

5. FUNCTIONAL DESCRIPTION

5.1 CPU Interface

5.1.1 Selecting interface type

The μPD161401 transfers data through an 8-bit bi-directional data bus (D_7 to D_0), a 16-bit bi-directional data bus (D_{15} to D_0), or a serial data input (SI) pin. Interface type can be selected by making the IFM1,IFM0 pin high or low, as shown in the following table.

IFM1	IFM0	Interface type
L	L	Serial data input
L	H	Setting Prohibited
H	L	i80 system CPU
H	H	M68 system CPU

Parallel data input or serial data input can be chosen as by setting the polarity of IFM1 terminal, as shown in the following table.

IFM1	/CS1, CS2	RS	/RD	/WR	D_{15} to D_8	D_7	D_6	D_5 to D_0
H: Parallel input	/CS1, CS2	RS	/RD	/WR	D_{15} to D_8	D_7	D_6	D_5 to D_0
L: Serial input	/CS1, CS2	RS	**Note1**	**Note1**	Hi-Z**Note2**	SI	SCL	Hi-Z**Note2**

Notes 1. Fix these pins to the high or low level.

2. Hi-Z: High impedance

5.1.2 Parallel interface

When the parallel interface is selected (IFM = H), an 8-bit bi-directional data bus (D_7 to D_0) or 16-bit bi-directional data bus (D_{15} to D_0) can be selected by setting the BMOD flag of the control register 2 (R1) to 1 or 0. In addition, the μPD161401 can be directly connected to an i80 or M68 system by making the IFM0 pin high or low as shown in the following table.

IFM0	/CS1, CS2	RS	/RD	/WR	BMOD	D_{15} to D_8	D_7 to D_0
H: M68 system CPU	/CS1, CS2	RS	E	R,/W	0	D_{15} to D_8	D_7 to D_0
					1	Hi-Z**Note**	D_7 to D_0
L: i80 system CPU	/CS1, CS2	RS	/RD	/WR	0	D_{15} to D_8	D_7 to D_0
					1	Hi-Z**Note**	D_7 to D_0

Note Hi-Z : High impedance (may be open)

The data bus signals are identified by the combination of the RS, /RD(E), /WR (R,/W) signals as shown in the following table.

Common	M68		i80		Common	Data Bus		Function
RS	R,/W	E	/RD	/WR	BMOD	D_{15} to D_8	D_7 to D_0	
1	1	1	0	1	0	Note1	Note1	Reads the register.
					1	Hi-Z	OUT	
1	0	1	1	0	0	Note2	IN	Writes the display data/register.
					1	Hi-Z	IN	
0	1	1	0	1	0	Hi-Z	OUT	Prohibited
					1	Hi-Z	OUT	
0	0	1	1	0	0	Hi-Z	IN	Writes the control index register.
					1	Hi-Z	IN	
0/1	Other					Hi-Z	Hi-Z	–

Remark IN : Input status (cannot be open), OUT : Output status, Hi-Z : High impedance (may be open)

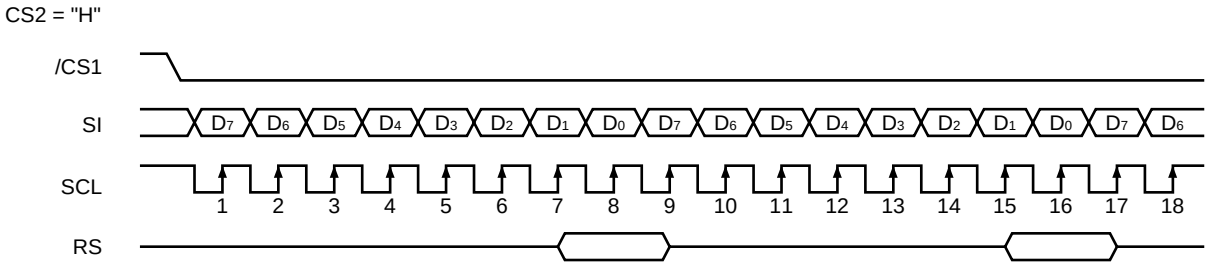
Notes1. In the μPD161401, the data of the display access memory register, the complementary color blink data memory register, the specified color blink data memory register and the reverse data memory access register (R12, R41, R45, R50) are read-prohibited. However, if R12 is selected, the data bus signals D_{15} to D_0 enter an output state. If another register is specified, the D_{15} to D_8 signals become Hi-Z and the D_7 to D_0 signals enter an output state.

2. Only the display access memory register (R12) enters the input state. If another register is specified, the D_{15} to D_8 signals become Hi-Z.

5.1.3 Serial interface

When the serial interface has been selected (IFM1, IFM0 = L, L), as long as the chip is in an active state (/CS1= L, CS2 = H), serial data input (SI) and serial clock input (SCL) can be received. Serial data is read in the order of D_7, then D_6 to D_0 at the rising edge of the serial clock input from the serial input pin. This data is converted to parallel data in synchronization with the 8th rising edge of the serial clock. Serial input data is judged as display data/command data if RS = H and an index if RS = L. The RS input is read every 8th rising edge of the serial clock after the chip becomes active and is used for data discrimination.

Figure 5–1. Serial Interface Signal Chart



Remarks 1. If the chip is not in an active state, the shift register and counter are reset to their initial statuses.

2. The serial clock counter is reset by initialization from the /DISP pin.

3. Data cannot be read when using serial interface mode.

4. Care must be taken when performing SCL wiring to avoid effects from terminal radiation or external noise caused by the wiring length. It is recommended to confirm operation using the actual equipment to be used.

5.1.4 Chip select

The μPD161401 has chip select pins (/CS1 and CS2). The CPU parallel interface or Serial interface can be used only when /CS1 = L (CS2 = H).

If the chip select pins are not active, the D_0 to D_{15} pins go into a high-impedance state, and the RS, /RD, and /WR pins do not become active.

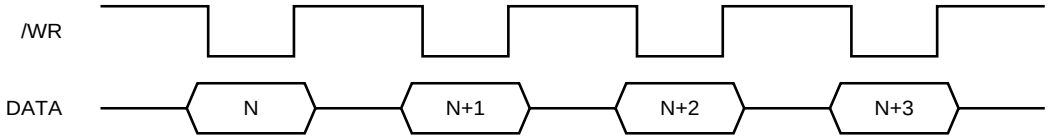
5.1.5 Accessing display data RAM and internal registers

When the CPU accesses the μPD161401, the CPU only has to satisfy the requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take wait time into consideration.

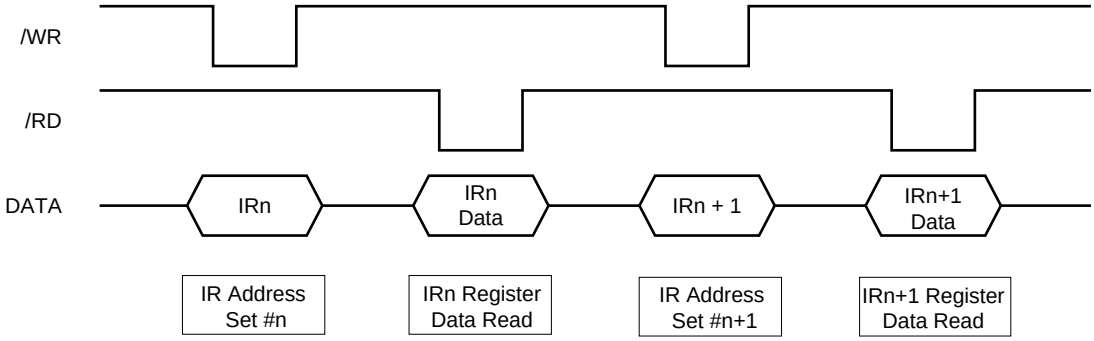
When the CPU writes data to the μPD161401, no dummy data is necessary. When reading data, dummy data is not necessary either. In the μPD161401, the data of the display access memory register, the complementary color blink data memory register, the specified color blink data memory register and the reverse data memory access register (R12, R41, R45, R50) cannot be read. **Figure 5–2** illustrates as follows.

Figure 5–2. Writing and Reading

Writing



Reading (other than display memory access register)



Caution Display access memory register, the complementary color blink data memory register, the specified color blink data memory register and the reverse data memory access register (R12, R41, R45, R50) cannot be read.

5.2 Display Data RAM

5.2.1 Display data RAM

This RAM stores dot data for display and consists of (101 × 80) × 8 bits. Any address of this RAM can be accessed by specifying an X address and a Y address.

Display data D_0 to D_{15} transmitted from the CPU corresponds to the pixels on the LCD (refer to **Table 5–1**). If the μPD161401 is used in a multi-chip configuration, restrictions on display data transfer are relaxed and display setting can be performed relatively freely.

The CPU writes data to the display RAM via I/O buffers. This write operation is performed independently of an operation to read signals for driving the LCD. Therefore, even if the display data RAM is asynchronously accessed, adverse effects such as flickering do not occur or the current LCD screen.

Table 5–1. Display Data RAM

MSB							LSB	MSB							LSB
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot (R)			Dot (G)			Dot (B)		Dot (R)			Dot (G)			Dot (B)	
Pixel 1								Pixel 2							

LCD panel									
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	00H	01H	02H	03H	04H	05H	06H	07H	

5.2.2 X address circuit

An X address of the display data RAM is specified by using the X address register (R4) as shown in **Figure 5–5**. If the X address increment mode (INC = 0: control register 2 (R1)) is used, the specified X address is incremented or decremented by one each time display data is written. Whether the address is incremented or decremented is specified by the XDIR flag of control register 2 (R1) as shown in **Table 5–2**.

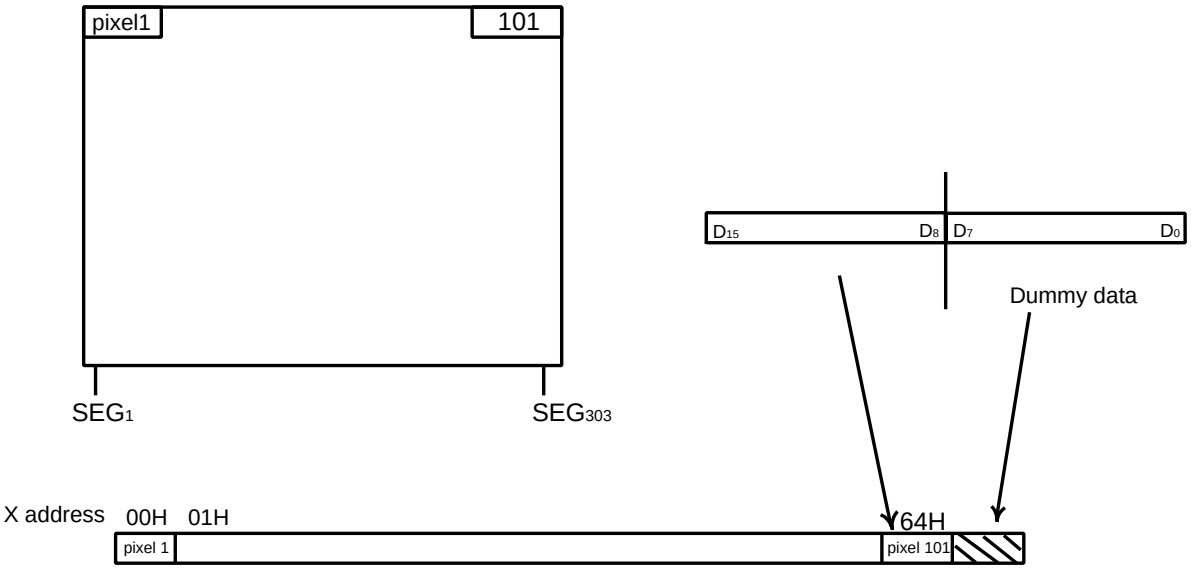
In the increment mode, the X address is incremented up to 64H. If more display data is written, the Y address is incremented (YDIR = 0) or decremented (YDIR = 1), and the X address returns to 00H.

In the decrement mode, the X address is decremented to 00H. If more display data is written, the Y address is incremented (YDIR = 0) or decremented (YDIR = 1), and the X address returns to 64H.

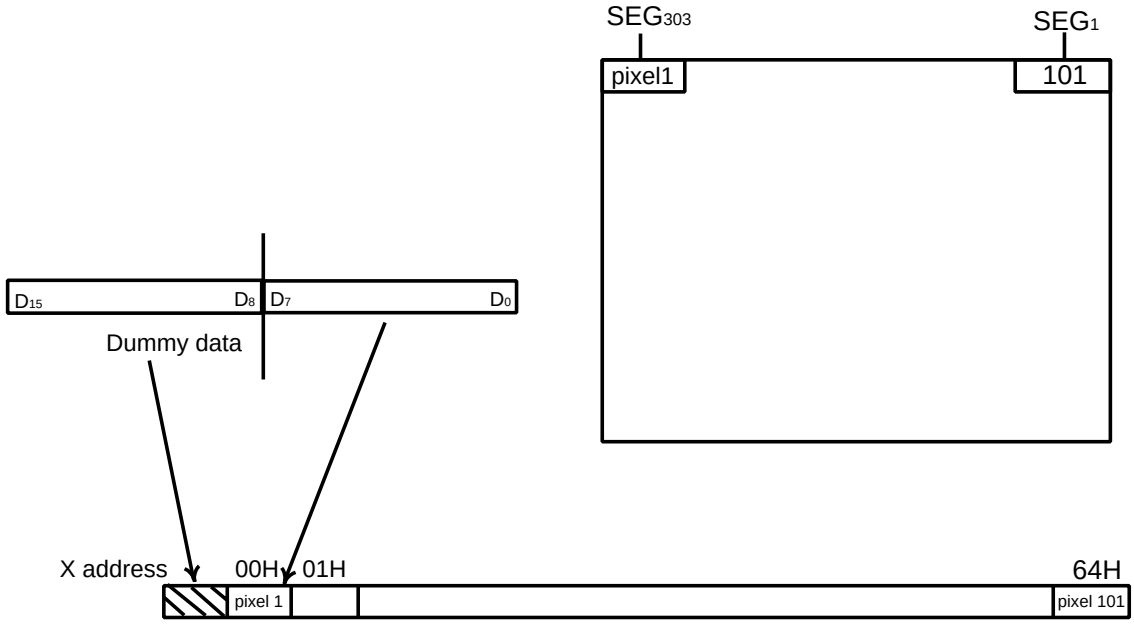
When the 16-bit data bus is selected (BMOD = 0), only an even address can be specified. Moreover, when the 16-bit data bus is selected, dummy data is required as shown in **Figure 5–3**.

Figure 5–3. About Dummy Data Required when the 16-bit Data Bus is Selected

· When an ADC = 0



· When an ADC = 1



5.2.3 Y address circuit

A Y address of the display data RAM is specified by using the Y address register (R5) as shown in **Figure 5–5**. If the Y address increment mode (INC = 1: control register 2 (R1)) is used, the specified Y address is incremented or decremented by one each time display is written. Whether the address is incremented or decremented is specified by the YDIR flag of control register 2 (R1) as shown in **Table 5–2**.

In the increment mode, the Y address is incremented up to 4FH. If more display data is written, the X address is incremented (XDIR = 0) or decremented (XDIR = 1), and the Y address returns to 00H.

In the decrement mode, the Y address is decremented to 00H. If more display data is written, the X address is incremented (XDIR = 0) or decremented (XDIR = 1), and the Y address returns to 4FH.

The relationship between the setting of INC, XDIR, and YDIR of control register 2 (R1) and the address is as follows:

Table 5–2. Relationship between INC, XDIR, and YDIR, and Address

INC	Setting
0	The address is successively incremented or decremented in the X direction when data is accessed.
1	The address is successively incremented or decremented in the Y direction when data is accessed Note.

Note This setting cannot be used when the 16-bit parallel interface is used.

XDIR	Setting
0	Increments the X address (+1) when data is accessed.
1	Decrements the X address (–1) when data is accessed.

YDIR	Setting
0	Increments the Y address (+1) when data is accessed.
1	Decrements the Y address (–1) when data is accessed.

Table 5–3. Combination of INC, XDIR, and YDIR, and Address Direction

INC	XDIR	YDIR	Image of Address Scanning
0	0	0	A-1
	0	1	A-2
	1	0	A-3
	1	1	A-4
1	0	0	B-1
	0	1	B-2
	1	0	B-3
	1	1	B-4

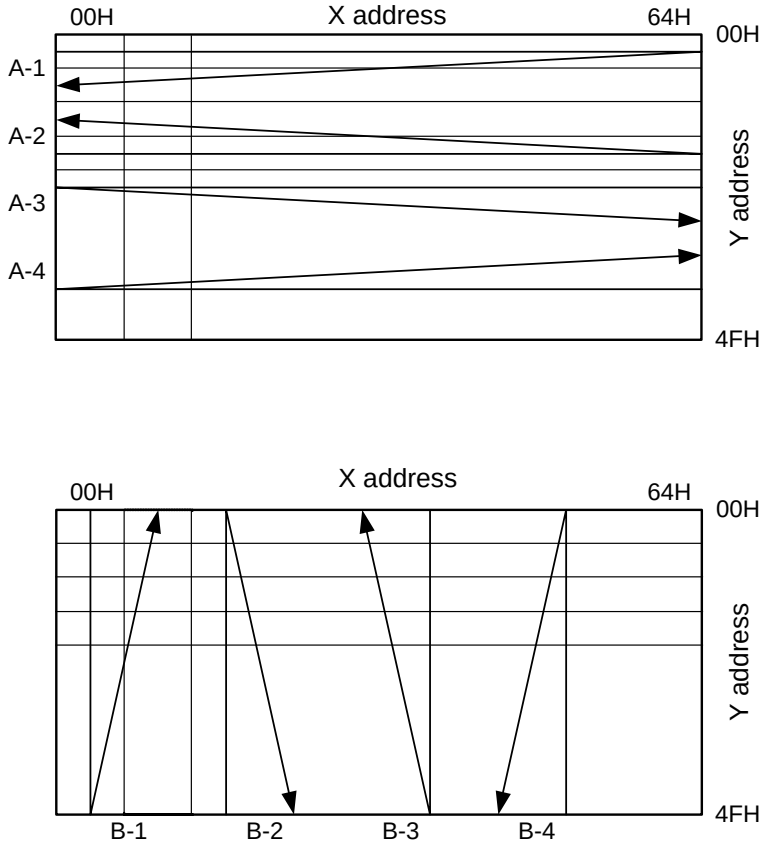
Caution If the access direction is changed by using INC, XDIR, or YDIR, be sure to set the X address register (R4) and Y address register (R5) before accessing the display RAM.

Y address register (R5)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	YA6	YA5	YA4	YA3	YA2	YA1	YA0

YA6 to YA0	Sets a line address.

Figure 5–4. Combination of INC, XDIR, and YDIR, and Address Scanning Image



5.2.4 Column address circuit

When the contents of the display data RAM are displayed, column addresses are output to the SEG output pins as shown in **Figure 5–5**.

The correspondence relationship between the column addresses of the display RAM and segment outputs can be reversed by the ADC flag (segment driver direction select flag) of control register 1 (R0). This reduces the restrictions on chip layout when the LCD module is assembled.

Table 5–4. Relationship between Column Address of Display RAM and Segment Output

SEG Output		SEG_1				SEG_{303}
ADC	0	000H	→	Column address	→	12EH
(D_1)	1	12EH	←	Column address	←	000H

5.2.5 Common scan circuit

The common scan circuit sets the sequence for the scan line of the common signal in which the display RAM is to be read. The RAM line reading direction is set as shown in **Table 5–5** by the COMR flag of control register 1 (R0).

For example, if the duty ratio is 1/64, the number of scroll steps is 0, and COMR = 0, the RAM line reading direction is from 00H to 3FH. If COMR = 1, it is from 3FH to 00H.

Table 5–5. Relationship between Common Scan Circuit and Scan Direction

COMR	0	00H	→	4FH
(D_0)	1	4FH	→	00H

In addition, scanning of the common outputs can be assigned by using the COM scanning address setting register (R21) as shown in **Table 5–6**, so that the scanning can be started from any O_1 to O_{80} output pin. Therefore, the common wiring of the LCD panel can be optimized when any duty ratio is selected.

When COMR = 0, the scan start (COM_1) pin and scan end (COM_a) pin are the On and $O_{(n+a-1)}$ pins, respectively. The value of a is 64, 72, and 80 for 1/64 duty, 1/72 duty, and 1/80 duty, respectively. When COMR = 1, the scan start (COM_1) pin and scan end (COM_a) pin are the $O_{(82-a-n)}$ and $O_{(80-n+1)}$ pins, respectively.

Examples of COM scan address settings for 1/64 duty, 1/72 duty, and 1/80 duty are shown in **Tables 5–5, 5–7**, and **5–8**, respectively.

Table 5–6. COM Scanning Address Setting (1/64 duty)

CSA4	CSA3	CSA2	CSA1	CSA0	n	COMR = 0			COMR = 1		
						the scan start (COM_1) pin	→	the scan end (COM_a)[Note] pin	the scan start (COM_1) pin	→	the scan end (COM_a)[Note] pin
						O_n	→	$O_{(n+a-1)}$ [Note]	$O_{(82-a-n)}$ [Note]	→	$O_{(80-n+1)}$
0	0	0	0	0	1	O_1	→	O_{64}	O_{17}	→	O_{80}
0	0	0	0	1	2	O_2	→	O_{65}	O_{16}	→	O_{79}
0	0	0	1	0	3	O_3	→	O_{66}	O_{15}	→	O_{78}
0	0	0	1	1	4	O_4	→	O_{67}	O_{14}	→	O_{77}
0	0	1	0	0	5	O_5	→	O_{68}	O_{13}	→	O_{76}
0	0	1	0	1	6	O_6	→	O_{69}	O_{12}	→	O_{75}
0	0	1	1	0	7	O_7	→	O_{70}	O_{11}	→	O_{74}
0	0	1	1	1	8	O_8	→	O_{71}	O_{10}	→	O_{73}
0	1	0	0	0	9	O_9	→	O_{72}	O_9	→	O_{72}
0	1	0	0	1	10	O_{10}	→	O_{73}	O_8	→	O_{71}
0	1	0	1	0	11	O_{11}	→	O_{74}	O_7	→	O_{70}
0	1	0	1	1	12	O_{12}	→	O_{75}	O_6	→	O_{69}
0	1	1	0	0	13	O_{13}	→	O_{76}	O_5	→	O_{68}
0	1	1	0	1	14	O_{14}	→	O_{77}	O_4	→	O_{67}
0	1	1	1	0	15	O_{15}	→	O_{78}	O_3	→	O_{66}
0	1	1	1	1	16	O_{16}	→	O_{79}	O_2	→	O_{65}
1	0	0	0	0	17	O_{17}	→	O_{80}	O_1	→	O_{64}

Note When in 1/64 duty, a = 64.

Table 5–7. COM Scanning Address Setting (1/72 duty)

CSA4	CSA3	CSA2	CSA1	CSA0	n	COMR = 0			COMR = 1			Remark
						the scan start (COM_1) pin	→	the scan end (COM_a)[Note] pin	the scan start (COM_1) pin	→	the scan end (COM_a)[Note] pin	
						O_n	→	$O_{(n+a-1)}$ [Note]	$O_{(82-a-n)}$ [Note]	→	$O_{(80-n+1)}$	
0	0	0	0	0	1	O_1	→	O_{72}	O_9	→	O_{80}	
0	0	0	0	1	2	O_2	→	O_{73}	O_8	→	O_{79}	
0	0	0	1	0	3	O_3	→	O_{74}	O_7	→	O_{78}	
0	0	0	1	1	4	O_4	→	O_{75}	O_6	→	O_{77}	
0	0	1	0	0	5	O_5	→	O_{76}	O_5	→	O_{76}	
0	0	1	0	1	6	O_6	→	O_{77}	O_4	→	O_{75}	
0	0	1	1	0	7	O_7	→	O_{78}	O_3	→	O_{74}	
0	0	1	1	1	8	O_8	→	O_{79}	O_2	→	O_{73}	
0	1	0	0	0	9	O_9	→	O_{80}	O_1	→	O_{72}	
0	1	0	0	1	10							Prohibit since here

Note When in 1/72 duty, a = 72

Caution The COM scan address setting register (R21) should be set so that $O_1 \leq$ scan start pin and scan end pin $\leq O_{80}$. If any other settings are made the IC operation is not guaranteed.

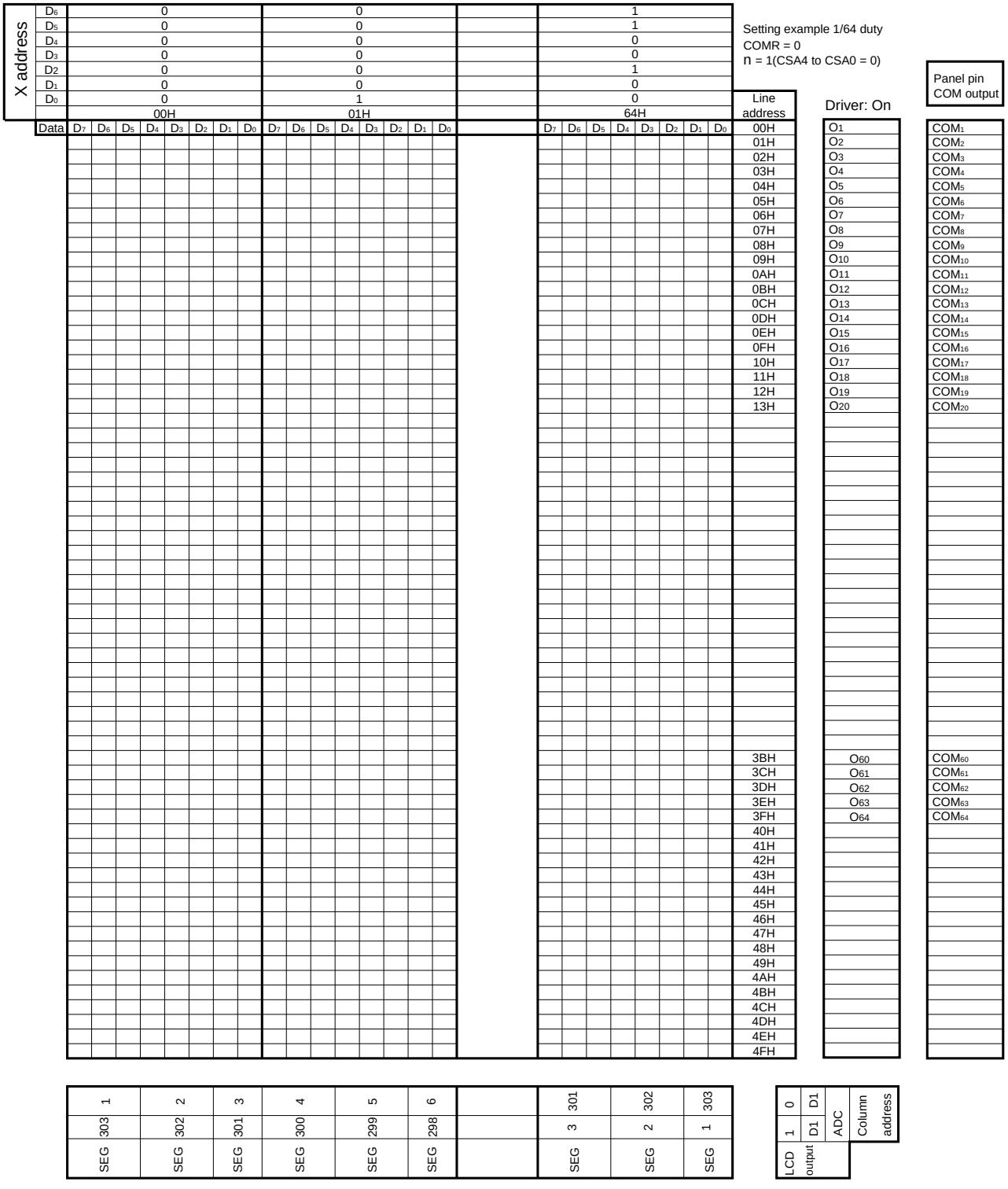
Table 5–8. COM Scanning Address Setting (1/80 duty)

CSA4	CSA3	CSA2	CSA1	CSA0	n	COMR = 0			COMR = 1			Remark
						the scan start (COM_1) pin	→	the scan end (COM_a)[Note] pin	the scan start (COM_1) pin	→	the scan end (COM_a)[Note] pin	
						O_n	→	$O_{(n+a-1)}$ [Note]	$O_{(82-a-n)}$ [Note]	→	$O_{(80-n+1)}$	
0	0	0	0	0	1	O_1	→	O_{80}	O_1	→	O_{80}	
0	0	0	0	1	2							Prohibit since here

Note When in 1/80 duty, a = 80

Caution When this μPD161401 is used in 1/80 duty, the COM scan address setting register (R21) should be set to CSA4, CSA3, CSA2, CSA1, CSA0 = 0, 0, 0, 0, 0. If any other settings are made the IC operation is not guaranteed.

Figure 5–5. Configuration of X Address Register



5.2.6 Display data latch circuit

The display data latch circuit temporarily stores (latches) the display data that is output from the display data RAM to the LCD driver circuit.

The display scan command for forwarding or reversing data and the display ON/OFF command control the latched data and do not affect the data of the display data RAM.

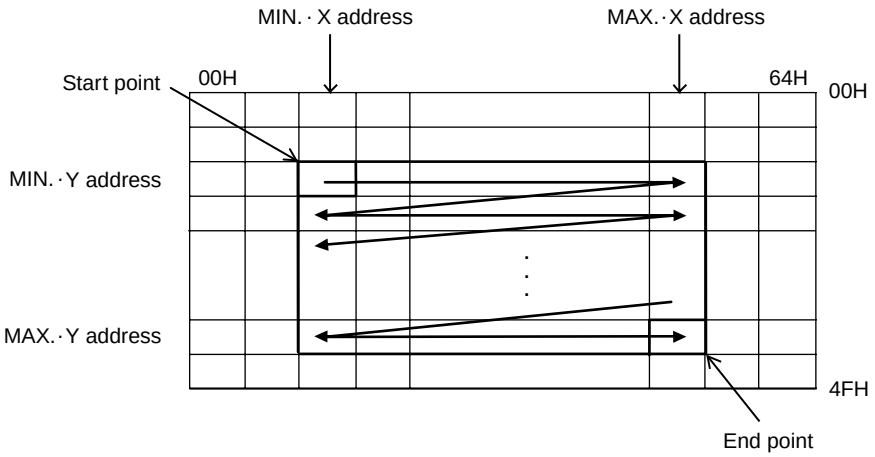
5.2.7 Arbitrary address area access (window access mode (WAS))

With the μPD161401, any area of the display RAM selected by the MIN.·X/Y address registers (R7 and R9) and MAX.·X/Y address registers (R8 and R10) can be accessed.

First, select the area to be accessed by using the MIN.·X/Y address registers and MAX.·X/Y address registers. When WAS of control register 1 is set to 1, the window access mode is then selected. The address scanning setting by INC, XDIR, and YDIR of control register 2 (R1) is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register (R4) and Y address register (R5).

Note that the display RAM must be accessed after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.· X/Y address register (R7, R9) or MAX.· X/Y address register (R8, R10).

Figure 5–6. Example of Incrementing Address When INC = 0, XDIR = 0, and YDIR = 0



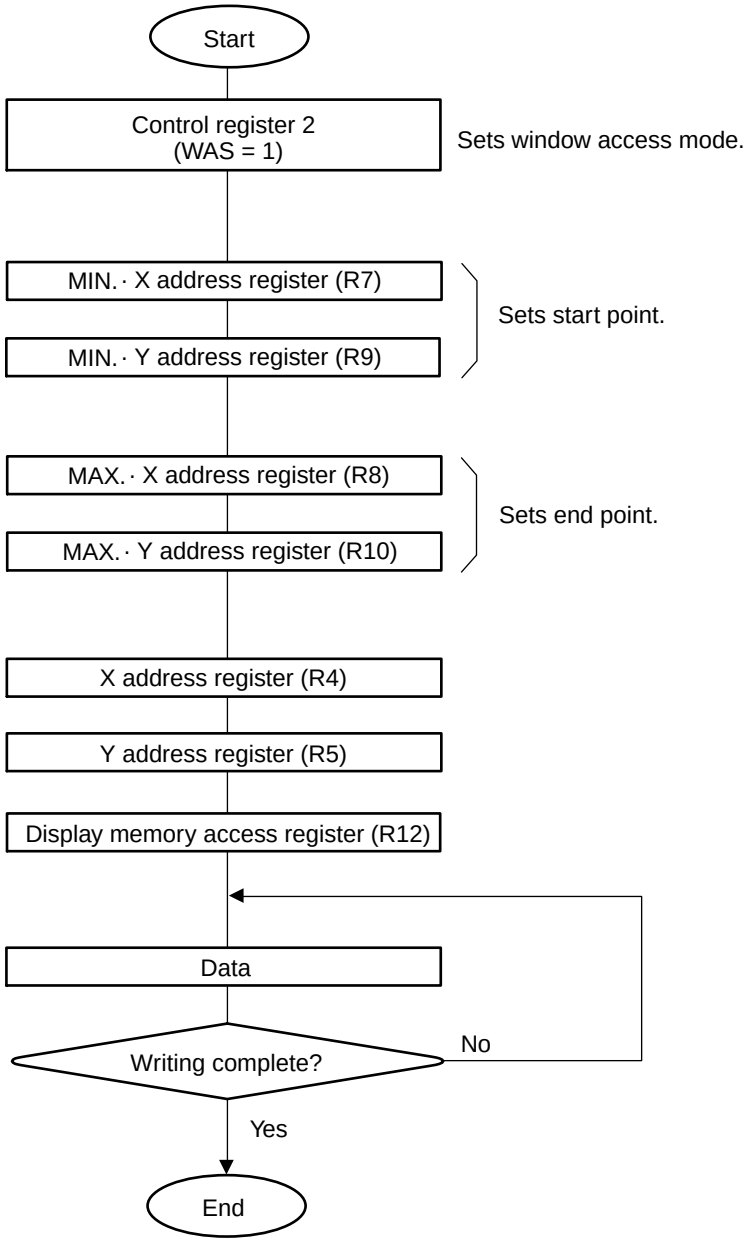
Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

Item	Address Relation Ship
X address	00H ≤ MIN.·X address ≤ X address (R4) ≤ MAX.·X address ≤ 64H
Y address	00H ≤ MIN.·Y address ≤ Y address (R5) ≤ MAX.·Y address ≤ 4FH

2. If invalid address data is set as the MIN./MAX.·address, operation is not guaranteed.

3. Access the display RAM after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.· X/Y address register (R7, R9) or MAX.· X/Y address register (R8, R10).

Figure 5–7. Example of Sequence in Window Access Mode



5.3 Screen Processing

5.3.1 Blink/reverse display circuit

The μPD161401 can blink or reverse a specific area of the full-dot display. Blinking is to turn ON/OFF display repeatedly at about 1 Hz (complementary color or specified color can be selected) and reversing is to reverse the grayscale data on the display.

The area to be blinked is specified by using the complementary color/specified color blink start/end line address registers (R39, R40, R43, and R44), complementary color/specified color blink X address registers (R38, R42), and complementary color/specified color blink data memory registers (R41, R45).

First, select a blink display start line address and end line address by using the start/end line address registers. Next, select the column to be blinked by using the blink X address register and blink data memory register.

The specified color blink is blinked between the graphic data and the color data specified by the specified color setting register (R46).

To select an area to be reversed, use the reverse start/end line address registers (R48, R49), reverse X address register (R47), and reverse data memory access register (R50).

First, select line addresses at which reverse display is started and stopped, by using the reverse start/end line address registers. Next, select a column to be reversed, by using the reverse X address register and reverse data memory access register. The specified blink/reverse X address is incremented by one each time blink/reverse data has been input.

The complementary color/specified color blink RAM and reverse RAM store the data to be blinked and reversed. Each RAM is configured of 101 bits ($12 \times 8 + 5$ bits).

To access a desired bit, specify an X address. Blink/reverse data D_0 to D_7 transmitted from the CPU corresponds to SEG_X on the LCD, as illustrated in **Figure 5–8**.

If the BLD bit and INV bit of the blink/reverse setting register (R37) are set to H after an area and data have been set, blinking or reversing the data is started. **Figure 5–9** shows the relationship between the start line address, end line address, blinking/reversing data, and LCD.

If the same area is specified for complementary color blinking and specified color blinking, the specified color blinking takes precedence.

Table 5–9. Reversing Operation and Display

Original Grayscale	After Reversing (supplement color)
R/G display data	
0, 0, 0	1, 1, 1
0, 0, 1	1, 1, 0
0, 1, 0	1, 0, 1
0, 1, 1	1, 0, 0
1, 0, 0	0, 1, 1
1, 0, 1	0, 1, 0
1, 1, 0	0, 0, 1
1, 1, 1	0, 0, 0
B display data	
0, 0	1, 1
0, 1	1, 0
1, 0	0, 1
1, 1	0, 0

Figure 5–8. Correspondence between Blink/Reverse Data and Segment

When an ADC = 0

R38,R42,R47 X address																								
	D_3	0							0									1						
	D_2	0							0									1						
	D_1	0							0									0						
	D_0	0							1									0						
		00H							01H									0CH						
	Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
															Note	Note	Note								

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F		60	61	62	63	64
pixel1	pixel2	pixel3	pixel4	pixel5	pixel6	pixel7	pixel8	pixel9	pixel10	pixel11	pixel12	pixel13	pixel14	pixel15	pixel16		pixel97	pixel98	pixel99	pixel100	pixel101

Column output → LCD Output

Note The value written in D_2 to D_0 of X address 0CH is invalid.

When an ADC = 1

R38,R42,R47 X address																								
	D_3	0							0									1						
	D_2	0							0									1						
	D_1	0							0									0						
	D_0	0							1									0						
		00H							01H									0CH						
	Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F		60	61	62	63	64
pixel1	pixel2	pixel3	pixel4	pixel5	pixel6	pixel7	pixel8	pixel9	pixel10	pixel11	pixel12	pixel13	pixel14	pixel15	pixel16		pixel97	pixel98	pixel99	pixel100	pixel101

Column output → LCD Output

Note The value written in D_7 to D_5 of X address 00H is invalid.

Figure 5–9. Blink/Reverse Display Area Setting Image

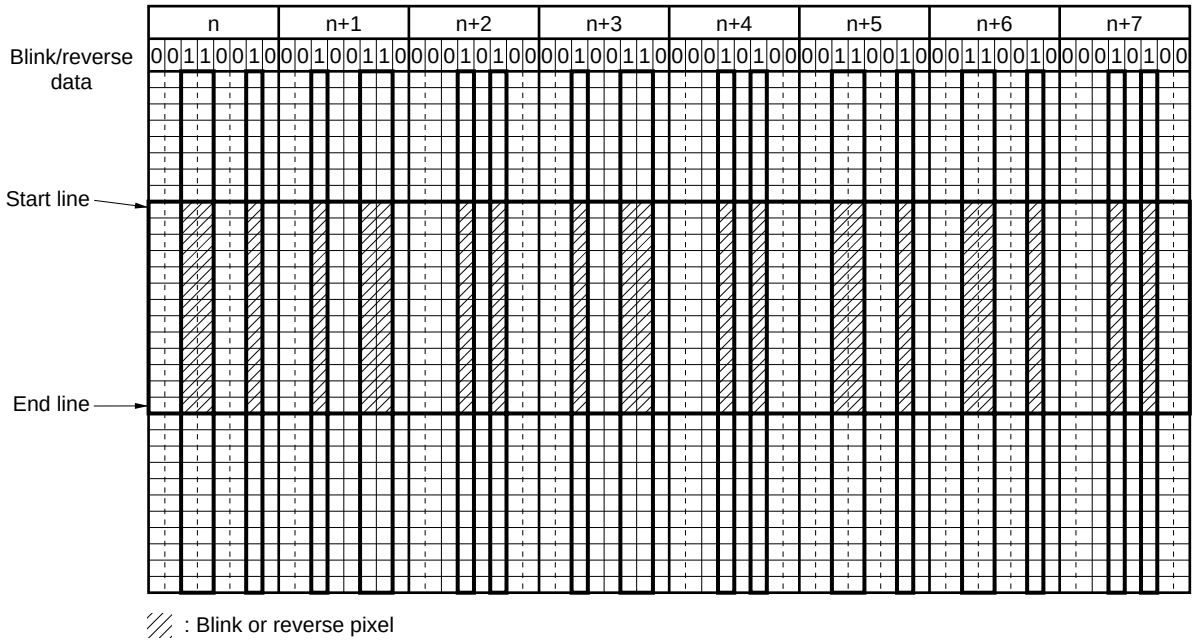
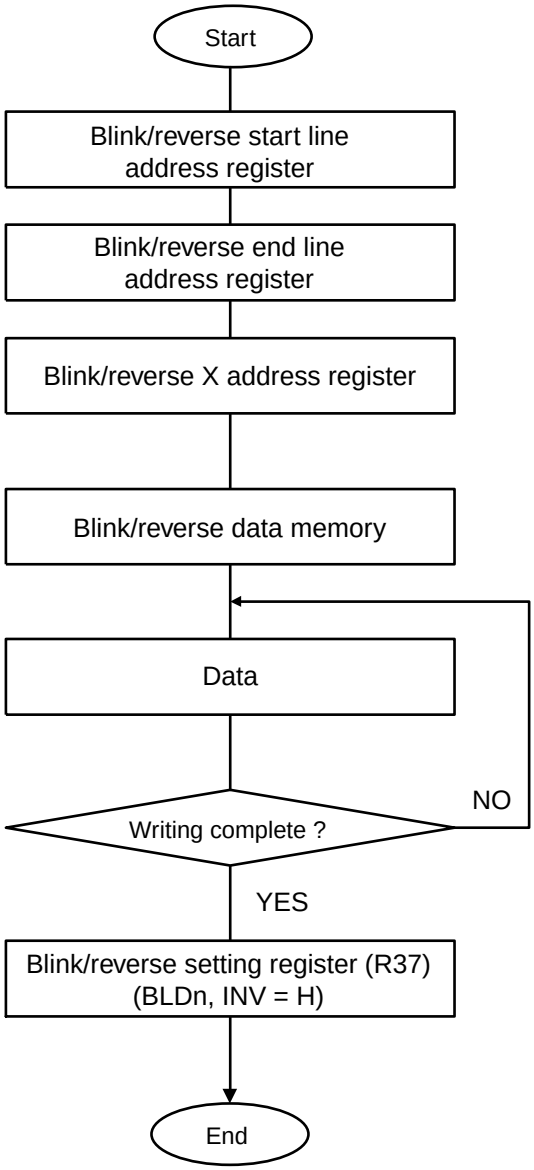


Figure 5–10. Example of Sequence of Setting Blink/Reverse Display



The data configuration of the range specification registers (start/end line address registers R39, R40, R43, R44, R48, and R49) of each line is in the format shown below. Each display area is set in this format. .

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	X_6	X_5	X_4	X_3	X_2	X_1	X_0

X_6 to X_0	Sets start/end line addresses.

Remark X_: CBS, CBE, SBS, SBE, IVS, IVE

5.3.2 Example of setting blink area

This section explains how to specify an area to be blinked, taking complementary color blinking as an example. The same setting is also applied to specified color blinking and reverse display.

(1) Example of using 1 chip at duty ratio of 1/80

T.B.D.

Remark T.B.D. (To be determined.)

(2) Example of using 2 chip (Master and slave) at duty ratio of 1/80

T.B.D.

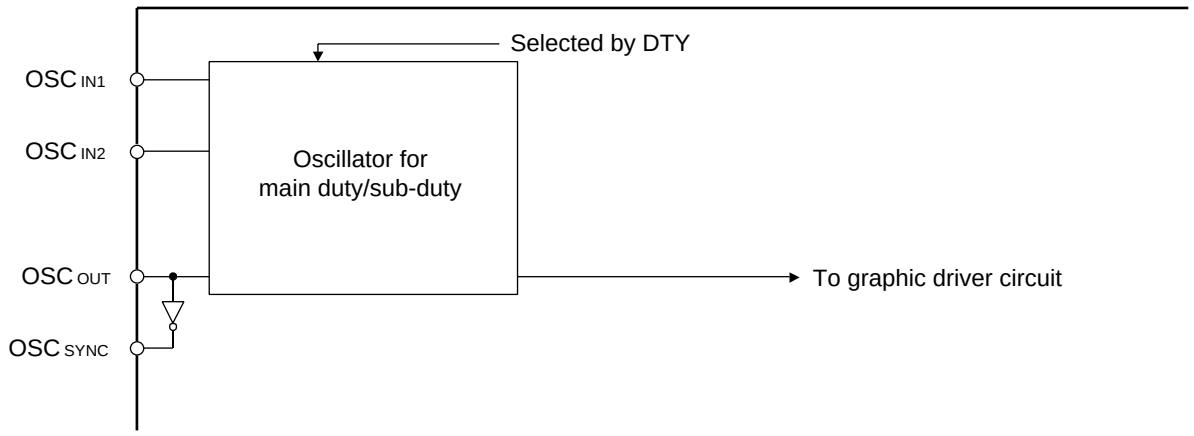
5.4 Oscillator

The μPD161401 has a CR oscillator (with external R) for main duty/sub-duty display. This oscillator generates the display clock.

This oscillator is controlled by the DTY flag of control register 2 (R1), and the configuration of its display clock can be set in accordance with the system used.

The function of each circuit of the oscillator is shown below. The main duty display/sub-duty display oscillator becomes valid only when oscillation resistors (RM and RS) are connected to it. The clock for main duty display or sub-duty display can be selected depending on the status of the DTY flag of control register 2 (R1).

Figure 5–11. Oscillator Block



The relationship between the frame frequency (f_{FRAME}) in the normal display mode, oscillation frequency (f_{OSCINn}), and set duty frame is as follows.

$$f_{FRAME} = f_{OSCINn} \div 16 \div N$$

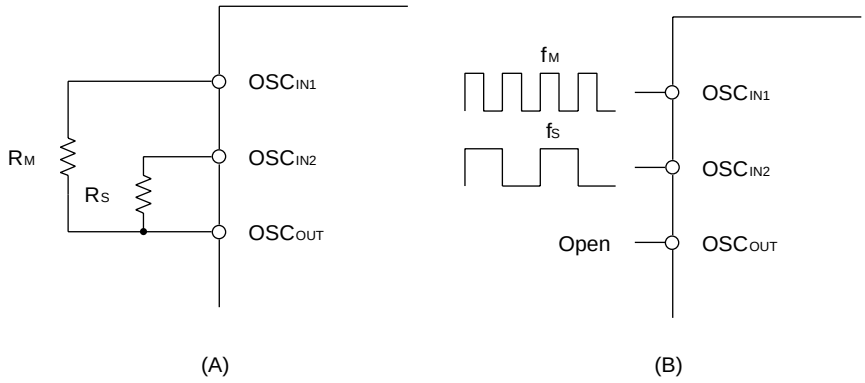
N = Duty ratio

Table 5–10 shows the relationship between oscillation resistors RM and RS, and the display clock circuit.

Table 5–10. Relationship between Display Clock Circuit, Pins, and Resistor

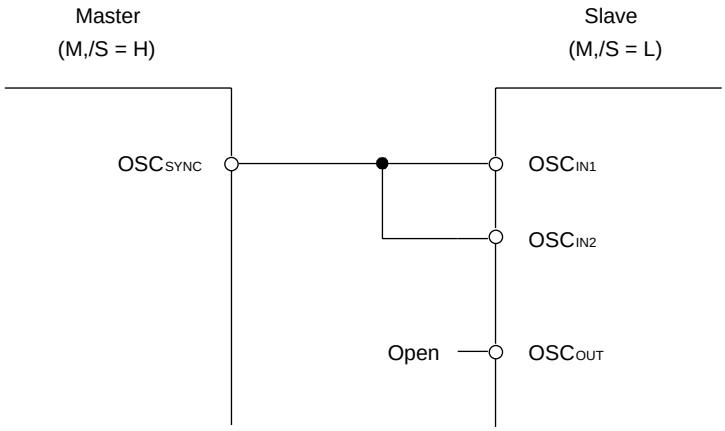
RM Connection	RS Connection	Clock for Main Duty Display	Clock for Sub-duty Display	Example
Connected	Connected	Internal oscillation	Internal oscillation	A
Not connected	Not connected	External clock	External clock	B

Figure 5–12. Example of Using Clock



OSC_{IN1} : For main duty
OSC_{IN2} : For sub-duty

Figure 5–13. Example of Master/Slave Connection



(A)

5.5 Display Timing Generator

The display timing generator generates timing signals for the line address circuit and display data latch circuit, from the display clock. The display data is latched to the display data latch circuit in synchronization with the display clock and output to the segment driver output pins. The display data can be read completely independently of the access to the display data RAM by the CPU. Therefore, even if the display data RAM is asynchronously accessed, no adverse effect, such as flickering, occurs on the LCD.

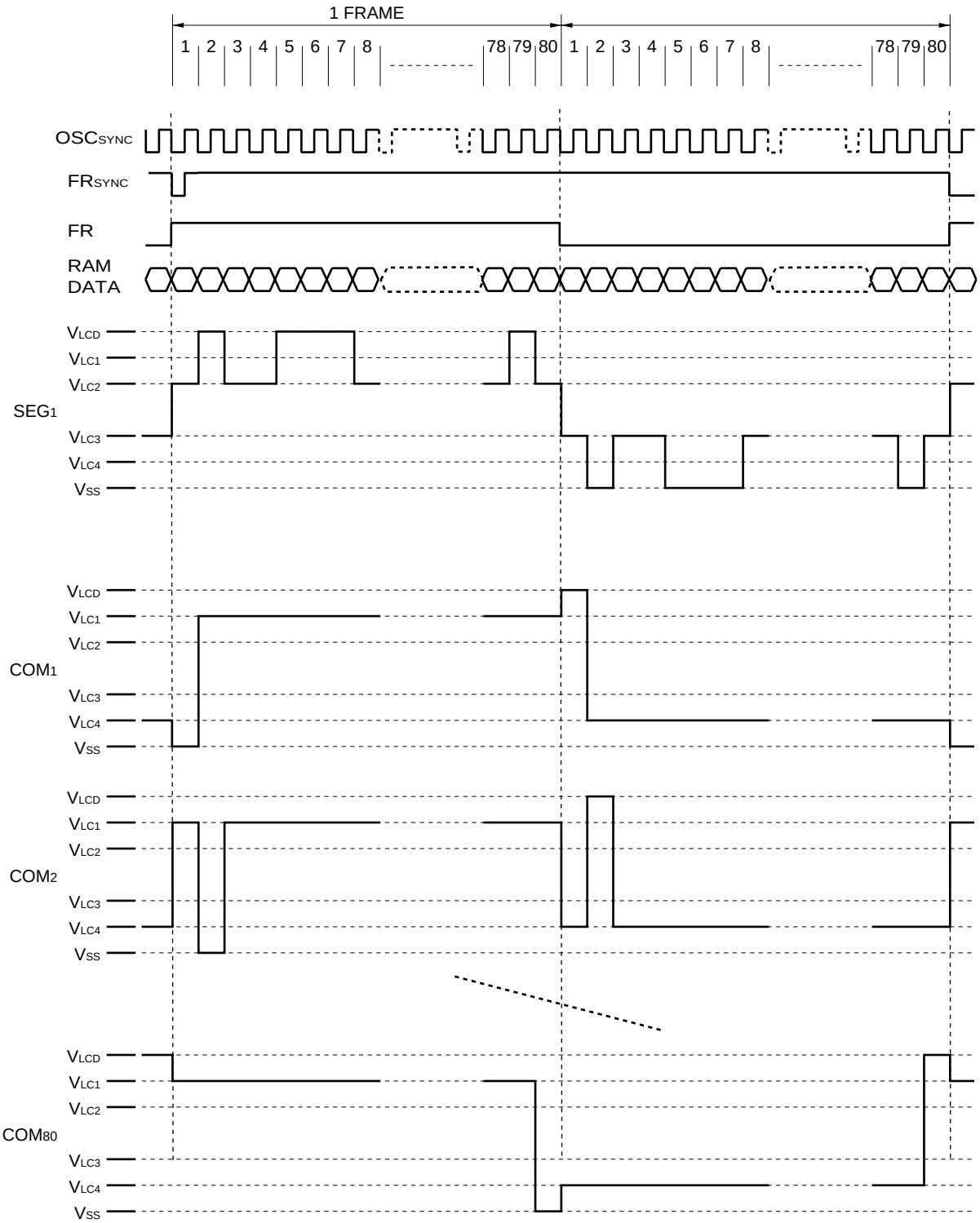
The internal common timing, LCD AC signal (FR), and frame synchronization signal (FR_{SYNC}) are generated by the display clock. A driver waveform in the frame AC driving mode shown in **Figure 5–14** is generated for the LCD driver circuit.

When the μPD161401 is used in a multi-chip configuration, the display timing signals for the slave chip (FR and FR_{SYNC}) must be supplied from the master chip.

Table 5–11. Relationship between FR, FR_{SYNC}, and Operation Mode

Operation Mode	FR	FR_{SYNC}
Master (M,/S = H)	Output	Output
Slave (M,/S = L)	Input	Input

Figure 5–14. Driver Waveform in Frame AC Driver Mode



5.6 Power Supply Circuit

5.6.1 Power supply circuit

The power supply circuit generates the voltage necessary for driving the LCD. The power circuit consists of a booster circuit, voltage regulator circuit, and voltage follower circuit.

Power system control register 1 (R52) turns ON/OFF the transformer, reference voltage generator, voltage regulator circuit (V regulator circuit), and voltage follower circuit (V/F circuit). Part of the internal power supply function and an external power supply can be used in combination. **Table 5–12** shows the functions controlled by the 4-bit data of power system control register 1 (R52). **Table 5–13** shows examples of combinations of the power circuit functions.

Table 5–12. Function of Each Bit of Power System Control Register

Item		Status	
		1	0
OP3	: Booster circuit control bit	ON	OFF
OP2	: Reference voltage generator control bit	ON	OFF
OP1	: Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
OP0	: Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 5–13. Examples of Combinations (Reference Values)

Status	OP3	OP2	OP1	OP0	Booster Circuit	Reference voltage	V Regulator Circuit	V/F Circuit	External Power Input	Booster System Pins
<1> Only internal power supply is used	1	1	1	1	O	O	O	O	V_{DD2}	Used
<2> External V_{OUT} power supply	0	1	1	1	×	O	O	O	V_{DD2}, V_{OUT}	Open
<3> Only V/F circuit is used	1	0	0	1	O	×	×	O	V_{DD2}, AMP_{OUT}	Used
<4> Only external power supply is used	0	0	0	0	×	×	×	×	V_{DD2}, V_{OUT}, V_{LCD}, V_{LC1} to V_{LC4}	Open

Remarks 1. The “booster system pins” are the C_1^+, C_1^- to C_5^+, C_5^- pins.

2. All the power circuits are turned OFF when the μPD161401 serves as a slave (M,/S pin = L).

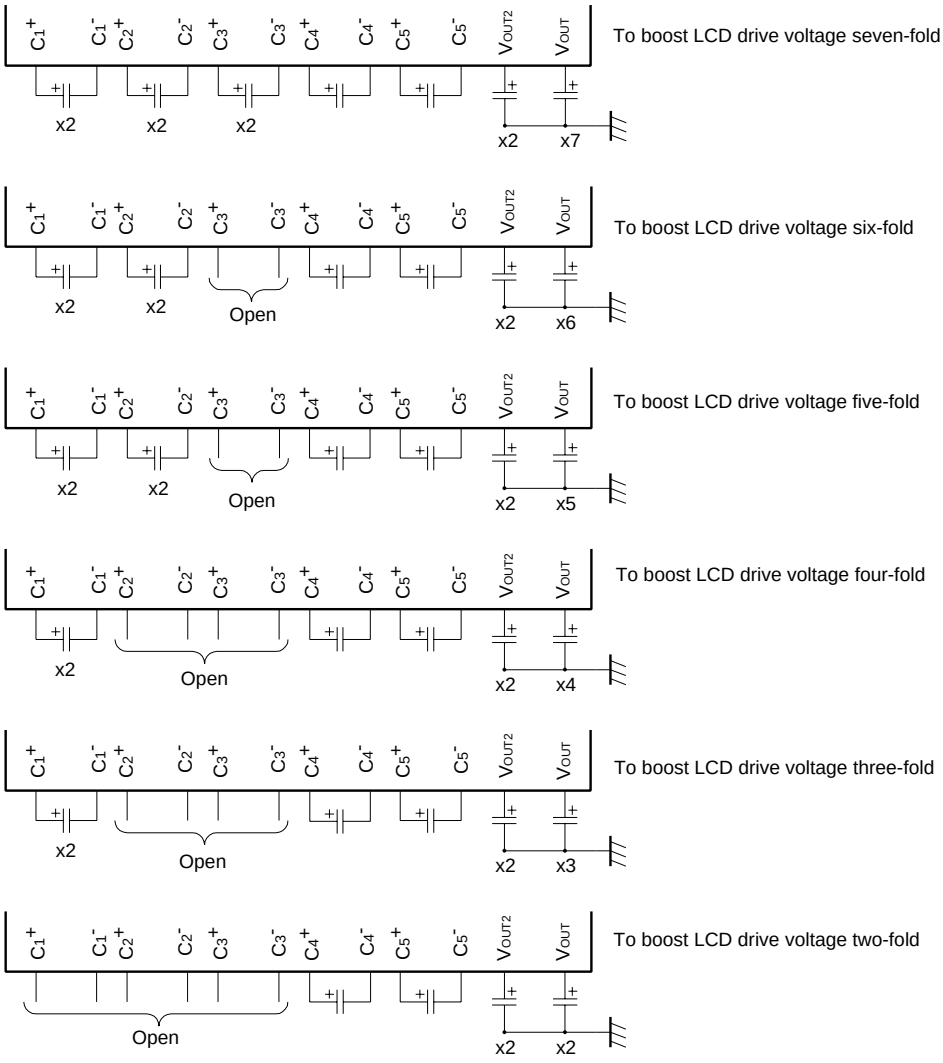
5.6.2 Booster circuit

The power supply circuit has an internal booster circuit that increases the LCD driver voltage two- to seven-fold. Because this booster circuit uses the internal oscillator signals, either the oscillator must be operating or an external display clock must be input to operate this circuit.

The booster circuit usually uses the C_1^+, C_1^- to C_5^+, C_5^- pins and V_{DD2} pins. Keep the wiring impedance of these pins as low as possible. The number of boosting steps for main duty display and sub-duty display is set as shown in **Table 5–14** by the MBT_n and SBT_n flags of power system control register 4 (R55).

For the number of boosting steps and how to connect capacitors, refer to **Figure 5–15**.

Figure 5–15. Number of Boosting Steps and Capacitor Connection



Remark "xN" (N = 2 to 7) of the capacitors in the above figure indicates the maximum voltage applied to the capacitors.

xN : V_{DD2} x N (V)

Table 5–14. Number of Boosting Steps of Main Duty/Sub-duty Display Booster Circuit (during Normal Display)

MBT2 SBT2	MBT1 SBT1	MBT0 SBT0	Number of Boosting steps (unit: fold)
0	0	0	Two
0	0	1	Three
0	1	0	Four
0	1	1	Five
1	0	0	Six
1	0	1	Seven
1	1	0	Prohibited
1	1	1	Prohibited

5.6.3 Voltage regulator circuit

The boosted voltage from V_{OUT} is supplied to the voltage regulator circuit and output to the LCD drive voltage pin V_{LCD}. Because the μPD161401 has a 128-step electronic volume function and an internal V_{LCD} adjuster resistor, a high-accuracy voltage regulator circuit can be configured by adding only a few components.

V_{LCD} regulator circuit

(a) When internal resistor for adjusting V_{LCD} is used

By using the internal resistor for adjusting V_{LCD} and the electronic control function, LCD drive voltage V_{LCD} can be controlled and the contrast of the LCD can be adjusted by using commands. In this case, no external resistor is necessary. Where $V_{LCD} < V_{OUT}$, the value of V_{LCD} can be calculated as follows:

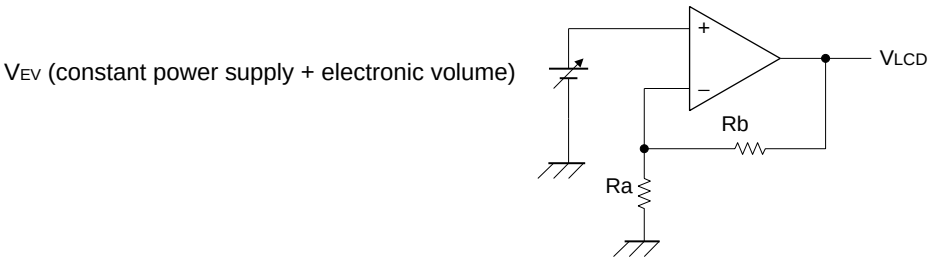
Example Calculating value of V_{LCD} (where $V_{LCD} < V_{OUT}$)

$$V_{LCD} = (1 + \frac{Rb}{Ra}) V_{EV}$$

$$V_{LCD} = (1 + \frac{Rb}{Ra}) (1 - \frac{\alpha}{256}) V_{REG}$$

Remark $V_{EV} = (1 - \frac{\alpha}{256}) V_{REG}$

Figure 5–16. Example of Circuit Using Internal Resistor for Adjustment V_{LCD}



V_{REG} is the internal fixed power source of the IC and has three types of temperature characteristic curves. These temperature characteristic curves can be adjusted as shown in **Table 5–15** depending on the setting of power system control register 1 (R52) (TCS2 to TCS0).

Table 5–15 shows V_{REG} at T_A = 25°C.

Table 5–15. Adjusting Temperature Characteristic Curve

Status	TCS2	TCS1	TCS0	Temperature Gradient (unit: %/°C)	V_{REG} (TYP.) (unit: V)
Internal power supply	0	0	0	–0.12	1.77
	0	0	1	–0.13	1.69
	0	1	0	–0.15	1.63
	0	1	1	–0.17	1.59
When external reference power supply is used	1	×	×	–	–

α is the value of the electronic volume register. It can take any of 128 values in accordance with the data set to the 7-bit electronic control register. The value of α set by the main electronic volume register (R57) (main duty display) and sub-electronic volume register (R58) (sub-duty display) is shown in **Table 5–16**.

Table 5–16. Changes in Value of α Depending on Setting of Electronic Volume Register

MEV6 / SEV6	MEV5 / SEV5	MEV4 / SEV4	MEV3 / SEV3	MEV2 / SEV2	MEV1 / SEV1	MEV0 / SEV0	α
0	0	0	0	0	0	0	256
0	0	0	0	0	0	1	126
0	0	0	0	0	1	0	125
0	0	0	0	0	1	1	124
			⋮				⋮
1	1	1	1	1	0	1	2
1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	0

Rb/Ra is a ratio of the internal resistors for adjusting V_{LCD}. This resistance ratio can be adjusted in 128 steps, by using power control register 2 (R53) (VRRn: main duty display mode, and SVRn: sub-duty display mode). The value of the reference voltage (1 + Rb/Ra) is determined as shown in **Table 5–17**, depending on the setting of 4 bits of the V_{LCD} internal resistance ratio register.

Table 5–17. Determining Reference Voltage Value by Setting of Internal Resistance Ratio Register

Register				1 + Rb/Ra
VRR3 / SVR3	VRR2 / SVR2	VRR1 / SVR1	VRR0 / SVR0	
0	0	0	0	3
0	0	0	1	4
0	0	1	0	5
0	0	1	1	6
0	1	0	0	7
0	1	0	1	8
0	1	1	0	9
0	1	1	1	10
1	0	0	0	11
1	0	0	1	12
1	0	1	0	13
1	0	1	1	14
1	1	0	0	15
1	1	0	1	16
1	1	1	0	17
1	1	1	1	18

(b) When external resistor is used (when internal resistor for adjusting V_{LCD} is not used)

LCD drive voltage V_{LCD} can be controlled not only by a setting of the internal resistor for adjusting V_{LCD} (IRS = L) but also by connecting resistors Rae, Rbe, and Rce between V_{SS} and V_R, between V_R and AMP_{OUTM}, and between V_R and AMP_{OUTS}, respectively. In this case also, LCD drive voltage V_{LCD} and the contrast of the LCD can be adjusted by using the electronic control function and commands.

In addition, the μPD161401 can select two values of V_{LCD} for normal display and partial display. These values are set by using an external divider resistor and automatically selected by the DTY flag of control register 2 (R1).

Where $V_{LCD} < V_{OUT}$, the value of V_{LCD} can be calculated by the expression in Example 1 (DTY = 0) and the expression in Example 2 (DTY = 1).

Example 1. To calculate value of V_{LCD} (DTY = 0, in main duty display mode)

$$V_{LCD} = (1 + \frac{Rbe}{Rae}) V_{EV}$$

$$V_{LCD} = (1 + \frac{Rbe}{Rae}) (1 - \frac{\alpha}{256}) V_{REG}$$

Remark $V_{EV} = (1 - \frac{\alpha}{256}) V_{REG}$

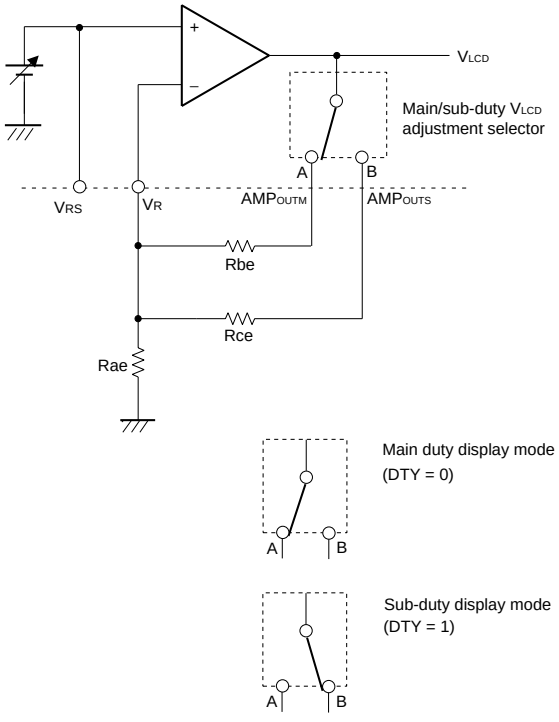
Example 2. To calculate value of V_{LCD} (DTY = 1, in sub-duty display mode)

$$V_{LCD} = (1 + \frac{Rce}{Rae}) V_{EV}$$

$$V_{LCD} = (1 + \frac{Rce}{Rae}) (1 - \frac{\alpha}{256}) V_{REG}$$

Remark $V_{EV} = (1 - \frac{\alpha}{256}) V_{REG}$

Figure 5–17. Example of Circuit Using External Resistor



5.6.4 Level voltage control by operational amplifier

Although the μPD161401 has a power-saving power supply circuit, the display quality may be degraded if it is used to drive a high-load LCD panel. The driving capability of the segment output can be controlled as shown in **Table 5–18** by LCS1 and LCS0 of power system control register 5 (R56), and the driving capability of the common outputs can be controlled as shown in **Table 5–19** by LCC1 and LCC0 of the same register. By controlling the driving capability, the display quality and power consumption may be improved. Determine the driving capability in accordance with the actual display status. If the display quality is not sufficiently improved in any driving mode, it will be necessary to supply the LCD drive voltage from an external power supply.

In addition, the operational amplifier driving modes shown in **Table 5–20** can be selected by the setting of HPM1 and HPM0, so that the wait time to stabilize the supply voltage immediately after the power has been turned ON or OFF can be shortened.

PSM1 specifies whether a boosting voltage of $V_{DD2} \times 2$ is applied to the V_{LC3} or V_{LC4} level voltage follower of (refer to **Table 5–21**). If a voltage boosted two-fold is applied to the voltage follower circuit, the current consumption may be reduced.

Thoroughly confirm and evaluate the V_{LC3} and V_{LC4} levels of the LCD panel with the actual system to determine whether the two-fold LCD drive voltage is to be supplied.

PSM0 can be used to set the current value of all the voltage follower circuits as shown in **Table 5–22**.

Table 5–18. Setting Driving Capability of Segment Outputs (LCS1, LCS0 = 0, 0)

LCS1	LCS0	Segment Output Driving Capability (unit: fold)
0	0	One
0	1	Two
1	0	Four
1	1	Eight

Table 5–19. Setting Driving Capability of Common Outputs (LCS1, LCS0 = 0, 0)

LCC1	LCC0	Common Output Driving Capability (unit: fold)
0	0	Two
0	1	Four
1	0	Eight
1	1	Sixteen

Table 5–20. Setting Operation Mode of Operational Amplifier

HPM1	HPM0	Mode Setting
0	0	Normal mode
0	1	Power supply ON mode 1
1	0	Power supply OFF mode
1	1	Power supply ON mode 2

Table 5–21. Setting of Two-Fold Drive Voltage

PSM1	Mode Setting
0	Not used
1	Used

Table 5–22. Voltage Follower Bias Current Setting

PSM0	Bias Current Setting (unit: fold)
0	One
1	Two

5.6.5 Application example of power supply circuit

Figure 5–18. IRS = H, [OP3, OP2, OP1, OP0] = [1, 1, 1, 1]

Six-fold drive voltage

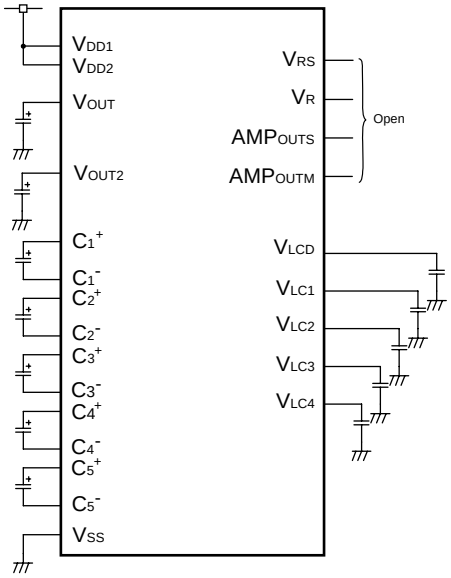


Figure 5–19. IRS = L, [OP3, OP2, OP1, OP0] = [1, 1, 1, 1]

Six-fold drive voltage

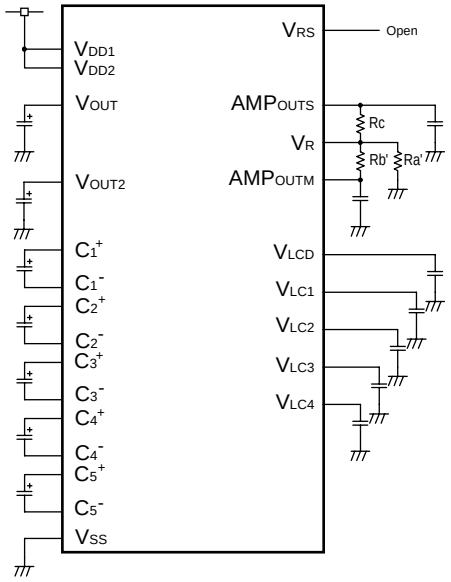


Figure 5–20. IRS = H, [OP3, OP2, OP1, OP0] = [0, 0, 0, 1]

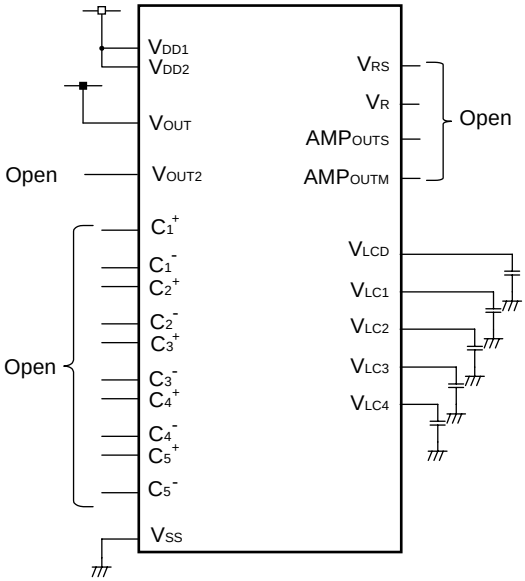


Figure 5–21. IRS = L, [OP3, OP2, OP1, OP0] = [0, 0, 0, 1]

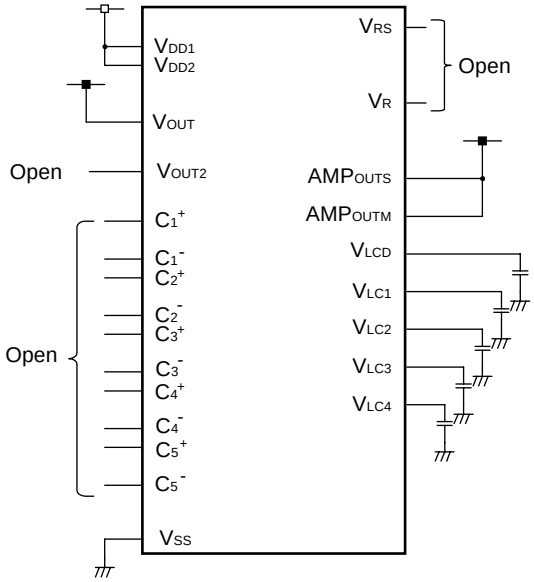


Figure 5–22. IRS = L, [OP3, OP2, OP1, OP0] = [0, 0, 0, 0]

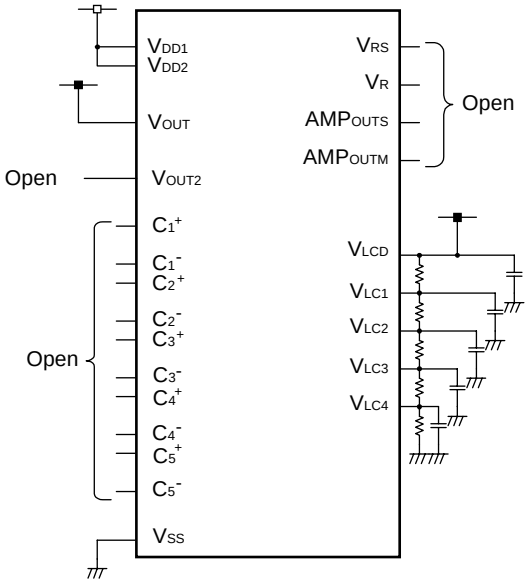


Figure 5–23. Master/Slave Connection Example 1

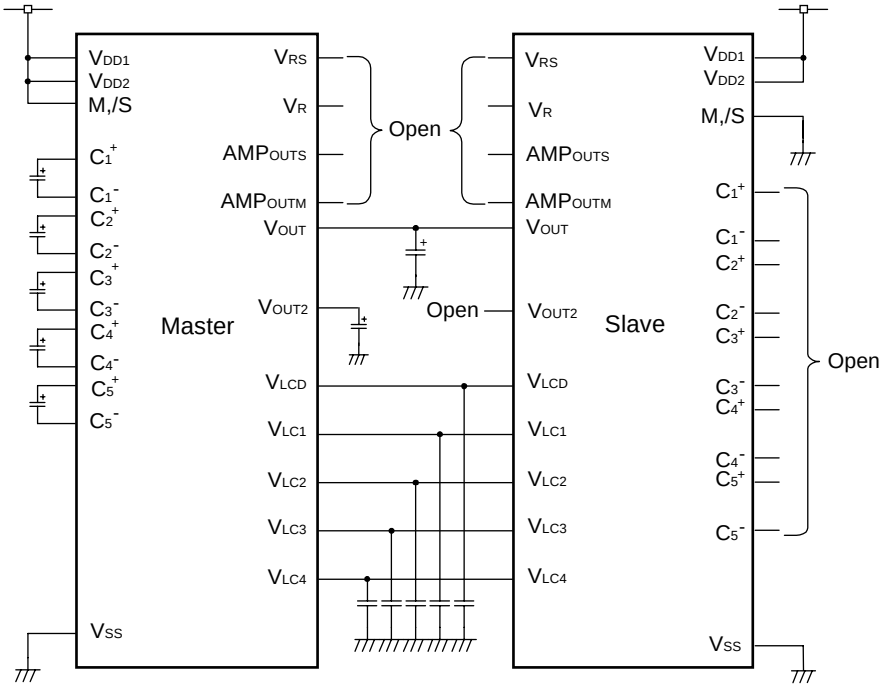
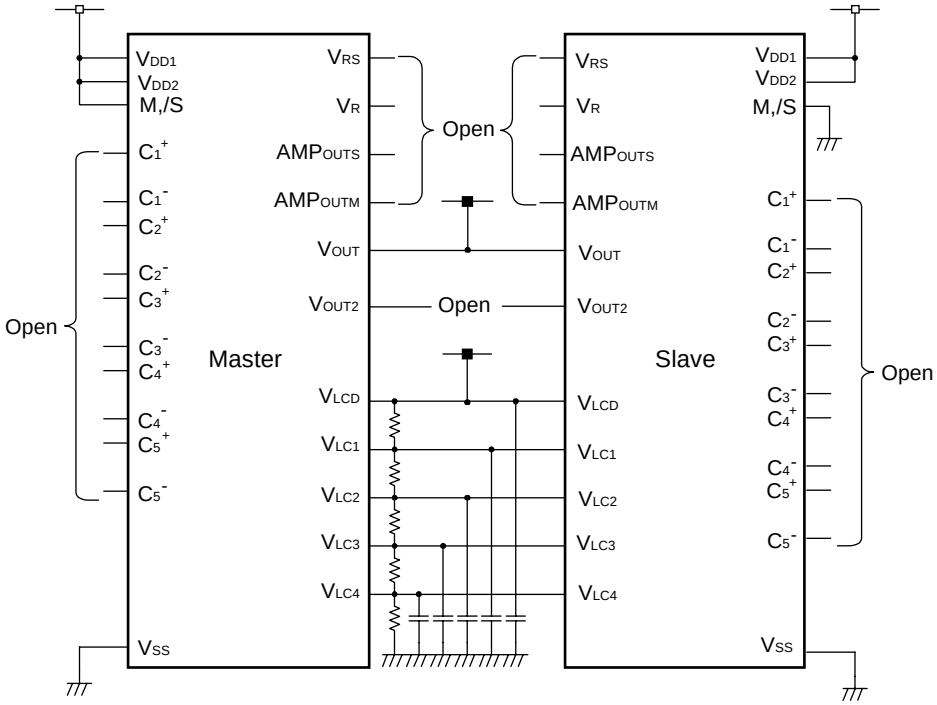


Figure 5–24. Master/Slave Connection Example 2



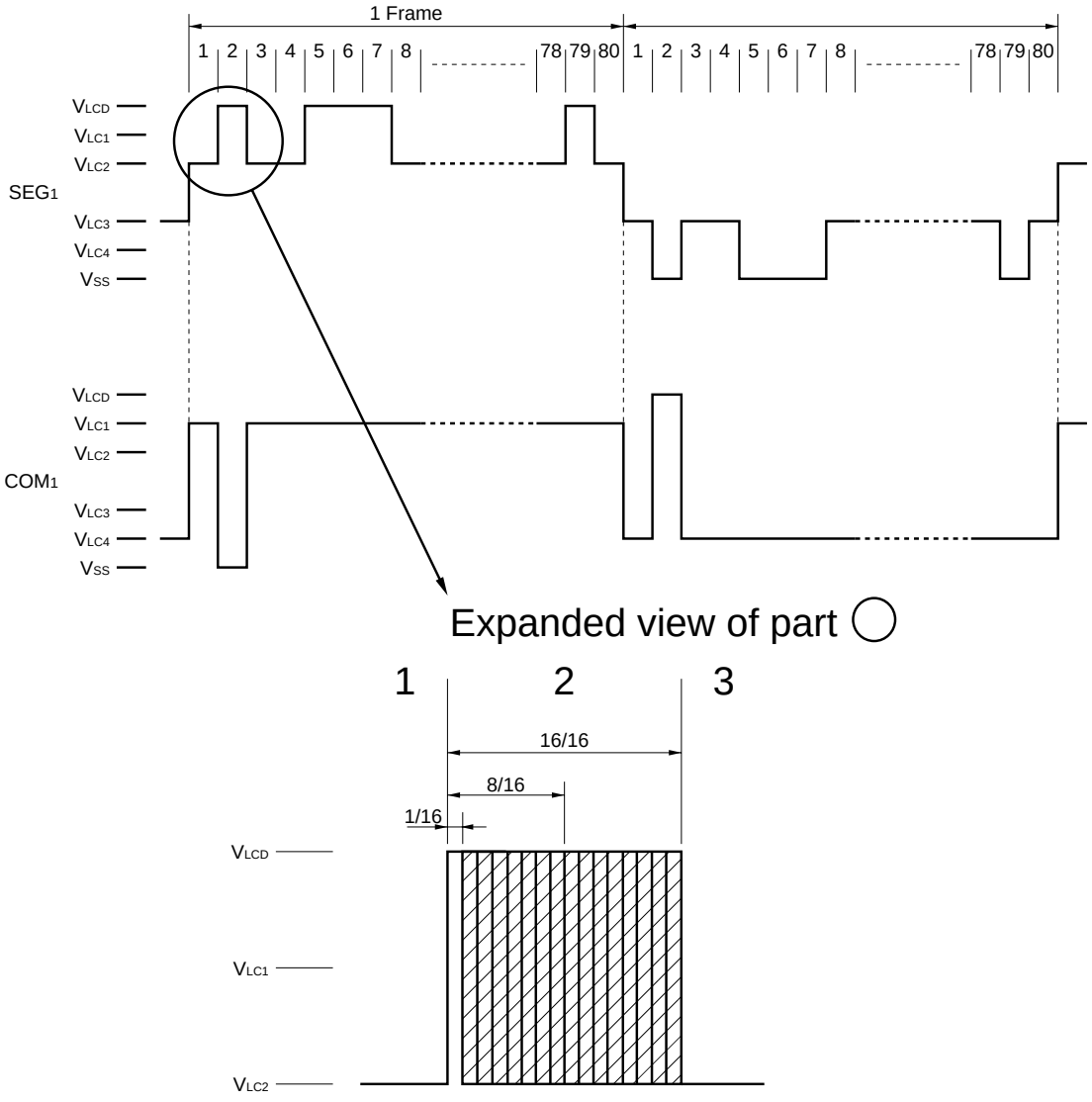
5.7 Driving LCD

The μPD161401 has a full-dot driver. This full-dot driver can modulate grayscale, depending on the setting of the pulse widths. In this driving mode, eight R/G output grayscales and four B output grayscales are selected from a 17-stage grayscale palette, and the selected grayscales are registered to the output grayscale palette of the IC. For details, refer to **Table 5–23** Example of Pulse Width Modulation Output.

5.7.1 Full-dot pulse modulation

The pulse width modulation function of the μPD161401 divides the segment pulse width of the signal for normal LCD display (16), and outputs the divided pulse width in accordance with the output timing of dots at the ratio of the grayscale palette selected by a command.

Figure 5–25. Full-Dot Pulse Width Modulation



Caution The width of the common output pulse is not modulated.

The pulse is output in the form of combined odd line/even line or even line/odd line output, as shown in **Figure 5–26**. **Table 5–23** shows the combination of the rising and falling edges of the pulse of each frame.

Figure 5–26. Example of Pulse Width Modulation Output of Odd/Even Line

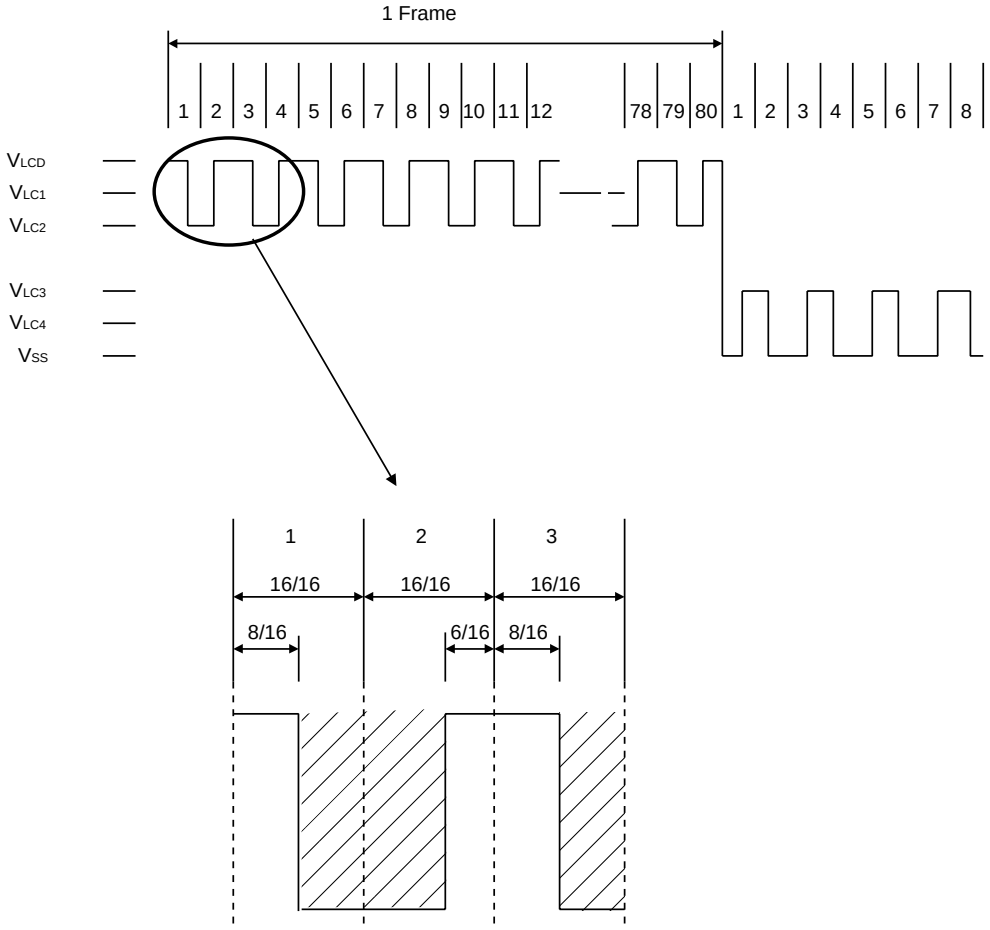


Table 5–23. Pulse Width Modulation Output

Grayscale Level	COM	1 or 2 Frames		3 or 4 Frames	
		SEG Odd Number	SEG Even Number	SEG Odd Number	SEG Even Number
0	2n+1	0	0	0	0
	2n+2	0	0	0	0
1	2n+1	1↑	1↓	1↓	1↑
	2n+2	1↓	1↑	1↑	1↓
2	2n+1	2↑	2↓	2↓	2↑
	2n+2	2↓	2↑	2↑	2↓
3	2n+1	3↑	3↓	3↓	3↑
	2n+2	3↓	3↑	3↑	3↓
4	2n+1	4↑	4↓	4↓	4↑
	2n+2	4↓	4↑	4↑	4↓
5	2n+1	5↑	5↓	5↓	5↑
	2n+2	5↓	5↑	5↑	5↓
6	2n+1	6↑	6↓	6↓	6↑
	2n+2	6↓	6↑	6↑	6↓
7	2n+1	7↑	7↓	7↓	7↑
	2n+2	7↓	7↑	7↑	7↓
8	2n+1	8↑	8↓	8↓	8↑
	2n+2	8↓	8↑	8↑	8↓
9	2n+1	9↑	9↓	9↓	9↑
	2n+2	9↓	9↑	9↑	9↓
10	2n+1	10↑	10↓	10↓	10↑
	2n+2	10↓	10↑	10↑	10↓
11	2n+1	11↑	11↓	11↓	11↑
	2n+2	11↓	11↑	11↑	11↓
12	2n+1	12↑	12↓	12↓	12↑
	2n+2	12↓	12↑	12↑	12↓
13	2n+1	13↑	13↓	13↓	13↑
	2n+2	13↓	13↑	13↑	13↓
14	2n+1	14↑	14↓	14↓	14↑
	2n+2	14↓	14↑	14↑	14↓
15	2n+1	15↑	15↓	15↓	15↑
	2n+2	15↓	15↑	15↑	15↓
16	2n+1	16↑	16↓	16↓	16↑
	2n+2	16↓	16↑	16↑	16↓

Remarks 1. n: Integer of 0 to 39

2. ↑A: Pulse rises in the middle of A line output.

3. ↓A: Pulse rises at the beginning of A line output.

4. A: PWM pulse width (A/16)

5.7.2 Grayscale palette

The μPD161401 has 17 levels of grayscale outputs. Eight R/G output grayscales and four B output grayscales can be selected for each of main duty display and sub-duty display, by using the grayscale data registers (R65 to R104), and can be output as the grayscale outputs of the IC to R/G/B.

Table 5–24. Correspondence of Grayscale Levels of Grayscale Data Registers

Grayscale Level	Set Value of Grayscale Data Register					Remark
	D_4	D_3	D_2	D_1	D_0	
Level 0	0	0	0	0	0	OFF data
Level 1	0	0	0	0	1	
Level 2	0	0	0	1	0	
Level 3	0	0	0	1	1	
Level 4	0	0	1	0	0	
Level 5	0	0	1	0	1	
Level 6	0	0	1	1	0	
Level 7	0	0	1	1	1	
Level 8	0	1	0	0	0	50%
Level 9	0	1	0	0	1	
Level 10	0	1	0	1	0	
Level 11	0	1	0	1	1	
Level 12	0	1	1	0	0	
Level 13	0	1	1	0	1	
Level 14	0	1	1	1	0	
Level 15	0	1	1	1	1	
Level 16	1	0	0	0	0	100%

5.7.3 Setting of display size

The μPD161401 can set the main duty cycles in a range of 1/80, 1/72 and 1/64 duty, the sub-duty cycles in a range of 1/48, 1/40, 1/32, 1/24 and 1/16 duty. This can be done by setting MDT6 to MDT0 and SDT6 to SDT0 of the main duty setting register (R14) and sub-duty setting register (R17) as **Table 5–25** and **5–26**:

Table 5–25. Setting of Main Duty (R14)

MDT6	MDT5	MDT4	MDT3	MDT2	MDT1	MDT0	Duty
1	0	0	1	1	1	1	1/80
1	0	0	0	1	1	1	1/72
0	1	1	1	1	1	1	1/64

Table 5–26. Setting of Sub-duty (R17)

SDT6	SDT5	SDT4	SDT3	SDT2	SDT1	SDT0	Duty
0	1	0	1	1	1	1	1/48
0	1	0	0	1	1	1	1/40
0	0	1	1	1	1	1	1/32
0	0	1	0	1	1	1	1/24
0	0	0	1	1	1	1	1/16

5.7.4 Setting of LCD N-line inversion and M-line shift

During main duty display, the shift amount of the reverse position of AC driving and the reverse position of each display frame can be set by the main duty N-line inversion register (R15) and main duty M-line shift register (R16). They can also be set by the sub-duty N-line inversion register (R18) and sub-duty M-line shift register (R19) during sub-duty display.

The N-line reverse cycle function can set a line to be reversed as shown in **Table 5–27**, depending on the setting of MID5 to MID0 or SID5 to SID0 of the main or sub-duty N-line inversion register.

The M-line shift amount of the reverse position of each display frame can be set as shown in **Table 5–28**, by using MSD5 to MSD0 or SSD5 to SSD0 of the main or sub-duty M-line shift register.

Table 5–27. Setting of N-line Inversion Register (R15)

MID5 / SID5	MID4 / SID4	MID3 / SID3	MID2 / SID2	MID1 / SID1	MID0 / SID0	Reversed Cycle
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
		⋮				⋮
1	0	0	1	0	1	38
1	0	0	1	1	0	39
1	0	0	1	1	1	40

Table 5–28. Setting of M-line Shift Register

MSD5	MSD4	MSD3	MSD2	MSD1	MSD0	Reversed Position Shift Amount
SSD5	SSD4	SSD3	SSD2	SSD1	SSD0	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
		⋮				⋮
1	0	0	1	1	0	38
1	0	0	1	1	1	39
1	0	1	0	0	0	40

Make sure that the display size, reverse cycle, and shift amount of reverse position have the relationship indicated by the following expression:

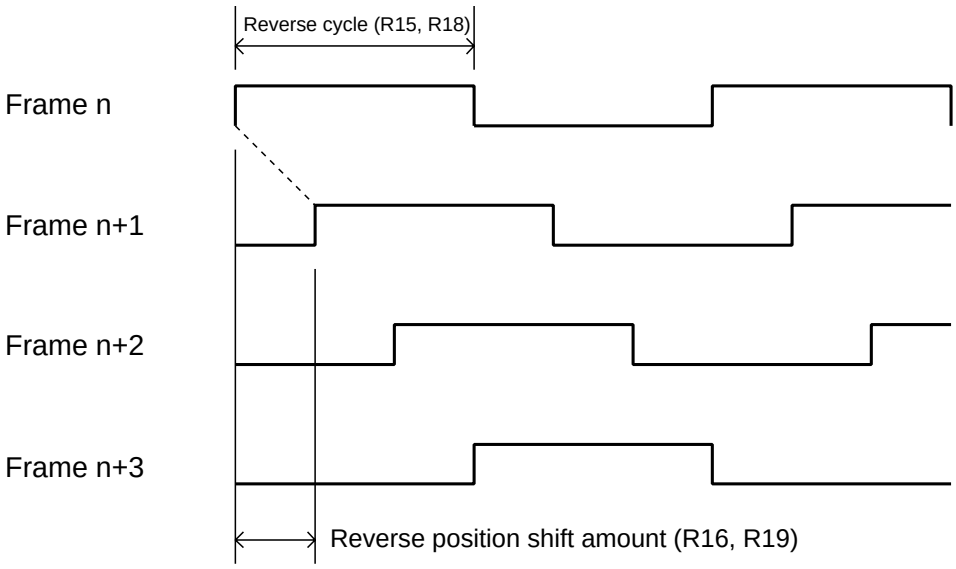
Display size (duty) ≥ reverse cycle ≥ reverse shift amount

5.7.5 Reverse driving between frames

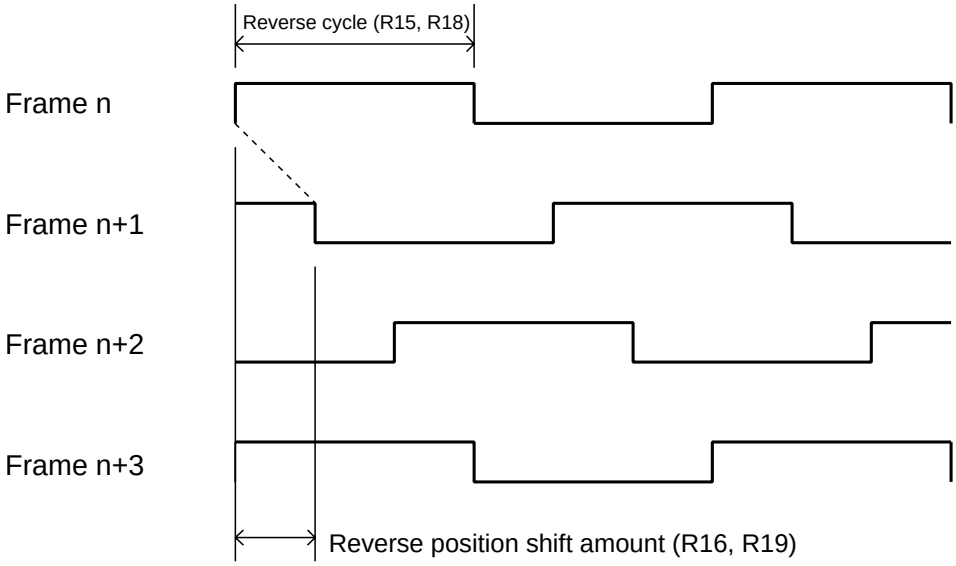
In the μPD161401, the LCD drive waveform can be reversed and output between frames by setting the FXOR flag of Driving mode select register (R64), as shown in **Figure 5–27**. This function is executed in combination with the reverse cycle and reverse shift functions.

Figure 5–27. Image of Reversal between Pulse Width Modulation Frames

Reversal between frames not implemented (FXOR = 0)



Implementation of reversal between frames (FXOR = 1)



5.8 Display Mode

5.8.1 Selecting display mode

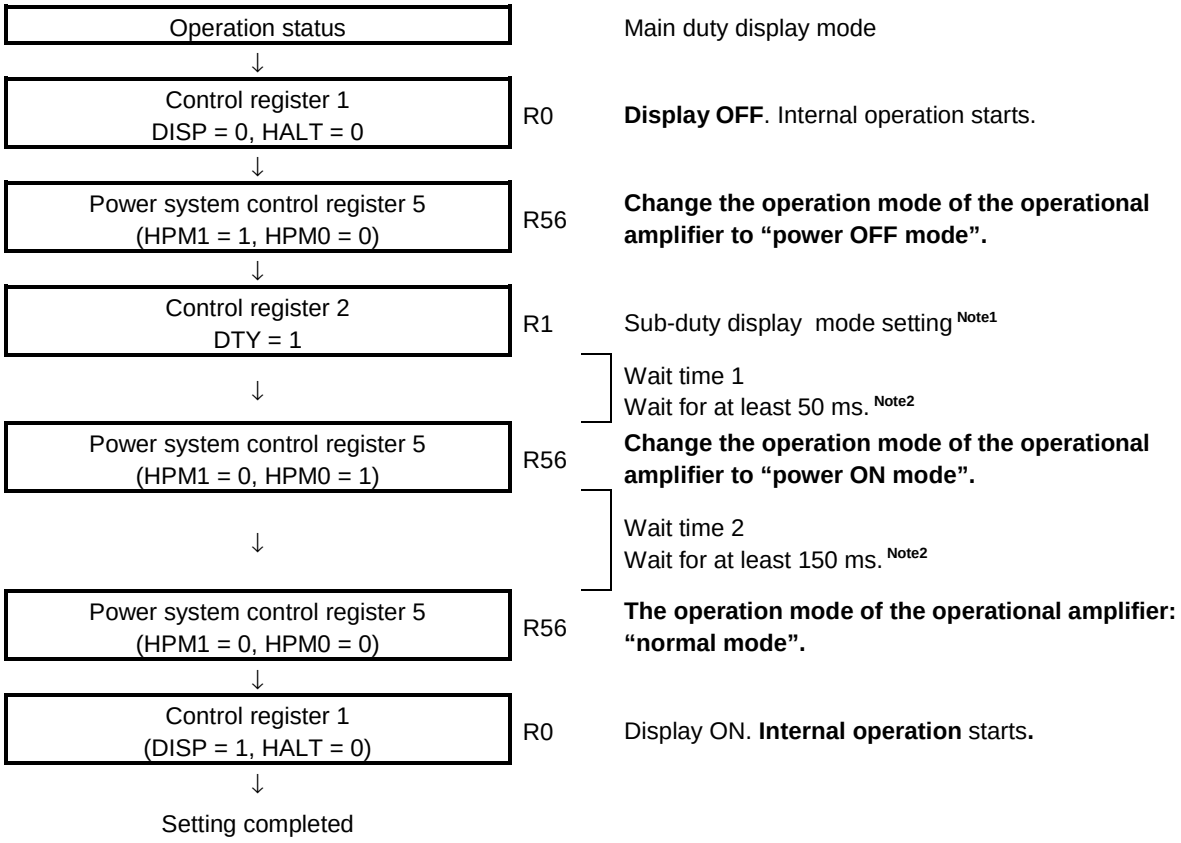
The μPD161401 has two display modes: main duty display and sub-duty display. In each of these modes, any duty ratio can be selected and parts other than the display area can be scanned with a non-selected waveform.

The display mode can be selected by using the DTY flag of control register 2 (R1), and parameters such as the duty ratio, bias value, and number of boosting steps are automatically selected as shown in the table below.

Display Setting	Main Duty Display (DTY = 0)	Sub-duty Display (DTY = 1)
Duty ratio	Main duty setting register (R14)	Sub-duty setting register (R17)
N-line inversion	Main duty N-line inversion register (R15)	Sub-duty N-line inversion register (R18)
M-line shift	Main duty M-line shift register (R16)	Sub-duty M-line shift register (R19)
V_{LCD} adjustment	Power system control register 2 (R53) VRR3 to VRR0	Power system control register 2 (R53) SVR3 to SVR0
Bias value	Power system control register 3 (R54) BIS2 to BIS0	Power system control register 3 (R54) SBIS2 to SBIS0
Number of boosting steps	Power system control register 4 (R55) MBT2 to MBT0	Power system control register 4 (R55) SBT2 to SBT0
Electronic volume	Main electronic volume register (R57)	Sub-electronic volume register (R58)
Grayscale data setting	Main R grayscale data registers (R65 to R72) Main G grayscale data registers (R73 to R80) Main B grayscale data registers (R81 to R84)	Sub R grayscale data registers (R85 to R92) Sub G grayscale data registers (R93 to R100) Sub B grayscale data registers (R101 to R104)

When the mode is changed from the main duty display mode to the sub-duty display mode or vice versa, the display screen may be temporarily disturbed, depending on the setting of each duty mode, if electric charge remains in the smoothing capacitor connected between the LCD drive voltage pins (V_{LCD}, V_{LC1} to V_{LC4}) and V_{SS}. It is recommended that the following power sequence be observed to avoid any trouble that may occur when the display mode is changed.

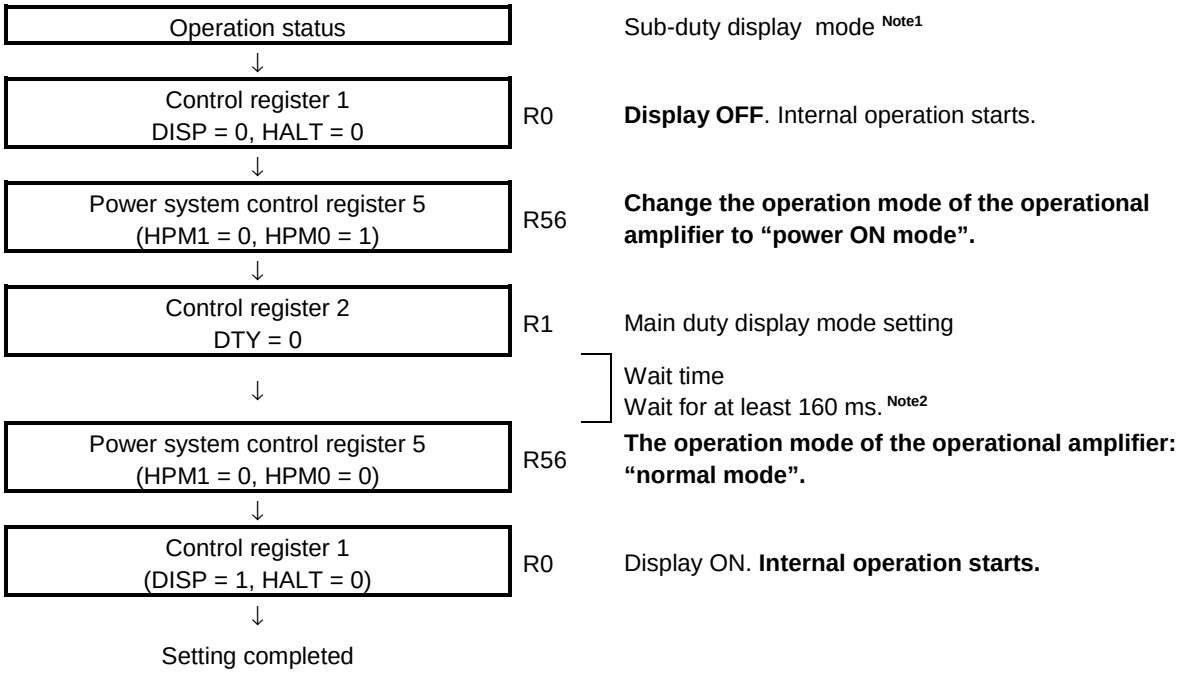
★ **(1) Main duty display mode to sub-duty display mode**



Notes 1. A scroll function cannot be used in sub-duty display mode. In the state where the scroll function is used by main duty display mode when it changes to sub-duty, a scroll function is disregarded. Then, when it changes to main duty display mode again, a scroll function returns to an effective state (state before changing to sub-duty).

2. The wait times 1, 2 vary depending on the characteristics of the LCD panel and the capacitance of the boosting or smoothing capacitor. It is recommended to determine these values after thorough evaluation with the actual system.

★ **(2) Sub-duty display mode to main duty display mode**



Notes 1. A scroll function cannot be used in sub-duty display mode. In the state where the scroll function is used by main duty display mode when it changes to sub-duty, a scroll function is disregarded. Then, when it changes to main duty display mode again, a scroll function returns to an effective state (state before changing to sub-duty).

2. The wait time varies depending on the characteristics of the LCD panel and the capacitance of the boosting or smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system.

5.8.2 Screen scrolling

The μPD161401 has a screen scroll function. This function is enabled during main duty display. The width of the area to be fixed is specified by the scroll fixed area width register (R27) and the number of scroll steps is set by the scroll step number register (R31). By these settings, other parts of screen can be scrolled with part of the screen fixed. To specify the position of the area to be fixed, set the FIXAHL flag of the scroll fixed area position register (R23) as shown in **Table 5–29**. Specify the fixed area position on the upper part of the LCD panel in master mode and on the bottom part of the panel in slave mode.

Table 5–29. Scroll Fixed Area Width Register (R27)

FIXAW1	FIXAW0	Fixed area width
0	0	0
0	1	16
1	0	24
1	1	32

Table 5–30. Scroll Step Count Register (R31)

MST6	MST5	MST4	MST3	MST2	MST1	MST0	Number of Scroll Steps
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
			⋮				⋮
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79
1	0	1	0	0	0	0	Other settings prohibited

Note that the relationship between the number of scroll steps and the width of the scroll fixed area needs to be set so that the following condition is set.

Number of scroll steps ≤ 79 – Width of scroll fixed area

Caution If values other than the above is set, the operation is not guaranteed.

Table 5–31. Scroll Fixed Area Position Register (R23)

FIXAHL	LCD Display Position
0	Bottom
1	Upper

5.8.3 Scroll setting examples

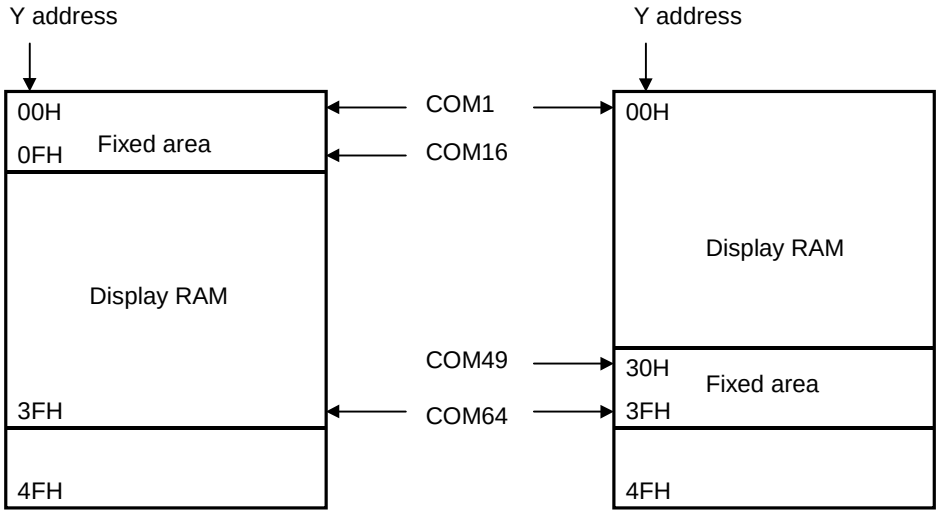
★ **(1) Setting example 1**

Duty: 1/64 duty

RAM read direction: normal (R0:COMR = 0)

Scroll fixed area width: 16 lines (R27: FIXAW1,0 = 0,1)

(a) Scroll fixed position: upper (R23: FIXAHL = 1)



(b) Scroll fixed position: bottom (R23: FIXAHL = 0)

The relationships between the numbers of scroll steps and RAM Y address scan order in cases of (a) and (b) are as follows.

(a)

Number of scroll steps: 0 (R31: MSTn = 00H)	RAM Y address: 00H → 0FH, 10H → 3FH
Number of scroll steps: 1 (R31: MSTn = 01H)	RAM Y address: 00H → 0FH, 11H → 40H
Number of scroll steps: 10 (R31: MSTn = 0AH)	RAM Y address: 00H → 0FH, 1AH → 49H

(b)

Number of scroll steps: 0 (R31: MSTn = 00H)	RAM Y address: 00H → 2FH, 30H → 3FH
Number of scroll steps: 1 (R31: MSTn = 01H)	RAM Y address: 00H → 2FH, 40H, 30H → 3FH
Number of scroll steps: 10 (R31: MSTn = 0AH)	RAM Y address: 0AH → 2FH, 40H → 49H, 30H → 3FH

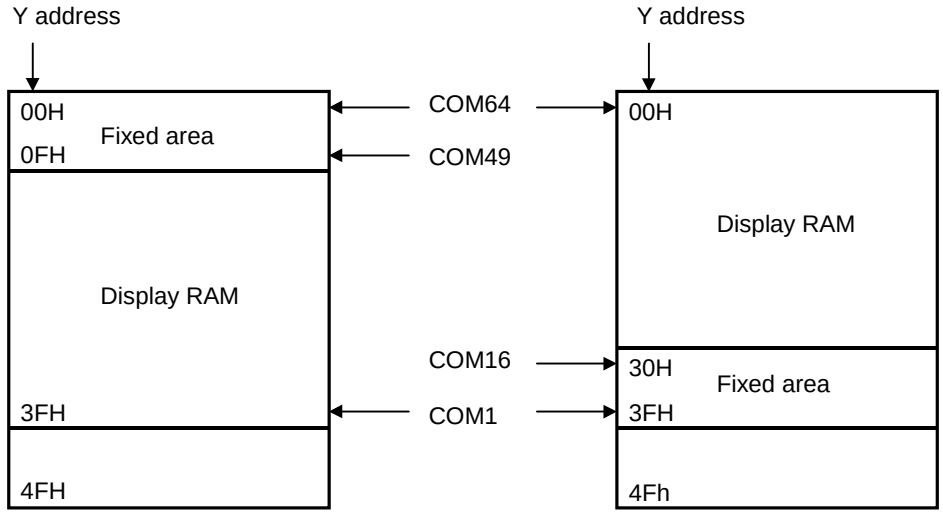
★ **(2) Setting example 2**

Duty: 1/64 duty

RAM read direction: reverse (R0: COMR = 1)

Scroll fixed area width: 16 lines (R27: FIXAW1,0 = 0,1)

(a) Scroll fixed position: upper (R23: FIXAHL = 1) **(b) Scroll fixed position: bottom (R23: FIXAHL = 0)**



The relationships between the numbers of scroll steps and RAM Y address scan order in cases of (a) and (b) are as follows.

(a)

Number of scroll steps: 0 (R31: MSTn = 00H)	RAM Y address: 3FH → 10h, 0FH → 00H
Number of scroll steps: 1 (R31: MSTn = 01H)	RAM Y address: 40H → 11h, 0FH → 00H
Number of scroll steps: 10 (R31: MSTn = 0AH)	RAM Y address: 49H → 1Ah, 0FH → 00H

(b)

Number of scroll steps: 0 (R31: MSTn = 00H)	RAM Y address: 3Fh → 30H, 2FH → 00H
Number of scroll steps: 1 (R31: MSTn = 01H)	RAM Y address: 3Fh → 30H, 40h, 2FH → 01H
Number of scroll steps: 10 (R31: MSTn = 0AH)	RAM Y address: 3Fh → 30hH, 49H → 40H, 2FH → 0AH

5.9 Reset

When the reset command is input, the IC is initialized to the default status shown in the table below. Note that initialization by using the /DISP pin should be used only to prevent malfunctioning due to noise.

Table 5–32. Default Values of Registers (1/2)

Register		Reset Command	/DISP
Control register 1	R0	O	O (DISP, TRON flag only)
Control register 2	R1	O	×
X address register	R4	O	×
Y address register	R5	O	×
MIN.·X address register	R7	O	×
MAX.·X address register	R8	O	×
MIN.·Y address register	R9	O	×
MIN.·Y address register	R10	O	×
Display memory access register	R12	×	×
Main duty setting register	R14	O	×
Main duty N-line inversion register	R15	O	×
Main duty M-line shift register	R16	O	×
Sub-duty setting register	R17	O	×
Sub-duty N-line inversion register	R18	O	×
Sub-duty M-line shift register	R19	O	×
COM scanning address setting register	R21	O	×
Sub-duty start address register	R22	O	×
Scroll fixed area position register	R23	O	×
Scroll fixed area width register	R27	O	×
Scroll steps number register	R31	O	×
Blinking/reverse setting register	R37	O	×
Complementary color blink X address register	R38	O	×
Complementary color blink start line address register	R39	O	×
Complementary color blink end line address register	R40	O	×
Complementary color blink data memory register	R41	×	×
Specified color blink X address register	R42	O	×
Specified color blink start line address register	R43	O	×
Specified color blink end line address register	R44	O	×
Specified color blink data memory register	R45	×	×
Specified color setting register	R46	O	×
Reverse X address register	R47	O	×
Reverse start line address register	R48	O	×

Remark O: Default value is input. X: Default value is not input.

Cautions 1. When initialization is made using the /DISP pin, the contents of memory are not guaranteed. In this case, use the initialized RAM. When initialization is made via the reset command, the contents of memory are retained.

2. If the device is initialized by the /DISP pin while the serial interface is being used, the serial clock counter is initialized.

3. Always input the reset command as the first command after power application.

Table 5–32. Default Values of Registers (2/2)

Register		Reset Command	/DISP
Reverse end line address register	R49	O	×
Reversed data memory access register	R50	×	×
Power system control register 1	R52	O	×
Power system control register 2	R53	O	×
Power system control register 3	R54	O	×
Power system control register 4	R55	O	×
Power system control register 5	R56	O	×
Main electronic volume register	R57	O	×
Sub-electronic volume register	R58	O	×
RAM test mode setting register	R61	O	×
Driving mode select register	R64	O	×
Main R grayscale data registers 1 to 8	R65 to R72	O	×
Main G grayscale data registers 1 to 8	R73 to R80	O	×
Main B grayscale data registers 1 to 4	R81 to R84	O	×
Sub R grayscale data registers 1 to 8	R85 to R92	O	×
Sub G grayscale data registers 1 to 8	R93 to R100	O	×
Sub B grayscale data registers 1 to 8	R101 to R104	O	×

Remark O: Default value is input. X: Default value is not input.

Cautions 1. When initialization is made using the /DISP pin, the contents of memory are not guaranteed. In this case, use the initialized RAM. When initialization is made via the reset command, the contents of memory are retained.

2. If the device is initialized by the /DISP pin while the serial interface is being used, the serial clock counter is initialized.

3. Always input the reset command as the first command after power application.

6. COMMANDS

The μPD161401 identifies data bus signals by a combination of the RS, /RD (E), and /WR (R,/W) signals. It interprets and executes commands only in accordance with the internal timing, without being dependent upon the external clock. Therefore, the processing speed is extremely high and, usually, no busy check is necessary.

An i80 system CPU interface inputs a low pulse to the /RD pin when it reads data from the μPD161401 to issue a command. It inputs a low pulse to the /WR pin when it writes data to the μPD161401.

Data can be read from an M68 system CPU interface if a high-pulse signal is input to the R,/W pin, and written if a low-pulse signal is input to the R,/W pin. A command is executed if a high-pulse signal is input to the E pin in this status. Therefore, in the explanation of the commands and display commands in **6.1 Control Register 1 (R0)** and the sections that follow, the M68 system CPU interface uses H, instead of /RD (E), when reading status or display data. This is how it differs from the i80 system CPU interface.

The commands of the μPD161401 are explained below, taking an i80 system CPU interface as an example. When the serial interface is used, sequentially input data to the μPD161401, starting from D_7.

The data bus length to input commands is as follows:

- Commands other than those that manipulate the display memory access register (R12) are input in byte units, regardless of the value of BMOD (control register 2 (R1), bus length setting).
- The commands that manipulate the display memory access register (R12) are input in 1-byte units when BMOD = 1, or in 2-byte units when BMOD = 0.

A. Commands other than those that manipulate display memory access register (R12)

BMOD = 1 (8-bit data bus)

Pin	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMOD = 0 (16-bit data bus)

Pin	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Note 0 or 1

B. Display memory access register (R12)

BMOD = 1 (8-bit data bus)

Pin	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMOD = 0 (16-bit data bus)

Pin	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

6.1 Control Register 1 (R0)

This command specifies the general operation mode of the μPD161401.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	TRON	WAS	COMF	DISP	STBY	HALT	ADC	COMR

TRON	0: Normal mode (all values written to the test register are ignored) 1: Test register valid mode (values written to the test register are valid)
WAS	0: Normal data write mode 1: Window access mode (Refer to **5.2.7 Arbitrary address area access (window access mode (WAS))**.)
COMF	0: Normal display operation 1: All output from common pins is OFF (all the common pins output a non-selected waveform. At this time, the segment pins output OFF data (level 0)).
DISP	0: Display OFF (All the LCD output pins output a V_{SS} level, and the oscillator and DC/DC converter operate.) 1: Display ON
STBY	0: Normal operation 1: Internal operation and oscillation stop. Display OFF
HALT	0: Internal operation starts. 1: Internal operation stops (all the LCD output pins output a V_{SS} level, the oscillator operates, and the DC/DC converter stops, and the reference voltage generator operates).
ADC	Column addresses correspond to SEG outputs that are used to display the display data RAM (refer to **Table 6–1**).
COMR	Selects the direction in which the lines of the graphic RAM are read (refer to **Table 6–2**).

Table 6–1. Relationship between Column Address of Display RAM and Segment Output

SEG Output		SEG_1	•••		SEG_{303}
ADC	0	000H	→	Column address →	12EH
(D_1)	1	12EH	←	Column address ←	000H

Table 6–2. Relationship between Common Scan Circuit and Scan Direction

COMR	0	00H	→	4FH
(D_0)	1	4FH	→	00H

Default (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.2 Control Register 2 (R1)

This command specifies the general operation mode of the μPD161401.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	FDM		BMOD		DTY	INC	XDIR	YDIR

FDM	Sets all screen display modes. 0: Normal operation 1: All screen display (Turns ON all screens [outputs grayscale level 16 to all screens].)
BMOD	Selects data length when parallel data is input. 0: 16-bit data bus 1: 8-bit data bus
DTY	0: Main duty display mode 1: Sub-duty display mode
INC Note	0: Increments/decrements X address each time it is accessed. 1: Increments/decrements Y address each time it is accessed.
XDIR Note	Specifies the direction in which the X address is to be accessed. 0: Increment (+1) 1: Decrement (-1)
YDIR Note	Specifies the direction in which the Y address is to be accessed. 0: Increment (+1) 1: Decrement (-1)

Note If the access direction is changed by INC, XDIR, or YDIR, be sure to set the X address register (R4) and Y address register (R5) before accessing the display RAM.

Table 6–3. Relationship between Functions of μPD161401 and Display Mode

Display Setting	Main Duty Display (DTY = 0)	Sub-duty Display (DTY = 1)
Duty	Main duty setting register (R14)	Sub-duty setting register (R17)
N-line inversion	Main duty N-line inversion register (R15)	Sub-duty N-line inversion register (R18)
M-line shift	Main duty M-line shift register (R16)	Sub-duty M-line shift register (R19)
V_{LCD} adjustment	Power system control register 2 (R53) VRR3 to VRR0	Power system control register 2 (R53) SVR3 to SVR0
Bias value	Power system control register 3 (R54) BIS2 to BIS0	Power system control register 3 (R54) SBIS to SBIS0
Number of boosting steps	Power system control register 4 (R55) MBT2 to MBT0	Power system control register 4 (R55) SBT2 to SBT0
Electronic volume	Main electronic volume register (R57)	Sub-electronic volume register (R58)
Grayscale data setting	Main R grayscale data register (R65 to R72) Main G grayscale data register (R73 to R80) Main B grayscale data register (R81 to R84)	Sub R grayscale data register (R85 to R92) Sub G grayscale data register (R93 to R100) Sub B grayscale data register (R101 to R104)

Default (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	**Note**	0	**Note**	0	0	0	0

Note 0 or 1

6.3 Reset Command Register (R3)

When this command is input, the registers of the μPD161401 (R0 to R104) are set to the default values.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0	1

Caution At power application, be sure to input the reset command as the first command.

6.4 X Address Register (R4)

The X address register specifies the X address of the display RAM the CPU accesses. This address is automatically incremented or decremented each time the display RAM has been accessed (INC = 0).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		XA6	XA5	XA4	XA3	XA2	XA1	XA0

Caution If the access direction is changed by control register 2 (R1: INC, XDIR, YDIR) or window access area is changed or set by MIN.·X address register (R7, R9) and MAX.·X address register (R8, R10), be sure to set the X address register (R4) and Y address register (R5) before accessing the display RAM.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.5 Y Address Register (R5)

The Y address register specifies the Y address of the display RAM the CPU accesses. This address is automatically incremented or decremented each time the display RAM is accessed (INC = 1).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		YA6	YA5	YA4	YA3	YA2	YA1	YA0

YA6 to YA0	Sets line address

Caution If the access direction is changed by control register 2 (R1: INC, XDIR, YDIR), be sure to set the X address register (R4) and Y address register (R5) before accessing the display RAM.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.6 MIN.·X Address Register (R7)

This register specifies the X address of the start point of the display RAM the CPU accesses when the window access mode is used.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		XMN6	XMN5	XMN4	XMN3	XMN2	XMN1	XMN0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.7 MAX.·X Address Register (R8)

This register specifies the X address of the end point of the display RAM the CPU accesses when the window access mode is used.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		XMX6	XMX5	XMX4	XMX3	XMX2	XMX1	XMX0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.8 MIN.·Y Address Register (R9)

This register specifies the Y address of the start point of the display RAM the CPU accesses when the window access mode is used.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		YMN6	YMN5	YMN4	YMN3	YMN2	YMN1	YMN0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.9 MAX.·Y Address Register (R10)

This register specifies the Y address of the end point of the display RAM the CPU accesses when the window access mode is used.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		YMX6	YMX5	YMX4	YMX3	YMX2	YMX1	YMX0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.10 Display Memory Access Register (R12)

The display memory access register is used to access the display RAM. When data is written to this register, it is directly written to the display RAM. In the μPD161401, the data of the display access memory register (R12) cannot be read.

BMOD = 1 (8-bit data bus)

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMOD = 0 (16-bit data bus)

RS	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
1	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Default value (default value of reset command)

BMOD = 1 (8-bit data bus)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**

Note 0 or 1

BMOD = 0 (16-bit data bus)

D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**

Note 0 or 1

6.11 Main Duty Setting Register (R14)

This register can set the display duty ratio in a range of 1/80, 1/72 and 1/64 duty as shown in **Table 6–5** in the main duty display mode.

Before changing the contents of this register, be sure to stop the internal operation by using the HALT command (control register 1 (R0)).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		MDT6	MDT5	MDT4	MDT3	MDT2	MDT1	MDT0

Table 6–5. Main Duty Setting Register (R14)

MDT6	MDT5	MDT4	MDT3	MDT2	MDT1	MDT0	Duty
1	0	0	1	1	1	1	1/80
1	0	0	0	1	1	1	1/72
0	1	1	1	1	1	1	1/64

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	1	0	0	1	1	1	1

Note 0 or 1

6.12 Main Duty N-line Inversion Register (R15)

This register can set the line position of AC driving in the main duty display mode as shown in **Table 6–6**.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1			MID5	MID4	MID3	MID2	MID1	MID0

Table 6–6. Setting of Main Duty N-line Inversion Register (R15)

MID5	MID4	MID3	MID2	MID1	MID0	Line to be reversed
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
		⋮				⋮
1	0	0	1	0	1	38
1	0	0	1	1	0	39
1	0	0	1	1	1	40

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	1	0	0	1	1	1

Note 0 or 1

6.13 Main Duty M-line Shift Register (R16)

This register shifts the reverse position of each frame in the main duty display mode by the shift amount shown in **Table 6–7**.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1			MSD5	MSD4	MSD3	MSD2	MSD1	MSD0

Table 6–7. Main Duty M-line Shift Register (R16)

MSD5	MSD4	MSD3	MSD2	MSD1	MSD0	Shift amount of position to be reversed
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
		⋮				⋮
1	0	0	1	1	0	38
1	0	0	1	1	1	39
1	0	1	0	0	0	40

Make sure that the relationship between the display size, reverse cycle, and reverse position is established as follows.

Display size (Duty) ≥ reverse cycle ≥ reverse shift amount

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	0	0	0	0	0	0

Note 0 or1

6.14 Sub-duty Setting Register (R17)

This register can set the display duty ratio in a range of 1/48, 1/40, 1/32, 1/24 and 1/16 as shown in **Table 6–8** in the sub-duty display mode by setting SDT6 to SDT0.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		SDT6	SDT5	SDT4	SDT3	SDT2	SDT1	SDT0

Table 6–8. Main Duty Setting Register (R17)

SDT6	SDT5	SDT4	SDT3	SDT2	SDT1	SDT0	Duty
0	1	0	1	1	1	1	1/48
0	1	0	0	1	1	1	1/40
0	0	1	1	1	1	1	1/32
0	0	1	0	1	1	1	1/24
0	0	0	1	1	1	1	1/16

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	1	0	1	1	1	1

Note 0 or 1

6.15 Sub-duty N-line Inversion Register (R18)

This register can set the line position of driving in the sub-duty display mode as shown in **Table 6–9**.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1			SID5	SID4	SID3	SID2	SID1	SID0

Table 6–9. Sub-duty N-line Inversion Register (R18)

SID5	SID4	SID3	SID2	SID1	SID0	Line to be reversed
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
		⋮				⋮
1	0	0	1	0	1	38
1	0	0	1	1	0	39
1	0	0	1	1	1	40

Caution Please protect the following relations.

Sub-duty display size (duty) ≥ sub-duty reversed line

If this relation is not protected, the operation is not guaranteed.

However, when the above-mentioned relation is not protected, inside μPD161401, processing which makes reversed line equal to display size is carried out. In addition, the value of a register is not rewritten automatically.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	1	0	0	1	1	1

Note 0 or 1

6.16 Sub-duty M-line Shift Register (R19)

This register shifts the reverse position of each frame in the sub-duty display mode by the shift amount shown in **Table 6–10**.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1			SSD5	SSD4	SSD3	SSD2	SSD1	SSD0

Table 6–10. Sub-duty M-line Shift Register (R19)

SSD5	SSD4	SSD3	SSD2	SSD1	SSD0	Shift amount of position to be reversed
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
		⋮				⋮
1	0	0	1	1	0	38
1	0	0	1	1	1	39
1	0	1	0	0	0	40

Make sure that the relationship between the display size, reverse cycle, and reverse position is established as follows.

Display size (duty) ≥ reverse cycle ≥ reverse shift amount

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	0	0	0	0	0	0

Note 0 or 1

6.17 COM Scanning Address Setting Register (R21)

This command specifies that scanning of the common outputs can be started from any of the On (n = 1 to 80) output pins. Set the CSA4 to CSA0 bits as shown in **Table 6–11 (1/2)**. The scan start pin can be specified by the value n obtained from this table and the selected duty shown in **Table 6–11 (2/2)**. The common wiring on the LCD panel can be optimized according to the selected duty.

Tables 6–12, **6–13**, and **6–14** indicate examples of the COM scan address settings for 1/64 duty, 1/72 duty, and 1/80 duty.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1				CSA4	CSA3	CSA2	CSA1	CSA0

Table 6–11. COM Scanning Address Setting Register (1/2)

CSA4	CSA3	CSA2	CSA1	CSA0	n
0	0	0	0	0	1
0	0	0	0	1	2
0	0	0	1	0	3
		⋮			⋮
0	1	1	1	0	15
0	1	1	1	1	16
1	0	0	0	0	17
1	0	0	0	1	Other settings prohibited

Table 6–11. COM Scanning Address Setting Register (2/2)

COMR = 0			COMR = 1		
Scanning start (COM1) pin	→	Scanning end (COMa) Note pin	Scanning start (COM1) pin	→	Scanning end (COMa) Note pin
On	→	O(n+a–1) Note	O(82–a–n)	→	O(80–n+1) Note

Note a = 64: 1/64 duty
a = 72: 1/72 duty
a = 80: 1/80 duty

Caution Set the COM scan address setting register so that the scan start pin and scan end pin satisfy the equation below. If a value that exceeds this condition is set, the μPD161401 operation is not guaranteed.

$O_1 \leq$ Scan start pin and scan end pin $\leq O_{80}$

Table 6–12. Example of COM Scanning Address Setting (1/64 duty)

CSA4	CSA3	CSA2	CSA1	CSA0	n	COMR = 0			COMR = 1		
						Scanning start (COM1) pin	→	Scanning end (COMa) Note pin	Scanning start (COM1) pin	→	Scanning end (COMa) Note pin
						On	→	O(n+a–1) Note	O(82–a–n)	→	O(80–n+1) Note
0	0	0	0	0	1	O_1	→	O_{64}	O_{17}	→	O_{80}
0	0	0	0	1	2	O_2	→	O_{65}	O_{16}	→	O_{79}
0	0	0	1	0	3	O_3	→	O_{66}	O_{15}	→	O_{78}
0	0	0	1	1	4	O_4	→	O_{67}	O_{14}	→	O_{77}
0	0	1	0	0	5	O_5	→	O_{68}	O_{13}	→	O_{76}
0	0	1	0	1	6	O_6	→	O_{69}	O_{12}	→	O_{75}
0	0	1	1	0	7	O_7	→	O_{70}	O_{11}	→	O_{74}
0	0	1	1	1	8	O_8	→	O_{71}	O_{10}	→	O_{73}
0	1	0	0	0	9	O_9	→	O_{72}	O_9	→	O_{72}
0	1	0	0	1	10	O_{10}	→	O_{73}	O_8	→	O_{71}
0	1	0	1	0	11	O_{11}	→	O_{74}	O_7	→	O_{70}
0	1	0	1	1	12	O_{12}	→	O_{75}	O_6	→	O_{69}
0	1	1	0	0	13	O_{13}	→	O_{76}	O_5	→	O_{68}
0	1	1	0	1	14	O_{14}	→	O_{77}	O_4	→	O_{67}
0	1	1	1	0	15	O_{15}	→	O_{78}	O_3	→	O_{66}
0	1	1	1	1	16	O_{16}	→	O_{79}	O_2	→	O_{65}
1	0	0	0	0	17	O_{17}	→	O_{80}	O_1	→	O_{64}

Note a = 64 at 1/64 duty

Table 6–13. Example of COM Scanning Address Setting (1/72 duty)

CSA4	CSA3	CSA2	CSA1	CSA0	n	COMR = 0			COMR = 1			Remark
						Scanning start (COM1) pin	→	Scanning end (COMa) Note pin	Scanning start (COM1) pin	→	Scanning end (COMa) Note pin	
						On	→	O(n+a–1) Note	O(82–a–n)	→	O(80–n+1) Note	
0	0	0	0	0	1	O_1	→	O_{72}	O_9	→	O_{80}	
0	0	0	0	1	2	O_2	→	O_{73}	O_8	→	O_{79}	
0	0	0	1	0	3	O_3	→	O_{74}	O_7	→	O_{78}	
0	0	0	1	1	4	O_4	→	O_{75}	O_6	→	O_{77}	
0	0	1	0	0	5	O_5	→	O_{76}	O_5	→	O_{76}	
0	0	1	0	1	6	O_6	→	O_{77}	O_4	→	O_{75}	
0	0	1	1	0	7	O_7	→	O_{78}	O_3	→	O_{74}	
0	0	1	1	1	8	O_8	→	O_{79}	O_2	→	O_{73}	
0	1	0	0	0	9	O_9	→	O_{80}	O_1	→	O_{72}	
0	1	0	0	1	10							Other settings prohibited

Note a = 72 at 1/72 duty

Caution Set the COM scan address setting register (R21) so that $O_1 \leq$ scan start pin and scan end pin $\leq O_{80}$. If a value that exceeds this condition is set, the μPD161401 operation is not guaranteed

Table 6–14. Example of COM Scanning Address Setting (1/80 duty)

CSA4	CSA3	CSA2	CSA1	CSA0	n	COMR = 0			COMR = 1			Remark
						Scanning start (COM1) pin	→	Scanning end (COMa) Note pin	Scanning start (COM1) pin	→	Scanning end (COMa) Note pin	
						On	→	O(n+a–1) Note	O(82–a–n)	→	O(80–n+1) Note	
0	0	0	0	0	1	O_1	→	O_{80}	O_1	→	O_{80}	
0	0	0	0	1	2							Other settings prohibited

Note a = 80 at 1/80 duty

Caution When the μPD161401 is used in 1/80 duty, set the COM scan address setting register (R21) to CSA4, CSA3, CSA2, CSA1, CSA0 = 0, 0, 0, 0, 0. If any other settings are made, the μPD161401 operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

6.18 Sub-duty Start Address Register (R22)

The sub-duty start address register specifies the start address of the display RAM the CPU accesses to use the sub-duty display mode. The sub-duty display area starts from this start line address and consists of the number of lines specified by the sub-duty setting register (R17).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0

Table 6–15. Sub-duty Start Address Register

SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	Common
0	0	0	0	0	0	0	COM_1
0	0	0	0	0	0	1	COM_2
0	0	0	0	0	1	0	COM_3
0	0	0	0	0	1	1	COM_4
			⋮				⋮
1	0	0	1	1	0	1	COM_{78}
1	0	0	1	1	1	0	COM_{79}
1	0	0	1	1	1	1	COM_{80}

Make sure that SSA (R22) and SDT (R17) have in the following relationship.

SSAn + SDTn ≤ MDT ≤ 4FH

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.19 Scroll Fixed Area Position Register (R23)

This command specifies the display position of the scroll fixed area to upper or bottom of side in LCD panel.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1								FIXAHL

Table 6–16. Scroll Fixed Position Register (R23)

FIXAHL	Display Position
0	bottom
1	upper

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	1

Note 0 or 1

6.20 Scroll Fixed Area Width Register (R27)

This register selects the width of the area to be fixed from 0, 16, 24, and 32 lines.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1							FIXAW1	FIXAW0

Table 4–16. Scroll Fixed Area Width Register (R27)

FIXAW1	FIXAW0	Fixed Area Width
0	0	0
0	1	16
1	0	24
1	1	32

Even if the screen display size is changed by the duty setting register (R14 and R17), FIXAW1 and FIXAW0 are not overwritten.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	0	0

Note 0 or 1

6.21 Scroll Step Number Register (R31)

This register sets the number of scroll steps when the scroll function is used.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		MST6	MST5	MST4	MST3	MST2	MST1	MST0

Table 6–18. Scroll Step Number Register (R31)

MST6	MST5	MST4	MST3	MST2	MST1	MST0	Number of Scroll Steps
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
			⋮				⋮
1	0	0	1	1	0	1	77
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79
1	0	1	0	0	0	0	Other settings prohibited

Caution The relationship between the number of scroll steps and scroll fixed area width should be as follows.

Number of scroll steps ≤ 79 – Scroll fixed area width

If values exceeding the above condition are set, the operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.22 Blink/Reverse Setting Register (R37)

This register controls blink display or reverse display. Blink display is controlled by the BLD1 and BLD0 flags of this register, and reverse display is controlled by the INV flag, as shown in the table below.

The condition of each of the blink and reverse display areas is individually set by R38 to R50.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1					INV		BLD1	BLD0

Table 6–19. Blink/Reverse Display Control

INV	Display
0	Reverse display OFF
1	Reverse display ON

BLD1	Display
0	Specified-color blink display OFF
1	Specified-color blink display ON

BLD0	Display
0	Complementary-color blink display OFF
1	Complementary-color blink display ON

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	0	**Note**	0	0

Note 0 or 1

6.23 Complementary Color Blink X Address Register (R38)

The complementary color blink X address register specifies the X address of the complementary color blink RAM the CPU accesses. This address is automatically incremented each time the complementary color blink data RAM is accessed.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1					CBX3	CBX2	CBX1	CBX0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	0	0	0	0

Note 0 or 1

6.24 Complementary Color Blink Start Line Address Register (R39)

The complementary color blink start line address register specifies the start line address the CPU accesses to use complementary color blinking display. The range of the complementary color blink lines is determined by this register and the complementary color blink end line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		CBS6	CBS5	CBS4	CBS3	CBS2	CBS1	CBS0	

CBS6 to CBS0	Sets a start line address

Caution Make sure that CBS [6:0] ≤ 4FH. If 4FH is exceeded, operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.25 Complementary Color Blink End Line Address Register (R40)

The complementary color blink end line address register specifies the end line address the CPU accesses to use complementary color blink display. The range of the complementary color blink lines is determined by this register and the complementary color blink start line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		CBE6	CBE5	CBE4	CBE3	CBE2	CBE1	CBE0	

CBE6 to CBE0	Sets an end line address

Caution Make sure that CBE [6:0] ≤ 4FH. If 4FH is exceeded, operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.26 Complementary Color Blink Data Memory Register (R41)

The complementary color blink data memory register is used to access the complementary color blink data RAM.

If this register is accessed for write, data is directly written to the complementary color blink data RAM.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Data	Status
0	Normal
1	Complementary color blinking

Default value (default value of reset command, all data)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**

Note 0 or 1

6.27 Specified Color Blink X Address Register (R42)

The specified color blink X address register specifies the X address of the specified color blinking RAM the CPU accesses. This address is automatically incremented each time the specified color blink data RAM is accessed.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1					SBX3	SBX2	SBX1	SBX0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	0	0	0	0

Note 0 or 1

6.28 Specified Color Blink Start Line Address Register (R43)

The specified color blink start line address register specifies the start line address the CPU accesses to use specified color blinking display. The range of the specified color blink lines is determined by this register and the specified color blinking end line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		SBS6	SBS5	SBS4	SBS3	SBS2	SBS1	SBS0	

SBS6 to SBS0	Sets a start line address.

Caution Make sure that SBS [6:0] ≤ 4FH. If 4FH is exceeded, operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.29 Specified Color Blink End Line Address Register (R44)

The specified color blink end line address register specifies the end line address the CPU accesses to use specified color blink display. The range of the specified color blink lines is determined by this register and the specified color blink start line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		SBE6	SBE5	SBE4	SBE3	SBE2	SBE1	SBE0	

SBE6 to SBE0	Sets an end line address.

Caution Make sure that SBE [6:0] ≤ 4FH. If 4FH is exceeded, operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.30 Specified Color Blink Data Memory Register (R45)

The specified color blink data memory register is used to access the specified color blink data RAM. If this register is accessed for write, data is directly written to the specified color blink data RAM.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Data	Status
0	Normal
1	Specified color blinking

Default value (default value of reset command, all data)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**

Note 0 or 1

6.31 Specified Color Setting Register (R46)

This register sets specified color data when the specified color blink function is used. The data between this data and the display RAM data blinks in a specified color.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remark
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
	R			G			B		In 256-color mode

Default value (default value of reset command, all data)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.32 Reverse X Address Register (R47)

The reverse X address register specifies the X address of the reverse data RAM the CPU accesses. This address is incremented each time the reverse RAM has been accessed.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1					IVX3	IVX2	IVX1	IVX0

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	0	0	0	0

Note 0 or 1

6.33 Reverse Start Line Address Register (R48)

The reverse start line address register specifies start line address of the display RAM the CPU accesses for reverse display. The range of the reverse lines is determined by this register and the reverse end line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1		IVS6	IVS5	IVS4	IVS3	IVS2	IVS1	IVS0

IVS6 to IVS0	Sets a start line address.

Caution Make sure that IVS [6:0] ≤ 4FH. If 4FH is exceeded, operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.34 Reverse End Line Address Register (R49)

The reverse end line address register specifies the end line address of the display RAM the CPU accesses for reverse display. The range of the reverse lines is determined by this register and the reverse start line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		IVE6	IVE5	IVE4	IVE3	IVE2	IVE1	IVE0	

IVE6 to IVE0	Sets an end line address.

Caution Make sure that IVE [6:0] ≤ 4FH. If 4FH is exceeded, operation is not guaranteed.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.35 Reverse Data Memory Access Register (R50)

The reverse data memory access register is used to access the reverse data RAM. When this register is accessed for write, data is directly written to the reverse data RAM.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	

Data	Status
0	Normal
1	Reverse

Default value (default value of reset command, all data)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**

Note 0 or 1

6.36 Power System Control Register 1 (R52)

This command sets the power system mode of the μPD161401.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0		TCS2	TCS1	TCS0	OP3	OP2	OP1	OP0

TCS2 to TCS0	These bits set the value that selects the temperature curve of the V_{REG} voltage to a value shown in **Table 6–20**.
OP3 to OP0	These bits turn ON/OFF the booster circuit, reference voltage generator, control the voltage regulator circuit (V regulator circuit) and voltage follower circuit (V/F circuit). The functions controlled by these four-power control set command controlled by these 4 bits are listed in **Table 6–21**.

Table 6–20. V_{REG} Voltage Temperature Curve Value

TCS2	TCS1	TCS0	Status	Temperature Gradient (unit: %/°C)	V_{REG} (TYP.) (unit: V)
0	0	0	Internal power supply	–0.12	1.77
0	0	1		–0.13	1.69
0	1	0		–0.15	1.63
0	1	1		–0.17	1.59
1	X	X	When external reference power supply is used	–	–

Table 6–21. Details of Control by Each Bit of Power System Control Register

Item		Status 1	Status 0
OP3	: Booster circuit control bit	ON	OFF
OP2	: Reference voltage generator control bit	ON	OFF
OP1	: Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
OP0	: Voltage follower circuit (V/F circuit) control bit	ON	OFF

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.37 Power System Control Register 2 (R53)

This command sets the power system mode of the μPD161401.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	1	0	VRR3	VRR2	VRR1	VRR0	SVR3	SVR2	SVR1	SVR0	

VRR3 to VRR0	When the main duty display mode is used, the resistance ratio can be changed in 16 steps by the V_{LCD} internal resistance ratio adjustment command. Four bits of the V_{LCD} internal resistance ratio adjustment register set the reference value of (1 + Rb/Ra) to the value shown in **Table 6–22**.
SVR3 to SVR0	When the sub-duty display mode is used, the resistance ratio can be changed in 16 steps by the V_{LCD} internal resistance ratio adjustment command. Four bits of the V_{LCD} internal resistance ratio adjustment register set the reference value of (1 + Rb/Ra) to the value shown in **Table 6–22**.

Table 6-22. VLCD Internal Resistance Ratio Adjustment Register

Register				1 + Rb/Ra
VRR3	VRR2	VRR1	VRR0	
SVR3	SVR2	SVR1	SVR0	
0	0	0	0	3
0	0	0	1	4
0	0	1	0	5
0	0	1	1	6
0	1	0	0	7
0	1	0	1	8
0	1	1	0	9
0	1	1	1	10
1	0	0	0	11
1	0	0	1	12
1	0	1	0	13
1	0	1	1	14
1	1	0	0	15
1	1	0	1	16
1	1	1	0	17
1	1	1	1	18

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

6.38 Power System Control Register 3 (R54)

This command sets the bias value for main duty display and sub-duty display by the μPD161401.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		BIS2	BIS1	BIS0		SBIS2	SBIS1	SBIS0	

BIS2 to BIS0 **Note**	These flags select the bias ratio in the main duty display mode as follows:			
	BIS2	BIS1	BIS0	Bias Ratio
	0	0	0	1/9 bias
	0	0	1	1/8 bias
	0	1	0	1/7 bias
	0	1	1	1/6 bias
	1	0	0	1/5 bias
	1	0	1	Prohibited
	1	1	0	Prohibited
	1	1	1	Prohibited
SBIS2 to SBIS0 **Note**	These flags select the bias ratio in the sub-duty display mode as follows:			
	SBIS2	SBIS1	SBIS0	Bias Ratio
	0	0	0	1/9 bias
	0	0	1	1/8 bias
	0	1	0	1/7 bias
	0	1	1	1/6 bias
	1	0	0	1/5 bias
	1	0	1	Prohibited
	1	1	0	Prohibited
	1	1	1	Prohibited

Note Before changing these flags, execute the HALT command.

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	**Note**	0	0	0

Note 0 or 1

6.39 Power System Control Register 4 (R55)

This command sets the number of boosting steps for main duty display and sub-duty display of μPD161401 as shown in **Table 6–23**.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		MBT2	MBT1	MBT0		SBT2	SBT1	SBT0	

Table 6–23. Number of Boosting Steps for Main/Sub-duty Display of Booster Circuit

MBT2	MBT1	MBT0	Number of Boosting Steps (unit: fold)
SBT2	SBT1	SBT0	
0	0	0	Two
0	0	1	Three
0	1	0	Four
0	1	1	Five
1	0	0	Six
1	0	1	Seven
1	1	0	Prohibited
1	1	1	Prohibited

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	**Note**	0	0	0

Note 0 or 1

6.40 Power System Control Register 5 (R56)

This command sets the status of the voltage follower circuit of the μPD161401 that drives the LCD, as follows:

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	LCS1	LCS0	LCC1	LCC0	HPM1	HPM0	PSM1	PSM0	

Table 6–24. Setting of Segment Output Driving Capability (LCS1, LCS0 = 0, 0)

LCS1	LCS0	Segment Output Driving Capability (unit: fold)
0	0	One
0	1	Two
1	0	Four
1	1	Eight

Table 6–25. Setting of Common Output Driving Capability (LCS1, LCS0 = 0, 0)

LCC1	LCC0	Common Output Driving Capability (unit: fold)
0	0	Two
0	1	Four
1	0	Eight
1	1	Sixteen

Table 6–26. Setting of Operational Amplifier Operation Mode

HPM1	HPM0	Mode Setting
0	0	Normal mode
0	1	Power ON mode1
1	0	Power OFF mode
1	1	Power ON mode2

Table 6–27. Setting of Two-fold Supply Voltage (V_{LC3}, V_{LC4} Level Voltage Follower Power Supply)

PSM1	Mode Setting
0	Not used
1	used

Table 6–28. Setting of Voltage Follower Bias Current

PSM0	Bias Current Setting (unit: fold)
0	One
1	Two

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	0	1	0

6.41 Main Electronic Volume Register (R57)

The main electronic volume register specifies the electronic volume value for adjusting the contrast in the main duty display mode, in 128 steps.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		MEV6	MEV5	MEV4	MEV3	MEV2	MEV1	MEV0	

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.42 Sub-electronic Volume Register (R58)

The sub-electronic volume register specifies an electronic volume value for adjusting the contrast in the sub-duty display mode, in 128 steps.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1		SEV6	SEV5	SEV4	SEV3	SEV2	SEV1	SEV0	

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	0	0	0	0	0	0	0

Note 0 or 1

6.43 RAM Test Mode Setting Register (R61)

The RAM test mode setting register directly writes the data of each display status to the display RAM as shown in **Table 6–29**.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1						RTS2	RTS1	RTS0

Table 6–29. RAM Test Mode

RTS2	RTS1	RTS0	Write Data
0	0	0	Normal operation
0	0	1	all [00000000] / pixel display
0	1	0	all [11111111] / pixel display
0	1	1	Checker pattern display of [00000000] / [11111111]
1	0	0	Vertical grayscale bar display
1	0	1	Horizontal grayscale bar display
1	1	0	Each color grayscale display
1	1	1	256-color display

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	**Note**	0	0	0

Note 0 or 1

6.44 Driving Mode Select Register (R64)

The FXOR flag of the drive mode select register controls the reversal of the LCD drive waveform between frames as shown in **Table 6–30**. Note that the reverse function is executed between frames regardless of the FXOR flag during sub-duty display.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1					FXOR			

Table 6–30. Driving Mode Select Register (R64)

FXOR	Reversing Between Frames
0	OFF
1	ON

Default value (default value of reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	**Note**	0	**Note**	**Note**	**Note**

Note 0 or 1

6.45 Main R Grayscale Data Registers (R65 to R72)

The main R grayscale data registers specify the grayscale level of the R output in the main duty display mode. By using these registers, grayscale display can be optimized.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R65	0, 0, 0	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R66	0, 0, 1	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R67	0, 1, 0	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R68	0, 1, 1	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R69	1, 0, 0	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R70	1, 0, 1	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R71	1, 1, 0	1				MRG4	MRG3	MRG2	MRG1	MRG0	
R72	1, 1, 1	1				MRG4	MRG3	MRG2	MRG1	MRG0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Grayscale Level
×	×	×	0	0	0	0	0	Level 0
×	×	×	0	0	0	0	1	Level 1
×	×	×	0	0	0	1	0	Level 2
×	×	×	0	0	0	1	1	Level 3
			⋮					⋮
×	×	×	0	1	1	1	1	Level 15
×	×	×	1	0	0	0	0	Level 16

Default value (default value of reset command, common to all grayscale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

6.46 Main G Grayscale Data Registers (R73 to R80)

The main G grayscale data registers specify the grayscale level of the G output in the main duty display mode. By using these registers, grayscale display can be optimized.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R73	0, 0, 0	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R74	0, 0, 1	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R75	0, 1, 0	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R76	0, 1, 1	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R77	1, 0, 0	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R78	1, 0, 1	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R79	1, 1, 0	1				MGG4	MGG3	MGG2	MGG1	MGG0	
R80	1, 1, 1	1				MGG4	MGG3	MGG2	MGG1	MGG0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Grayscale Level
×	×	×	0	0	0	0	0	Level 0
×	×	×	0	0	0	0	1	Level 1
×	×	×	0	0	0	1	0	Level 2
×	×	×	0	0	0	1	1	Level 3
			⋮					⋮
×	×	×	0	1	1	1	1	Level 15
×	×	×	1	0	0	0	0	Level 16

Default value (default value of reset command, common to all grayscale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

6.47 Main B Grayscale Data Registers (R81 to R84)

The main B grayscale data registers specify the grayscale level of the B output in the main duty display mode. By using these registers, grayscale display can be optimized.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R81	0, 0	1				MBG4	MBG3	MBG2	MBG1	MBG0	
R82	0, 1	1				MBG4	MBG3	MBG2	MBG1	MBG0	
R83	1, 0	1				MBG4	MBG3	MBG2	MBG1	MBG0	
R84	1, 1	1				MBG4	MBG3	MBG2	MBG1	MBG0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Grayscale Level
×	×	×	0	0	0	0	0	Level 0
×	×	×	0	0	0	0	1	Level 1
×	×	×	0	0	0	1	0	Level 2
×	×	×	0	0	0	1	1	Level 3
			⋮					⋮
×	×	×	0	1	1	1	1	Level 15
×	×	×	1	0	0	0	0	Level 16

Default value (default value of reset command, common to all grayscale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

6.48 Sub R Grayscale Data Registers (R85 to R92)

The sub R grayscale data registers specify the grayscale level of the R output in the sub-duty display mode. By using these registers, grayscale display can be optimized.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R85	0, 0, 0	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R86	0, 0, 1	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R87	0, 1, 0	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R88	0, 1, 1	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R89	1, 0, 0	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R90	1, 0, 1	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R91	1, 1, 0	1				SRG4	SRG3	SRG2	SRG1	SRG0	
R92	1, 1, 1	1				SRG4	SRG3	SRG2	SRG1	SRG0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Grayscale Level
×	×	×	0	0	0	0	0	Level 0
×	×	×	0	0	0	0	1	Level 1
×	×	×	0	0	0	1	0	Level 2
×	×	×	0	0	0	1	1	Level 3
			⋮					⋮
×	×	×	0	1	1	1	1	Level 15
×	×	×	1	0	0	0	0	Level 16

Default value (default value of reset command, common to all grayscale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

6.49 Sub G Grayscale Data Registers (R93 to R100)

The sub G grayscale data registers specify the grayscale level of the G output in the sub-duty display mode. By using these registers, grayscale display can be optimized.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R93	0, 0, 0	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R94	0, 0, 1	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R95	0, 1, 0	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R96	0, 1, 1	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R97	1, 0, 0	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R98	1, 0, 1	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R99	1, 1, 0	1				SGG4	SGG3	SGG2	SGG1	SGG0	
R100	1, 1, 1	1				SGG4	SGG3	SGG2	SGG1	SGG0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Grayscale Level
×	×	×	0	0	0	0	0	Level 0
×	×	×	0	0	0	0	1	Level 1
×	×	×	0	0	0	1	0	Level 2
×	×	×	0	0	0	1	1	Level 3
			⋮					⋮
×	×	×	0	1	1	1	1	Level 15
×	×	×	1	0	0	0	0	Level 16

Default value (default value of reset command, common to all grayscale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

6.50 Sub B Grayscale Data Registers (R101 to R104)

The sub B grayscale data registers specify the grayscale level of the B output in the sub-duty display mode. By using these registers, grayscale display can be optimized.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R101	0, 0	1				SBG4	SBG3	SBG2	SBG1	SBG0	
R102	0, 1	1				SBG4	SBG3	SBG2	SBG1	SBG0	
R103	1, 0	1				SBG4	SBG3	SBG2	SBG1	SBG0	
R104	1, 1	1				SBG4	SBG3	SBG2	SBG1	SBG0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Grayscale Level
×	×	×	0	0	0	0	0	Level 0
×	×	×	0	0	0	0	1	Level 1
×	×	×	0	0	0	1	0	Level 2
×	×	×	0	0	0	1	1	Level 3
			⋮					⋮
×	×	×	0	1	1	1	1	Level 15
×	×	×	1	0	0	0	0	Level 16

Default value (default value of reset command, common to all grayscale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Note	**Note**	**Note**	0	0	0	0	0

Note 0 or 1

7. μPD161401 REGISTER LIST

(1/2)

CS	RS	Index Register								Register Name	R/W	Data Bit							
		6	5	4	3	2	1	0				7	6	5	4	3	2	1	0
1																			
0	0								IR	Index Register	W		IR6	IR5	IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	0	0	R0	Control Register 1	R/W	TRON	WAS	COMF	DISP	STBY	HALT	ADC	COMR
0	1	0	0	0	0	0	0	1	R1	Control Register 2	R/W	FDM		BMOD		DTY	INC	XDIR	YDIR
0	1	0	0	0	0	0	1	0	R2										
0	1	0	0	0	0	0	1	1	R3	Reset Command	W								RES
0	1	0	0	0	0	1	0	0	R4	X Address Register	R/W		XA6	XA5	XA4	XA3	XA2	XA1	XA0
0	1	0	0	0	0	1	0	1	R5	Y Address Register	R/W		YA6	YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	0	0	1	1	0	R6										
0	1	0	0	0	0	1	1	1	R7	MIN.·X Address Register	R/W		XMN6	XMN5	XMN4	XMN3	XMN2	XMN1	XMN0
0	1	0	0	0	1	0	0	0	R8	MAX. X Address Register	R/W		XMX6	XMX5	XMX4	XMX3	XMX2	XMX1	XMX0
0	1	0	0	0	1	0	0	1	R9	MIN. Y Address Register	R/W		YMN6	YMN5	YMN4	YMN3	YMN2	YMN1	YMN0
0	1	0	0	0	1	0	1	0	R10	MAX. Y Address Register	R/W		YMX6	YMX5	YMX4	YMX3	YMX2	YMX1	YMX0
0	1	0	0	0	1	0	1	1	R11										
0	1	0	0	0	1	1	0	0	R12	Display Memory Access Register	W	D15	D14	D13	D15	D11	D10	D9	D8
												D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	1	R13										
0	1	0	0	0	1	1	1	0	R14	Main Duty Setting Register	R/W		MDT6	MDT5	MDT4	MDT3	MDT2	MDT1	MDT0
0	1	0	0	0	1	1	1	1	R15	Main Duty N-line Inversion Register	R/W			MID5	MID4	MID3	MID2	MID1	MID0
0	1	0	0	1	0	0	0	0	R16	Main Duty M-line Shift Register	R/W			MSD5	MSD4	MSD3	MSD2	MSD1	MSD0
0	1	0	0	1	0	0	0	1	R17	Sub-duty Setting Register	R/W		SDT6	SDT5	SDT4	SDT3	SDT2	SDT1	SDT0
0	1	0	0	1	0	0	1	0	R18	Sub-duty N-line Inversion Register	R/W			SID5	SID4	SID3	SID2	SID1	SID0
0	1	0	0	1	0	0	1	1	R19	Sub-duty M-line Shift Register	R/W			SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
0	1	0	0	1	0	1	0	0	R20										
0	1	0	0	1	0	1	0	1	R21	COM Scanning Address Setting Register	R/W				CSA4	CSA3	CSA2	CSA1	CSA0
0	1	0	0	1	0	1	1	0	R22	Sub-duty Start Address Register	R/W		SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
0	1	0	0	1	0	1	1	1	R23	Scroll Fixed Area Position Register	R/W								FIXAHL
0	1	0	0	1	1	0	0	0	R24										
0	1	0	0	1	1	0	0	1	R25										
0	1	0	0	1	1	0	1	0	R26										
0	1	0	0	1	1	0	1	1	R27	Scroll Fixed Area Width Register	R/W							FIXAW1	FIXAW0
0	1	0	0	1	1	1	0	0	R28										
0	1	0	0	1	1	1	0	1	R29										
0	1	0	0	1	1	1	1	0	R30										
0	1	0	0	1	1	1	1	1	R31	Scroll Step Number Register	R/W		MST6	MST5	MST4	MST3	MST2	MST1	MST0
0	1	0	1	0	0	0	0	0	R32										
0	1	0	1	0	0	0	0	1	R33										
0	1	0	1	0	0	0	1	0	R34										
0	1	0	1	0	0	0	1	1	R35										
0	1	0	1	0	0	1	0	0	R36										
0	1	0	1	0	0	1	0	1	R37	Blink/Reverse Setting Register	R/W					INV		BLD1	BLD0
0	1	0	1	0	0	1	1	0	R38	Complementary Color Blink X Address Register	R/W					CBX3	CBX2	CBX1	CBX0
0	1	0	1	0	0	1	1	1	R39	Complementary Color Blink Start Line Address Register	R/W		CBS6	CBS5	CBS4	CBS3	CBS2	CBS1	CBS0
0	1	0	1	0	1	0	0	0	R40	Complementary Color Blink End Line Address Register	R/W		CBE6	CBE5	CBE4	CBE3	CBE2	CBE1	CBE0
0	1	0	1	0	1	0	0	1	R41	Complementary Color Blink Data Memory Register	W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	R42	Specified Color Blinking X Address Register	R/W					SBX3	SBX2	SBX1	SBX0
0	1	0	1	0	1	0	1	1	R43	Specified Color Blink Start Line Address Register	R/W		SBS6	SBS5	SBS4	SBS3	SBS2	SBS1	SBS0
0	1	0	1	0	1	1	0	0	R44	Specified Color Blink End Line Address Register	R/W		SBE6	SBE5	SBE4	SBE3	SBE2	SBE1	SBE0
0	1	0	1	0	1	1	0	1	R45	Specified Color Blink Data Memory Register	W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	0	R46	Specified Color Setting Register	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	1	R47	Reverse X Address Register	R/W					IVX3	IVX2	IVX1	IVX0
0	1	0	1	1	0	0	0	0	R48	Reverse Start Line Address Register	R/W		IVS6	IVS5	IVS4	IVS3	IVS2	IVS1	IVS0
0	1	0	1	1	0	0	0	1	R49	Reverse End Line Address Register	R/W		IVE6	IVE5	IVE4	IVE3	IVE2	IVE1	IVE0
0	1	0	1	1	0	0	1	0	R50	Reverse Data Memory Access Register	W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	1	1	R51										
0	1	0	1	1	0	1	0	0	R52	Power System Control Register 1	R/W		TCS2	TCS1	TCS0	OP3	OP2	OP1	OP0
0	1	0	1	1	0	1	0	1	R53	Power System Control Register 2	R/W	VRR3	VRR2	VRR1	VRR0	SVR3	SVR2	SVR1	SVR0
0	1	0	1	1	0	1	1	0	R54	Power System Control Register 3	R/W		BIS2	BIS1	BIS0		SBIS2	SBIS1	SBIS0
0	1	0	1	1	0	1	1	1	R55	Power System Control Register 4	R/W		MBT2	MBT1	MBT0		SBT2	SBT1	SBT0
0	1	0	1	1	1	0	0	0	R56	Power System Control Register 5	R/W	LCS1	LCS0	LCC1	LCC0	HPM1	HPM0	PSM1	PSM0
0	1	0	1	1	1	0	0	1	R57	Main Electronic Volume Register	R/W		MEV6	MEV5	MEV4	MEV3	MEV2	MEV1	MEV0
0	1	0	1	1	1	0	1	0	R58	Sub-electronic Volume Register	R/W		SEV6	SEV5	SEV4	SEV3	SEV2	SEV1	SEV0
0	1	0	1	1	1	0	1	1	R59										
0	1	0	1	1	1	1	0	0	R60										
0	1	0	1	1	1	1	0	1	R61	RAM Test Mode Setting Register	R/W						RTS2	RST1	RST0
0	1	0	1	1	1	1	1	0	R62										
0	1	0	1	1	1	1	1	1	R63										

(2/2)

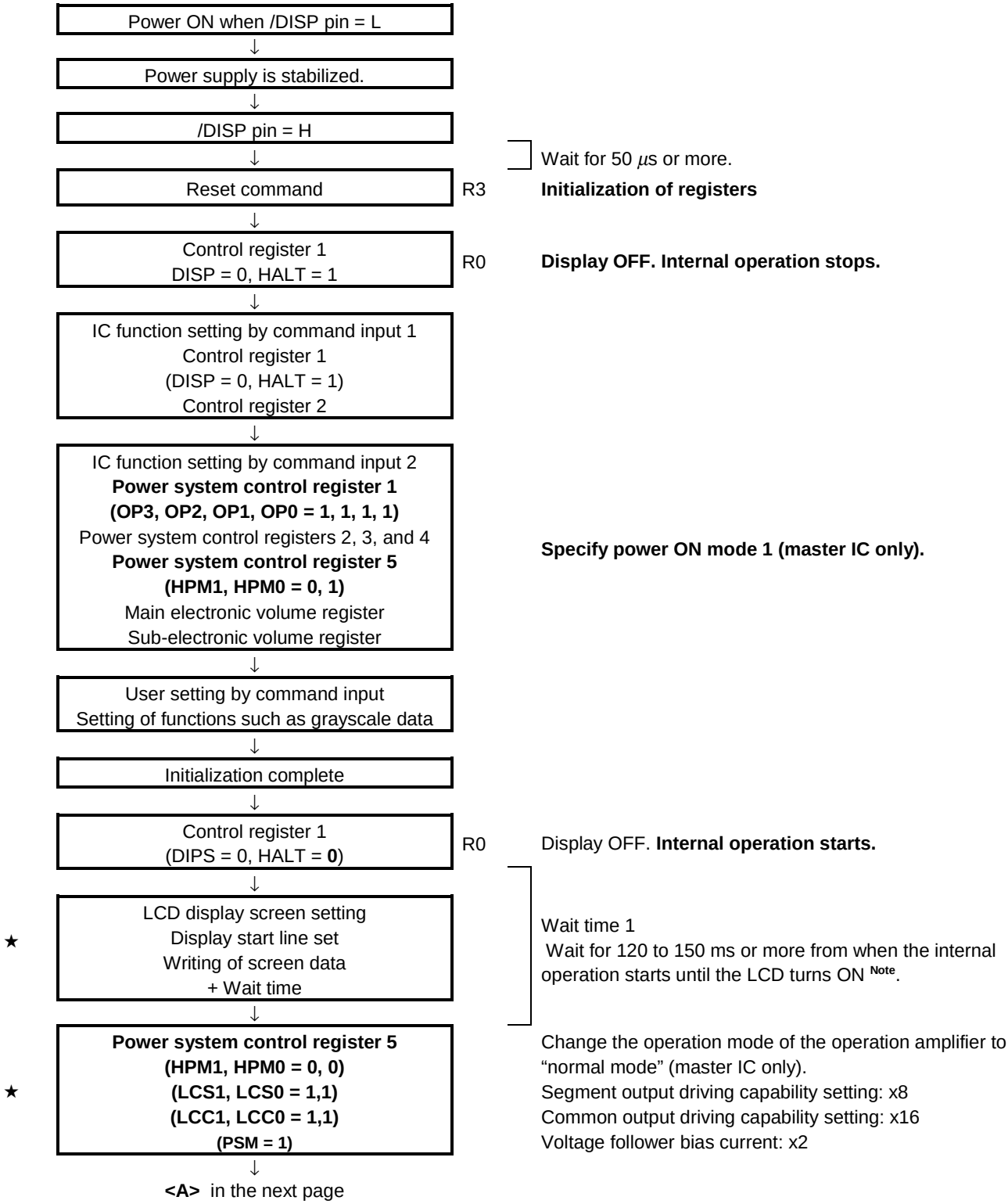
CS	RS	Index Register								Register Name	R/W	Data Bit							
		6	5	4	3	2	1	0				7	6	5	4	3	2	1	0
1																			
0	0								IR										
0	1	1	0	0	0	0	0	0	R64	Driving Mode Select Register						FXOR			
0	1	1	0	0	0	0	0	1	R65	Main R Grayscale Data Register 1 (0, 0, 0)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	0	0	1	0	R66	Main R Grayscale Data Register 2 (0, 0, 1)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	0	0	1	1	R67	Main R Grayscale Data Register 3 (0, 1, 0)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	0	1	0	0	R68	Main R Grayscale Data Register 4 (0, 1, 1)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	0	1	0	1	R69	Main R Grayscale Data Register 5 (1, 0, 0)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	0	1	1	0	R70	Main R Grayscale Data Register 6 (1, 0, 1)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	0	1	1	1	R71	Main R Grayscale Data Register 7 (1, 1, 0)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	1	0	0	0	R72	Main R Grayscale Data Register 8 (1, 1, 1)					MRG4	MRG3	MRG2	MRG1	MRG0
0	1	1	0	0	1	0	0	1	R73	Main G Grayscale Data Register 1 (0 ,0, 0)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	0	1	0	1	0	R74	Main G Grayscale Data Register 2 (0, 0, 1)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	0	1	0	1	1	R75	Main G Grayscale Data Register 3 (0, 1, 0)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	0	1	1	0	0	R76	Main G Grayscale Data Register 4 (0, 1, 1)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	0	1	1	0	1	R77	Main G Grayscale Data Register 5 (1, 0, 0)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	0	1	1	1	0	R78	Main G Grayscale Data Register 6 (1, 0, 1)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	0	1	1	1	1	R79	Main G Grayscale Data Register 7 (1, 1, 0)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	1	0	0	0	0	R80	Main G Grayscale Data Register 8 (1, 1, 1)					MGG4	MGG3	MGG2	MGG1	MGG0
0	1	1	0	1	0	0	0	1	R81	Main B Grayscale Data Register 1 (0, 0)					MBG4	MBG3	MBG2	MBG1	MBG0
0	1	1	0	1	0	0	1	0	R82	Main B Grayscale Data Register 2 (0, 1)					MBG4	MBG3	MBG2	MBG1	MBG0
0	1	1	0	1	0	0	1	1	R83	Main B Grayscale Data Register 3 (1, 0)					MBG4	MBG3	MBG2	MBG1	MBG0
0	1	1	0	1	0	1	0	0	R84	Main B Grayscale Data Register 4 (1, 1)					MBG4	MBG3	MBG2	MBG1	MBG0
0	1	1	0	1	0	1	0	1	R85	Sub R Grayscale Data Register 1 (0, 0, 0)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	0	1	1	0	R86	Sub R Grayscale Data Register 2 (0, 0, 1)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	0	1	1	1	R87	Sub R Grayscale Data Register 3 (0, 1, 0)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	1	0	0	0	R88	Sub R Grayscale Data Register 4 (0, 1, 1)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	1	0	0	1	R89	Sub R Grayscale Data Register 5 (1, 0, 0)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	1	0	1	0	R90	Sub R Grayscale Data Register 6 (1, 0, 1)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	1	0	1	1	R91	Sub R Grayscale Data Register 7 (1, 1, 0)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	1	1	0	0	R92	Sub R Grayscale Data Register 8 (1, 1, 1)					SRG4	SRG3	SRG2	SRG1	SRG0
0	1	1	0	1	1	1	0	1	R93	Sub G Grayscale Data Register 1 (0, 0, 0)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	0	1	1	1	1	0	R94	Sub G Grayscale Data Register 2 (0, 0, 1)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	0	1	1	1	1	1	R95	Sub G Grayscale Data Register 3 (0, 1, 0)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	1	0	0	0	0	0	R96	Sub G Grayscale Data Register 4 (0, 1, 1)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	1	0	0	0	0	1	R97	Sub G Grayscale Data Register 5 (1, 0, 0)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	1	0	0	0	1	0	R98	Sub G Grayscale Data Register 6 (1, 0, 1)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	1	0	0	0	1	1	R99	Sub G Grayscale Data Register 7 (1, 1, 0)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	1	0	0	1	0	0	R100	Sub G Grayscale Data Register 8 (1, 1, 1)					SGG4	SGG3	SGG2	SGG1	SGG0
0	1	1	1	0	0	1	0	1	R101	Sub B Grayscale Data Register 1 (0, 0)					SBG4	SBG3	SBG2	SBG1	SBG0
0	1	1	1	0	0	1	1	0	R102	Sub B Grayscale Data Register 2 (0, 1)					SBG4	SBG3	SBG2	SBG1	SBG0
0	1	1	1	0	0	1	1	1	R103	Sub B Grayscale Data Register 3 (1, 0)					SBG4	SBG3	SBG2	SBG1	SBG0
0	1	1	1	0	1	0	0	0	R104	Sub B Grayscale Data Register 4 (1, 1)					SBG4	SBG3	SBG2	SBG1	SBG0
0	1	1	1	0	1	0	0	1	R105										
0	1	1	1	0	1	0	1	0	R106										
0	1	1	1	0	1	0	1	1	R107										
0	1	1	1	0	1	1	0	0	R108										
0	1	1	1	0	1	1	0	1	R109										
0	1	1	1	0	1	1	1	0	R110										
0	1	1	1	0	1	1	1	1	R111										
0	1	1	1	1	0	0	0	0	R112										
0	1	1	1	1	0	0	0	1	R113										
0	1	1	1	1	0	0	1	0	R114										
0	1	1	1	1	0	0	1	1	R115										
0	1	1	1	1	0	1	0	0	R116										
0	1	1	1	1	0	1	0	1	R117										
0	1	1	1	1	0	1	1	0	R118										
0	1	1	1	1	0	1	1	1	R119										
0	1	1	1	1	1	0	0	0	R120										
0	1	1	1	1	1	0	0	1	R121										
0	1	1	1	1	1	0	1	0	R122										
0	1	1	1	1	1	0	1	1	R123										
0	1	1	1	1	1	1	0	0	R124										
0	1	1	1	1	1	1	0	1	R125										
0	1	1	1	1	1	1	1	0	R126										
0	1	1	1	1	1	1	1	1	R127										

8. POWER SEQUENCE

The μPD161401 has on-chip power circuits such as a booster circuit and a voltage follower circuit. Resetting by the /DISP pin should only be used to prevent malfunctioning due to noise.

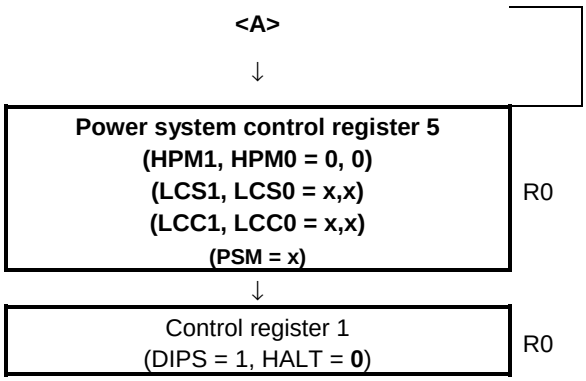
If charge remains in the smoothing capacitor connected between the LCD drive pins (V_{LCD}, V_{LC1} to V_{LC4}) and V_{SS}, the display screen may momentarily blackout when power is turned ON or OFF. It is therefore recommended to turn ON/OFF power in the following sequence to avoid any trouble.

8.1 Power ON Sequence (with Internal Power Supply, Power ON → Display ON)



Note The wait times1, 2 vary depending on the characteristics of the LCD panel and the capacitance of the boosting or smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system (refer to **8.5 Flow of V_{OUT} and V_{LCD} Voltages from Power ON to Power OFF**).

★



Wait time 2
Wait for at least 250 ms from when the output mode of the operation amplifier is changed until the LCD turns ON [Note].

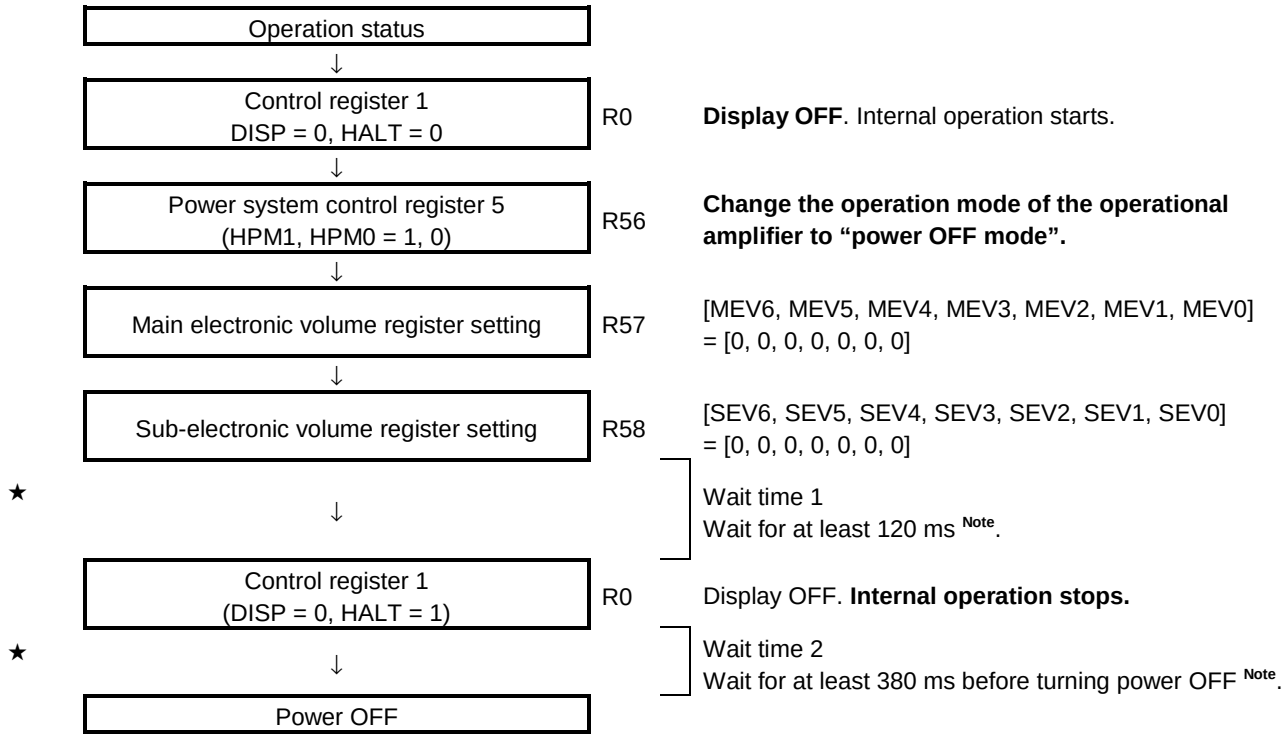
The operation mode of the operation amplifier: normal mode
Change the setting of the segment output driving capability, common output driving capability, and voltage follower bias current to the normal state.

Display ON. **Internal operation starts.**

x: 0 or 1

Note The wait times1, 2 vary depending on the characteristics of the LCD panel and the capacitance of the boosting or smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system (refer to **8.5 Flow of V_{OUT} and V_{LCD} Voltages from Power ON to Power OFF**).

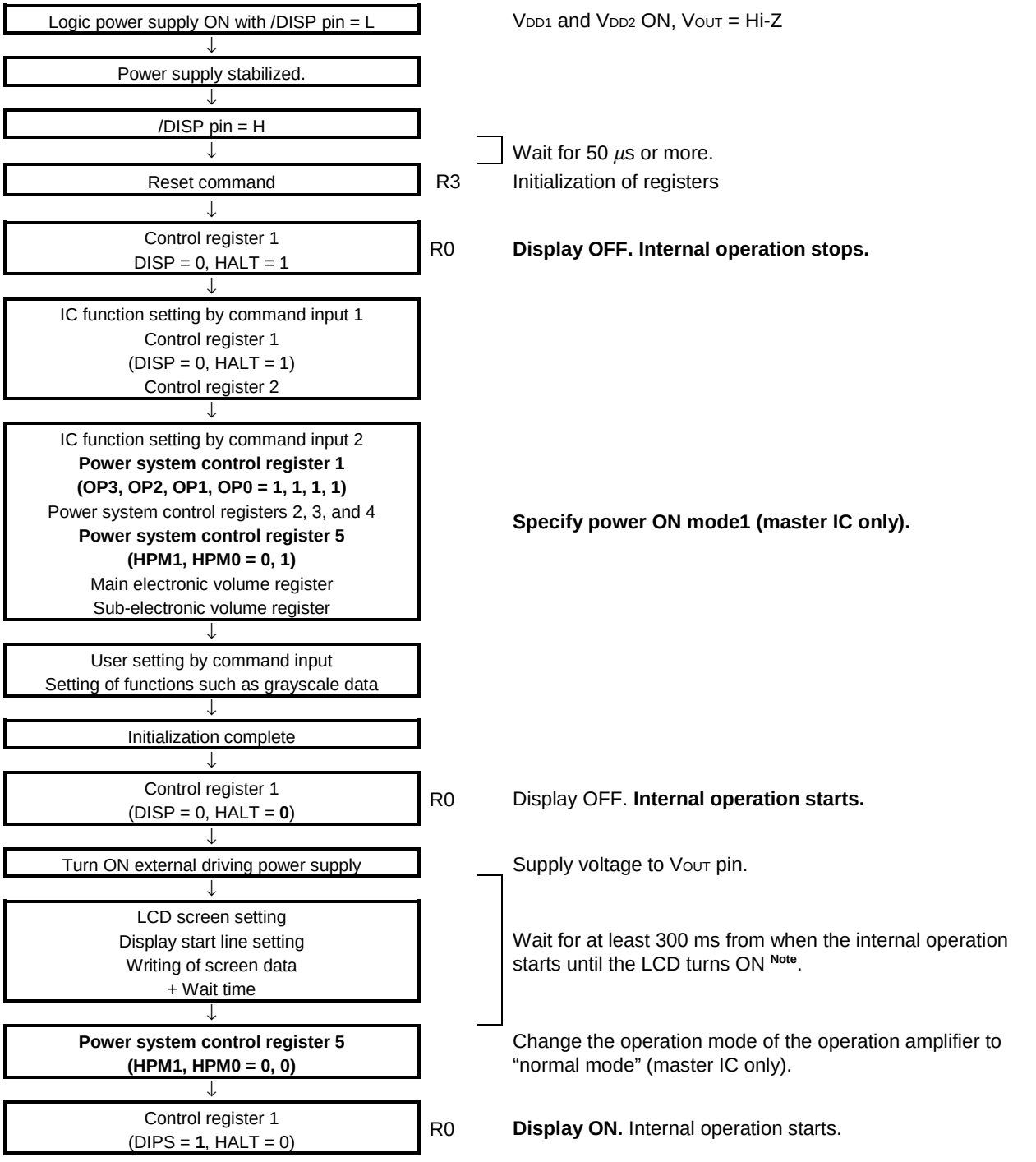
8.2 Power OFF Sequence (with Internal Power Supply)



Note The wait times 1, 2 vary depending on the characteristics of the LCD panel and the capacitance of the boosting or smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system (refer to **8.5 Flow of V_{OUT} and V_{LCD} Voltages from Power ON to Power OFF**).

8.3 Power ON Sequence (with External Driving Power Supply, Power ON → Display ON)

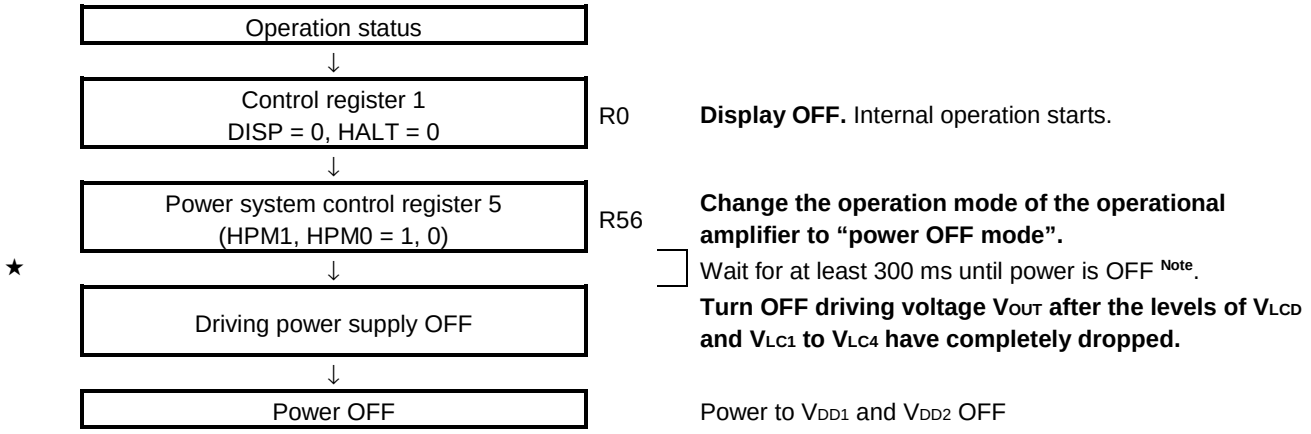
This is an example of inputting a reference voltage to the V_{RS} pin and a driving voltage to the V_{OUT} pin from an external power supply.



Note The time of 300 ms varies depending on the characteristics of the LCD panel and the capacitance of the smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system (refer to **8.5 Flow of V_{OUT} and V_{LCD} Voltages from Power ON to Power OFF**).

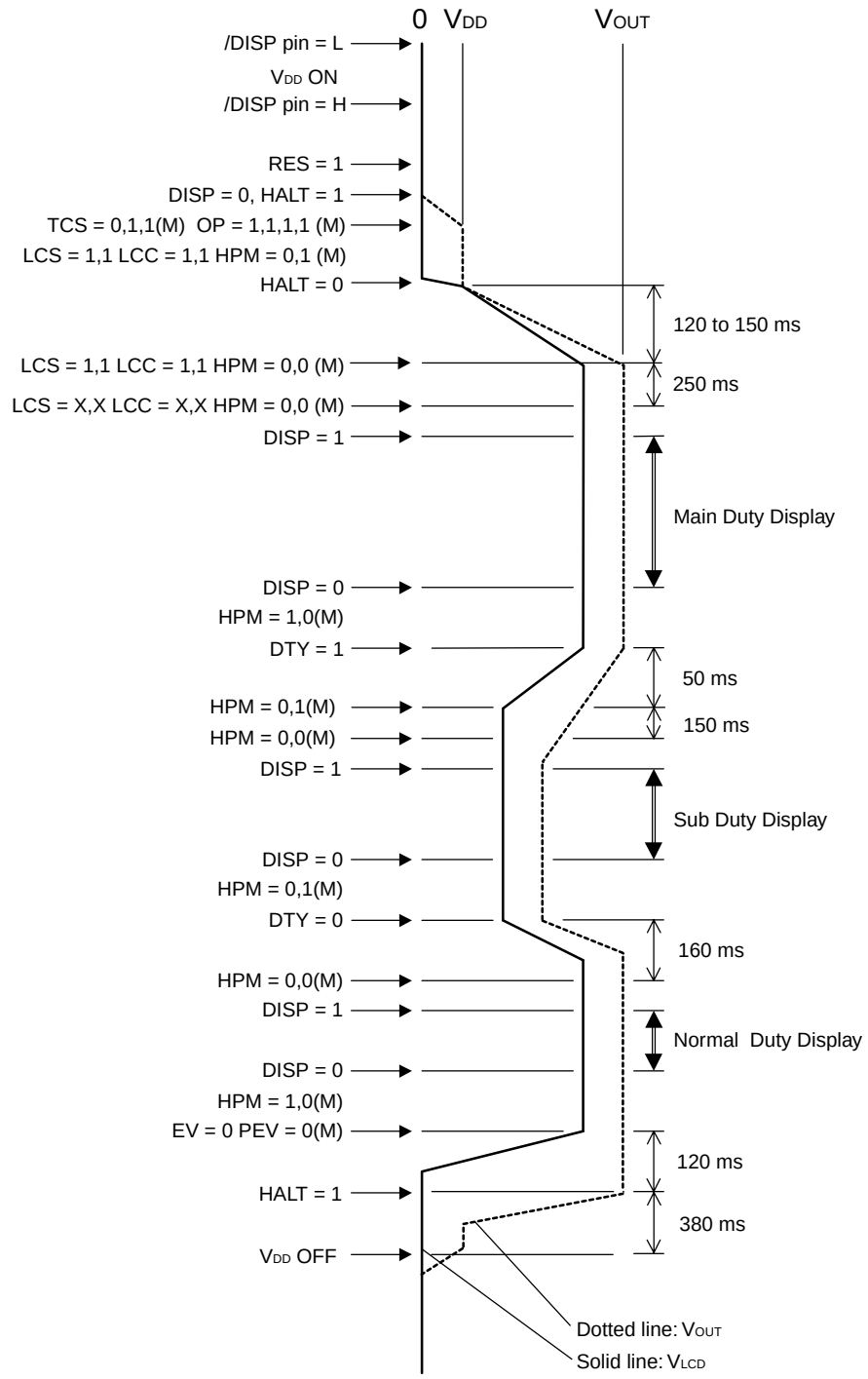
8.4 Power OFF Sequence (with External Driving Power Supply)

This is an example of inputting a reference voltage to the V_{RS} pin and a driving voltage to the V_{OUT} pin from an external power supply.



Note The time of 300 ms varies depending on the characteristics of the LCD panel and the capacitance of the smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system (refer to **8.5 Flow of V_{OUT} and V_{LCD} Voltages from Power ON to Power OFF**).

★ 8.5 Flow of V_{OUT} and V_{LCD} Voltages from Power ON to Power OFF



x: 1 or 0

Test conditions:

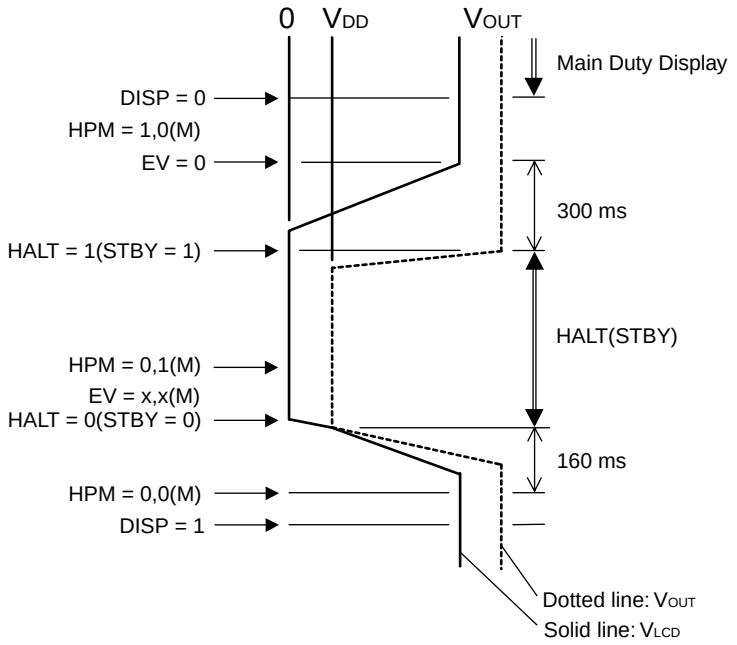
Supply voltage: $V_{DD1} = V_{DD2} = 3.0$ V

Number of boosting stages: x5 (in normal display mode), x3 (in partial display mode)

Capacitance: Between V_{LCn} pin and $C_n^{+/-}$ pins = 1.0 μF

Caution Connect a capacitor of 0.1 μF or less to the AMP_{OUTM} and AMP_{OUTS} pins.

★ 8.6 Flow of V_{OUT} and V_{LCD} Voltages in Display Output and HALT/Standby Modes



x: 1 or 0

Test conditions:

Supply voltage: $V_{DD1} = V_{DD2} = 3.0$ V.

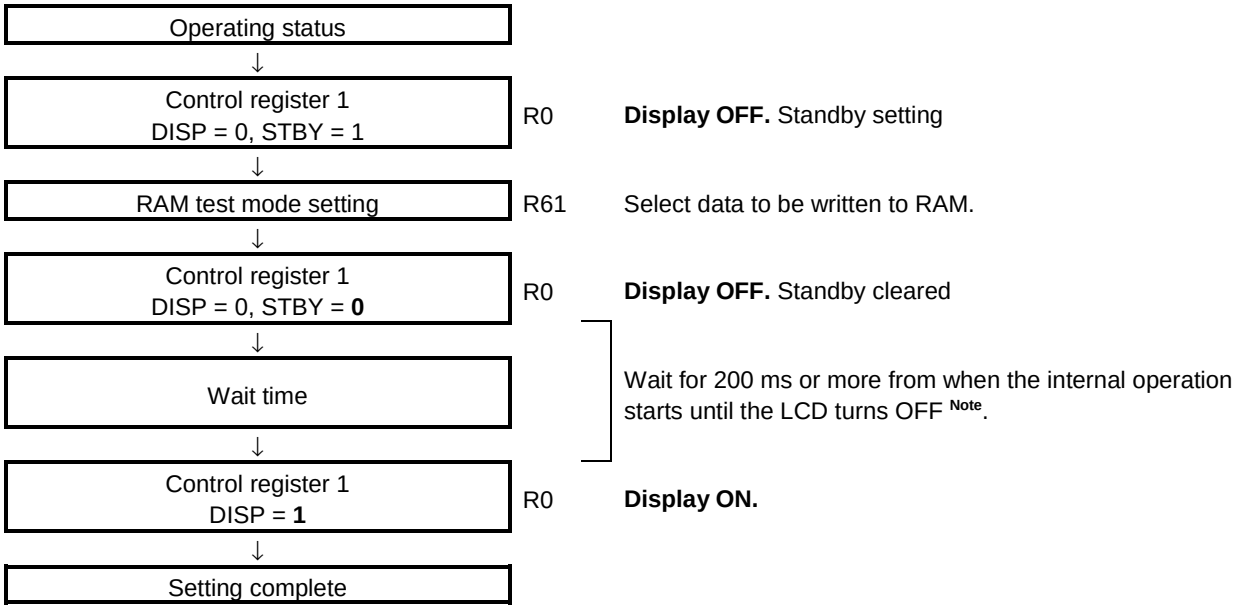
Number of boosting stages: x5 (in normal display mode), x3 (in partial display mode)

Capacitance: Between V_{LCn} pin and $C_n^{+/-}$ pins = 1.0 μF

Caution Connect a capacitor of 0.1 μF or less to the AMP_{OUTM} and AMP_{OUTS} pins.

9. USING RAM TEST MODE

The μPD161401 has a test mode in which seven types of screen data are written to the display RAM. When using this test mode, be sure to execute the following sequence. If the RAM test mode is executed in any other sequence, erroneous data may be displayed.



Note The time of 200 ms varies depending on the characteristics of the LCD panel and the capacitance of the boosting or smoothing capacitor. It is recommended to determine this value after thorough evaluation with the actual system.

Remark The set display data is always written to the display RAM in the RAM test mode.

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD1}	–0.3 to +4.0	V
Booster circuit supply voltage	V_{DD2}	–0.3 to +4.0	V
Driver supply voltage	V_{OUT}	–0.3 to +20.0	V
Driver reference power input voltage	V_{LCD}, V_{LC1} to V_{LC4}	–0.3 to V_{OUT} + 0.3	V
Logic input voltage	V_{IN1}	–0.3 to V_{DD1} + 0.3	V
Logic output voltage	V_{O1}	–0.3 to V_{DD1} + 0.3	V
Logic I/O voltage	$V_{I/O1}$	–0.3 to V_{DD1} + 0.3	V
Driver input voltage	V_{IN2}	–0.3 to V_{OUT} + 0.3	V
Driver output voltage	V_{O2}	–0.3 to V_{OUT} + 0.3	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	1.8		3.6	V
Booster circuit supply voltage	V_{DD2} **Note1**	2.4		3.6	V
Driver supply voltage	V_{OUT} **Note2**	5.5		18.0	V
Logic supply voltage	V_{IN}	0		V_{DD1}	V
Driver supply voltage	V_{LCD}, V_{LC1} to V_{LC4} **Note2**	0		V_{OUT}	V
Maximum LCD voltage setting range	V_{LCD} **Note3**			V_{OUT} – 0.5	V

Notes 1. It is essential that $V_{DD1} \leq V_{DD2}$.

2. These conditions are recommended when the LCD is driven by an external power supply.

3. This condition is recommended when the LCD is driven by the internal power supply circuit.

Cautions 1. Make sure that the relationship of $V_{SS} < V_{LC4} < V_{LC3} < V_{LC2} < V_{LC1} < V_{LCD} \leq V_{OUT}$ is satisfied when the LCD is driven by an external power supply.

2. Make sure that the condition described in 8. POWER SEQUENCE are satisfied when turning power ON or OFF.

3. Keep the voltage at the V_R and V_{RS} pins to between 1.0 V and V_{DD1} when an external resistor is used (when the internal resistor is not used to adjust V_{LCD}).

Electrical Specifications (Unless otherwise specified, T_A = –40 to +85°C, V_{DD1} = 1.8 to 3.6 V, V_{DD2} = 2.4 to 3.6 V.)

Parameter	Symbol	Conditions	MIN.	TYP.Notes1	MAX.	Unit
Input voltage, high	V_{IH}		0.8 V_{DD1}			V
Input voltage, low	V_{IL}				0.2 V_{DD1}	V
Input current, high	I_{IH1}	Other than D_{15} to D_0			1	μA
Input current, low	I_{IL1}	Other than D_{15} to D_0			–1	μA
Output voltage, high	V_{OH}	I_{OUT} = –1 mA. Other than OCS_{OUT}	V_{DD1} – 0.5			V
Output voltage, low	V_{OL}	I_{OUT} = 1 mA. Other than OCS_{OUT}			0.5	V
Leakage current, high	I_{LOH}	D_{15} to D_8, D_7(SI), D_6(SCL), D_5 to D_0, $V_{IN/OUT}$ = V_{DD1}			10	μA
Leakage current, low	I_{LOL}	D_{15} to D_8, D_7(SI), D_6(SCL), D_5 to D_0, $V_{IN/OUT}$ = V_{SS}			–10	μA
Common output ON resistance	R_{COM}	V_{LCn} → COM_n, V_{OUT} = 15 V, V_{LCD} = 13 V, 1/9 bias, |I_O| = 50 μA			4	kΩ
Segment output ON resistance	R_{SEG}	V_{LCn} → SEG_n, V_{OUT} = 15 V, V_{LCD} = 13 V, 1/9 bias, |I_O| = 50 μA			4	kΩ
Driver voltage (booster voltage)	V_{OUT}	In 5-fold mode, V_{DD2} = 3.0 V, diced display	13.8			V
		In 6-fold mode, V_{DD2} = 3.0 V, diced display	16.6			V
Regulated voltageNotes2	V_{REG}	T_A = 85°C. (TCS2, TCS1, TCS0) = (0,1,0) Temperature curve –0.15 %/°C	1.430	1.485	1.540	V
Output voltage deflection	ΔV_{LCn}	V_{LCn}: V_{LCD}, V_{LC1} to V_{LC4}, (OP3, OP2, OP1, OP0) = (0, 0, 0, 1) V_{DD1} = 2.5 V, V_{OUT} = 15 V, AMP_{OUTM} = 14 V, bias = 1/5 to 1/9, IRS pin = L, display OFF, no load	–50		50	mV
	ΔAMP_{OUT}	IRS pin = H, 1+Rb/Ra = 10-fold	–100		100	mV
Oscillation frequency Notes3	f_{OSC}	V_{DD1} = 3.0 V, T_A = 25°C, 1/80 duty, R = 360 kΩ (OSC_{IN1}-OSC_{OUT})	72	85	97	kHz
		V_{DD1} = 3.0 V, T_A = 25°C, 1/38 duty, R = 770 kΩ (OSC_{IN2}-OSC_{OUT})	33	40	46	kHz
Current consumption	I_{DD11}	Frame frequency = 70 Hz, all PWM display output, 1/80 duty, V_{DD1} = V_{DD2} = 3.0 V, V_{LCD} = 13 V, in 5-fold mode, driving mode (segment x 1, common x 4)		175	280	μA
		Frame frequency = 70 Hz, all PWM display output, 1/32 duty, V_{DD1} = V_{DD2} = 3.0 V, V_{LCD} = 7.0 V, in 3-fold mode, driving mode (segment x 1, common x 4)		72	120	μA
Current consumption (standby mode)	I_{DD22}	V_{DD1} = V_{DD2} = 3.0 V			10	μA

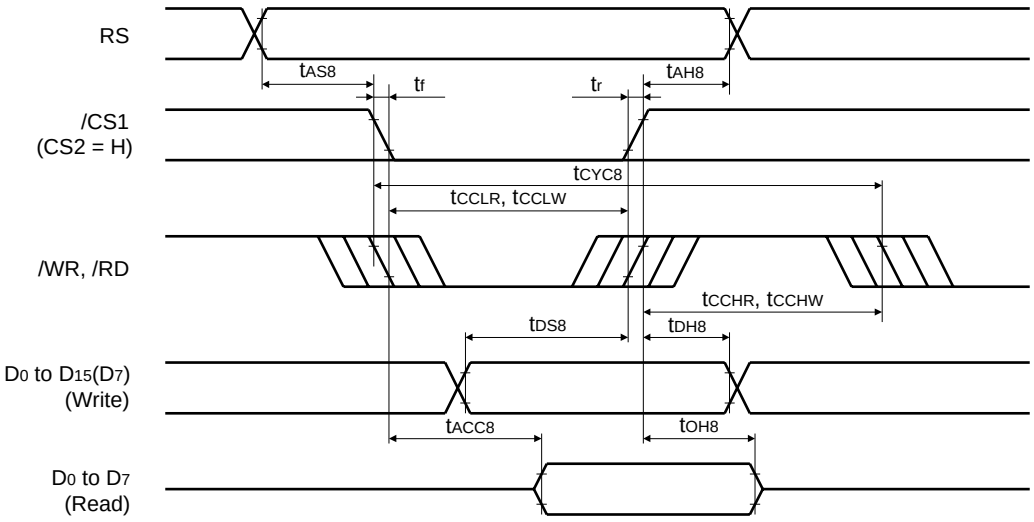
Notes1 The TYP. values are reference values at T_A = 25°C (except for regulated voltage (V_{REG})).

2 The TYP. values of Regulated voltage (V_{REG}) at T_A = 25°C are MIN. 1.580 V, TYP. 1.635 V, MAX. 1.690 V

3 Oscillation frequency is changed under the influence of the wiring capacity to the external resistor for oscillation.

Timing Requirements (Unless otherwise specified, T_A = –30 to +85°C.)

(1) i80 CPU interface



(V_{DD1} = 1.8 to 2.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		1000			ns
Control L pulse width (/WR)	t_{CCLW}	/WR	160			ns
Control L pulse width (/RD)	t_{CCLR}	/RD	430			ns
Control H pulse width (/WR)	t_{CCHW}	/WR	160			ns
Control H pulse width (/RD)	t_{CCHR}	/RD	160			ns
Data setup time	t_{DS8}	D_0 to D_{15} (D_7)	160			ns
Data hold time	t_{DH8}	D_0 to D_{15} (D_7)	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		470	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 5 pF, R_L = 3 kΩ	0		170	ns

Note The TYP. values are reference values at T_A = 25°C.

(V_{DD1} = 2.0 to 2.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		600			ns
Control L pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control L pulse width (/RD)	t_{CCLR}	/RD	240			ns
Control H pulse width (/WR)	t_{CCHW}	/WR	120			ns
Control H pulse width (/RD)	t_{CCHR}	/RD	120			ns
Data setup time	t_{DS8}	D_0 to D_{15} (D_7)	120			ns
Data hold time	t_{DH8}	D_0 to D_{15} (D_7)	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		280	ns
Output disable time	t_{OH8}	D_0 to D_7 , C_L = 5 pF, R_L = 3 kΩ	0		170	ns

Note The TYP. values are reference values at T_A = 25°C.

(V_{DD1} = 2.5 to 3.6 V)

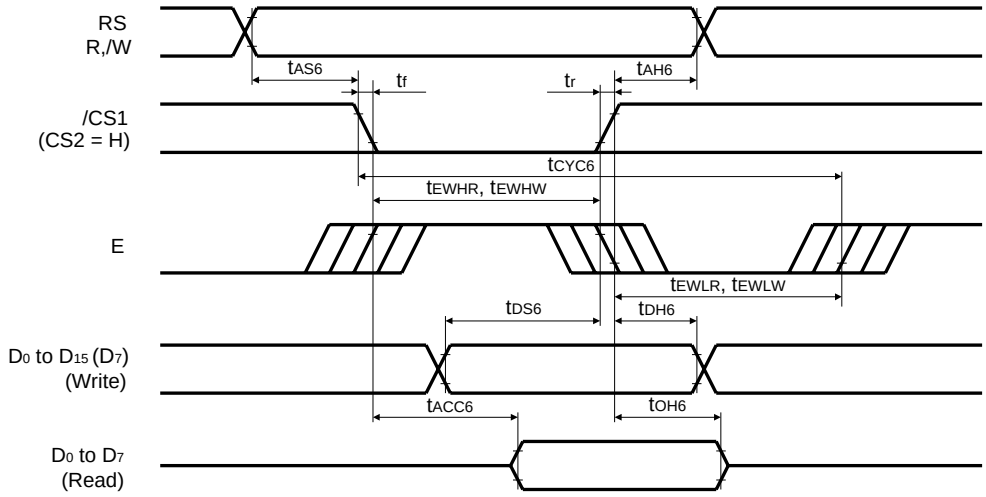
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		100			ns
Control L pulse width (/WR)	t_{CCLW}	/WR	40			ns
Control L pulse width (/RD)	t_{CCLR}	/RD	40			ns
Control H pulse width (/WR)	t_{CCHW}	/WR	40			ns
Control H pulse width (/RD)	t_{CCHR}	/RD	40			ns
Data setup time	t_{DS8}	D_0 to D_{15} (D_7)	40			ns
Data hold time	t_{DH8}	D_0 to D_{15} (D_7)	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		50	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 5 pF, R_L = 3 kΩ	0		50	ns

Note The TYP. values are reference values at T_A = 25°C.

Cautions 1. The rise and fall times (t_r and t_f) of an input signal are 10 ns or less.

2. All timing data is specified at 20% and 80% of V_{DD1}.

(2) M68 CPU interface



(V_{DD1} = 1.8 to 2.0 V)

Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		1000			ns
Data setup time		t_{DS6}	D_0 to D_{15} (D_7)	160			ns
Data hold time		t_{DH6}	D_0 to D_{15} (D_7)	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		470	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns
Enable H pulse width	Read	t_{EWHR}	E	430			ns
	Write	t_{EWHW}	E	160			ns
Enable L pulse width	Read	t_{EWLR}	E	160			ns
	Write	t_{EWLW}	E	160			ns

Note The TYP. values are reference values at T_A = 25°C.

(V_{DD1} = 2.0 to 2.5 V)

Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		600			ns
Data setup time		t_{DS6}	D_0 to D_{15} (D_7)	120			ns
Data hold time		t_{DH6}	D_0 to D_{15} (D_7)	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		280	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns
Enable H pulse width	Read	t_{EWHR}	E	240			ns
	Write	t_{EWHW}	E	120			ns
Enable L pulse width	Read	t_{EWLR}	E	120			ns
	Write	t_{EWLW}	E	120			ns

Note The TYP. values are reference values at T_A = 25°C.

(V_{DD1} = 2.5 to 3.6 V)

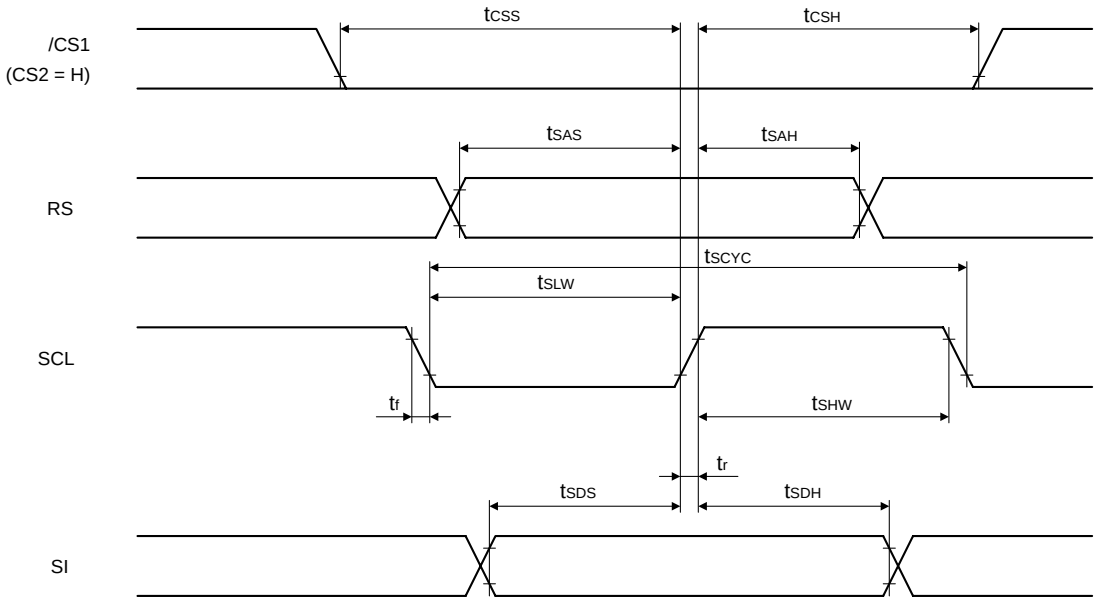
Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		100			ns
Data setup time		t_{DS6}	D_0 to D_{15} (D_7)	50			ns
Data hold time		t_{DH6}	D_0 to D_{15} (D_7)	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		50	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		50	ns
Enable H pulse width	Read	t_{EWHR}	E	40			ns
	Write	t_{EWHW}	E	40			ns
Enable L pulse width	Read	t_{EWLR}	E	40			ns
	Write	t_{EWLW}	E	40			ns

Note The TYP. values are reference values at T_A = 25°C.

Cautions 1. The rise and fall times (t_r and t_f) of an input signal are 10 ns or less. If the system cycle time is short, ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) or ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$).

2. All timing data is specified at 20% and 80% of V_{DD1}.

(3) Serial interface



(V_{DD1} = 1.8 to 2.5 V)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	250			ns
SCL high-level pulse width	t_{SHW}	SCL	100			ns
SCL low-level pulse width	t_{SLW}	SCL	100			ns
Address hold time	t_{SAH}	RS	150			ns
Address setup time	t_{SAS}	RS	150			ns
Data setup time	t_{SDS}	SI	100			ns
Data hold time	t_{SDH}	SI	100			ns
CS - SCL time	t_{CSS}	/CS1 (CS2 = H)	150			ns
	t_{CSH}	/CS1 (CS2 = H)	150			ns

Note TYP. values are reference values when T_A = 25°C.

(V_{DD1} = 2.5 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high-level pulse width	t_{SHW}	SCL	60			ns
SCL low-level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address setup time	t_{SAS}	RS	90			ns
Data setup time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS - SCL time	t_{CSS}	/CS1 (CS2 = H)	90			ns
	t_{CSH}	/CS1 (CS2 = H)	90			ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20% and 80% of V_{DD1}.

(4) Common

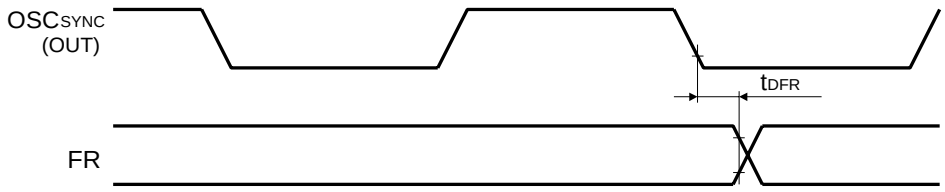
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Clock input 1	f_M	OSC_{IN1}. External clock is used in main duty display mode,1/80 duty		85		kHz
Clock input 2	f_S	OSC_{IN2}. External clock is used in sub-duty display mode, 1/40 duty		40		kHz

Note The TYP. values are reference value at a frame frequency = 70 Hz.

Cautions 1. The rise time and fall time (t_r and t_f) of an input signal is 15 ns or less.

2. All timing data is specified at 20% and 80% of V_{DD1}.

(a) Timing of display control output



(V_{DD1} = 1.8 to 2.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
FR delay time	t_{DFR}	FR, C_L = 50 pF		50	200	ns

Note The TYP. values are reference values at T_A = 25°C.

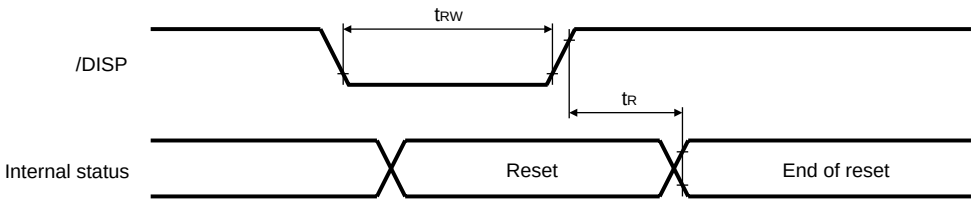
(V_{DD1} = 2.5 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
FR delay time	t_{DFR}	FR, C_L = 50 pF		20	80	ns

Note The TYP. values are reference values at T_A = 25°C.

Caution All timing data is specified at 20% and 80% of V_{DD1}.

(b) Reset timing



(V_{DD1} = 1.8 to 2.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Reset time	t_R				50	μs
Reset L pulse width	t_{RW}	/DISP	50			μs

Note The TYP. values are reference values at T_A = 25°C.

(V_{DD1} = 2.5 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Reset time	t_R				50	μs
Reset L pulse width	t_{RW}	/DISP	50			μs

Note The TYP. values are reference values at T_A = 25°C.

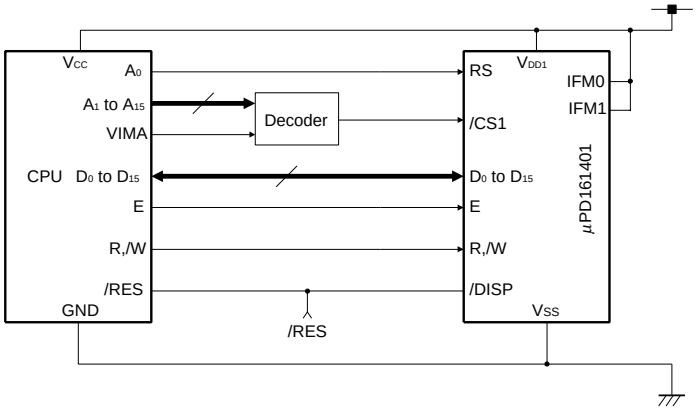
Caution All timing data is specified at 20% and 80% of V_{DD1}.

11. CPU INTERFACE (Reference Example)

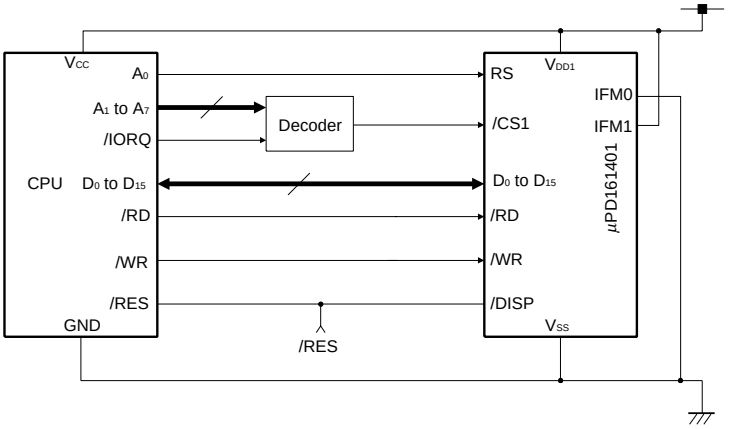
The μPD161401 can be connected to both an i80 system CPU and a M68 system CPU. In addition, the number of signal lines can be reduced by using the serial interface.

The display area can be expanded by using two or more μPD161401 chips. In this case, each IC is selected and accessed by a chip select signal.

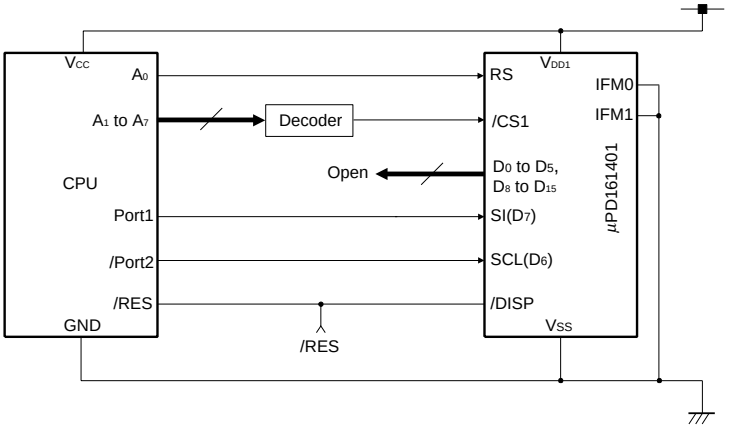
(1) M68 series CPU



(2) i80 series CPU



(3) Serial interface in used



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of June, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4