AS5163

12 BIT AUTOMOTIVE Angle Position Sensor

General Description

The AS5163 is a contactless magnetic angle position sensor for accurate angular measurement over a full turn of 360°. A sub range can be programmed to achieve the best resolution for the application. It is a system-on-chip, combining integrated Hall elements, analog front end, digital signal processing and best in class automotive protection features in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.022° = 16384 positions per revolution. According to this resolution the adjustment of the application specific mechanical positions are possible. The angular output data is available over a 12 bit PWM signal or 12 bit ratiometric analog output.

The AS5163 operates at a supply voltage of 5 V and the supply and output pins are protected against overvoltage up to +27 V. In addition the supply pins are protected against reverse polarity up to – 18 V.
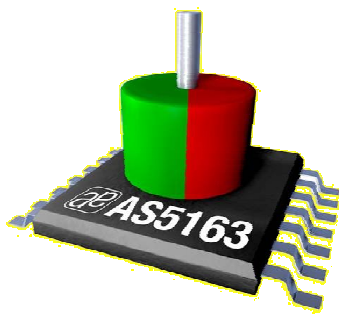

Figure 1: Typical arrangement of AS5163 and magnet

Applications

- Automotive applications:
    - throttle and valve position sensing
    - gearbox position sensor
    - Headlight position control
    - Torque sensing
    - pedal position sensing
    - non contact potentiometers

Benefits

- Unique fully differential patented solution
- Best protections for automotive applications
- Easy to program
- Flexible interface selection PWM, analog output
- Ideal for applications in harsh environments due to contactless position sensing
- Robust system, tolerant to magnet misalignment, air gap variations, temperature variations and external magnetic fields
- No calibration required because of inherent accuracy.
- High driving capability of analog output (including diagnostics)

Key Features

– 360° contactless high resolution angular position encoding

– User programmable start and end point of the application region.

– User programmable clamping levels and programming of the transition point.

– Powerful analog output
  - short circuit monitor
  - High driving capability for resistive and capacitive loads

– Wide temperature range: - 40°C to + 150°C

– Small Pb-free package: TSSOP 14.

– Broken GND and VDD detection over a wide range of different load conditions.
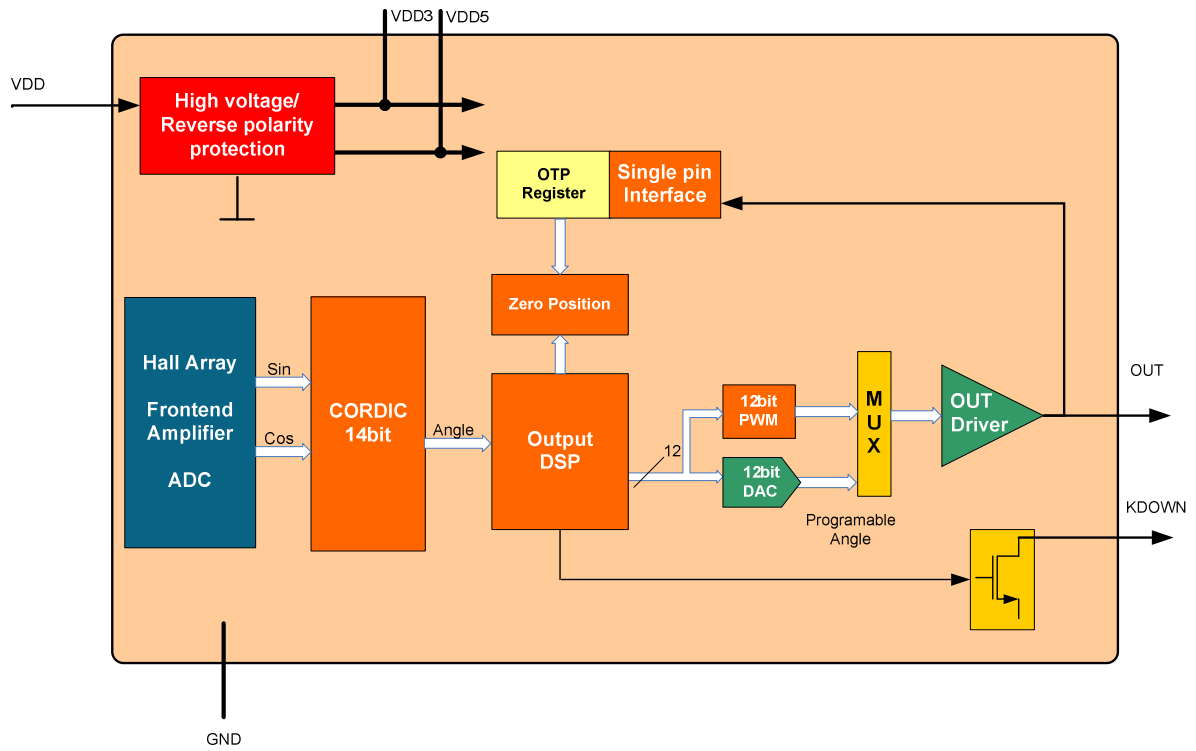
Blockdiagram

Figure 2: Block diagram AS5163

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1.1 Pin Description

Table 1: Pin description TSSOP14 shows the description of each pin of the standard TSSOP14 package (Thin Shrink Small Outline Package, 14 leads; see Figure 3).

Pins 1, 2, 4, 5, 8 and 12 are supply pins and outputs of the internal voltage regulators.

Pins 3, 6, 7, 9, 10 and 13 are used for fabrication test purpose and should be connected according Table 1 at the application board.

Pin 11 is one additional output pin which can be used for a compare function including a hysteresis. An open drain configuration is used. If the internal angle is above a programmable threshold the output is switched to low. Below the threshold the output is high using a pull up resistor.

Pin 14 is the output pin which is used for the analog output or digital PWM output mode. In addition this pin is used for programming of the device.

Pin	Symbol	Type	Description
1	VDD	S	Positive supply pin. This pin is over voltage protected.
2	VDD5	S	4,5V-Regulator output, internally regulated from VDD. This pin needs an external ceramic capacitor of 2.2 µF
3	NC	DIO/AIO	Test pins for fabrication. Connected to ground in the application.
4	VDD3	S	3,45V-Regulator output, internally regulated from VDD5. This pin needs an external ceramic capacitor of 2.2 µF
5	GNDA	S	Analogue ground pin. Connected to ground in the application.
6	NC	DIO/AIO	Test pins for fabrication. Connected to ground in the application.
7	NC	DIO/AIO	Test pins for fabrication. Open in the application.
8	GNDD	S	Digital ground pin. Connected to ground in the application.
9	NC	DIO/AIO	Test pins for fabrication. Connected to ground in the application.
10	NC	DIO/AIO	Test pins for fabrication. Connected to ground in the application.
11	KDOWN	DO_OD	Kick down functionality.
12	GNDP	S	Analogue ground pin. Connected to ground in the application.
13	NC	DIO/AIO	Test pins for fabrication. Connected to ground in the application.
14	OUT	DIO/AIO	Output pin can be programmed as analogue output or PWM output. Over this pin the programming is possible.

Table 1: Pin description TSSOP14

S   supply pin
DO_OD   digital output open drain
DI/AIO   multi purpose pin
DO_T   digital output /tri-state

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Value	Unit	Note
DC supply voltage at pin VDD Overvoltage	VDD	-18	27	V	No operation
Output voltage OUT	Vout	-0.3	27	V	permanent
Output voltage KDOWN	V_{KDOWN}	-0.3	27	V	permanent
DC supply voltage at pin VDD3	VDD3	-0.3	5.5	V	
DC supply voltage at pin VDD5	VDD5	-0.3	7	V	
Input current (latchup immunity)	I_{scr}	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	ESD		± 4	kV	Norm: MIL 883 E method 3015 VDD, GND, OUT and KDOWN Pin. All other pins ± 2 kV
Storage temperature	T_{strg}	-55	125	°C	Min – 67°F ; Max +257°F
Body temperature (Lead-free package)	T_{Body}		260	°C	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn "matte tin"
Humidity non-condensing	H	5	85	%	

Table 2: Absolute maximum ratings

2.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Ambient temperature	T_{amb}	-40		+150	°C	-40°F…+302°F
Supply current	I_{supp}		15		mA	
Supply voltage at pin VDD	VDD	4.5	5.0	5.5	V	5V Operation
Voltage regulator output voltage at pin VDD3	VDD3	3.3	3.45	3.6	V	
Voltage regulator output voltage at pin VDD5	VDD5		4.5		V	

Table 3: Operating Conditions

2.3 Timing Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Internal Master Clock	FRCOT	4.05	4.5	4.95	MHz	±10%
Interface Clock Time	TCLK		222.2		ns	TCLK = 1 / FRCOT
WachDog error detection time	TDETWD			12	ms	

Table 4 Timing conditions

2.4 Magnetic Input Specification

(Operating conditions: T_{amb} = -40 to +150°C, VDD5 = 4.5-5.5V (5V operation) unless otherwise noted)

Two-pole cylindrical diametrically magnetized source:

Parameter	Symbol	Min	Typ	Max	Unit	Note
Diameter	d_{mag}		6		mm	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets
Thickness	t_{mag}	2.5			mm	
Magnetic input field amplitude	B_{pk}	30		70	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm

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Parameter	Symbol	Min	Typ	Max	Unit	Note
Magnetic offset	B_{off}			± 10	mT	Constant magnetic stray field
Field non-linearity				5	%	Including offset gradient
Displacement radius	Disp		0.25	1	mm	Offset between defined device center and magnet axis (see Figure 27). Dependant on the selected magnet.
Eccentricity	Ecc		100		µm	Eccentricity of magnet center to rotational axis
Recommended magnet material and temperature drift			-0.12		%/K	NdFeB (Neodymium Iron Boron)
			-0.035			SmCo (Samarium Cobalt)

Table 5: Magnet Input Specification

2.5 Electrical System Specifications

(Operating conditions: T_{amb} = -40 to +150°C, VDD = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution Analog and PWM Output	RES			12	bit	
Integral non-linearity (optimum) 360 degree full turn	INL_{opt}			± 0.5	deg	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{amb} =25 °C.
Integral non-linearity (optimum) 360 degree full turn	INL_{temp}			± 0.9	deg	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{amb} = -40 to +150°C
Integral non-linearity 360 degree full turn	INL			± 1.4	deg	Best line fit = $(Err_{max} – Err_{min}) / 2$ Over displacement tolerance with 6mm diameter magnet, without calibration, T_{amb} = -40 to +150°C
Transition noise	TN		0.06		Deg RMS	1 sigma
Power-on reset thresholds On voltage; 300mV typ. hysteresis Off voltage; 300mV typ. hysteresis	V_{on} V_{off}	1.37 1.08	2.2 1.9	2.9 2.6	V V	DC supply voltage 3.3V (VDD3) DC supply voltage 3.3V (VDD3)
Power-up time	t_{PwrUp}			10	ms	
System propagation delay absolute output : delay of ADC, DSP and absolute interface	t_{delay}			100	µs	Fast mode, times 2 in slow mode

Table 5: Electrical System Specifications

Note: The INL performance is specified over the full turn of 360 degrees. An operation in an angle segment increases the accuracy. A two point linearization is recommended to achieve the best INL performance for the chosen angle segment.

3 Functional Description

The AS5163 is manufactured in a CMOS process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5163 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs that indicate movements of the used magnet towards or away from the device's surface.

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A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 26).

The AS5163 senses the orientation of the magnetic field and calculates a 14-bit binary code. This code is mapped to a programmable output characteristic. The type of output is programmable and can be selected as PWM or analog output. This signal is available at the pin 14 (**OUT**).

The analog and PWM output can be configured in many ways. The application angular region can be programmed in a user friendly way. The start angle position **T1** and the end point **T2** can be set and programmed according the mechanical range of the application with a resolution of 14 bits. In addition the **T1Y** and **T2Y** parameter can be set and programmed according the application. The transition point 0 to 360 degree can be shifted using the break point parameter **BP**. This point is programmable with a high resolution of 14 bits of 360 degrees. The voltage for clamping level low **CLL** and clamping level high **CLH** can be programmed with a resolution of 7 bits. Both levels are individually adjustable.

These parameters are also used to adjust the PWM duty cycle.

The AS5163 provides also a compare function. The internal angular code is compared to a programmable level using hysteresis. The function is available over the output pin 11 (**KDOWN**).

The output parameters can be programmed in an OTP register. No additional voltage is required to program the AS5163. The setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by using a lock bit the content could be frozen for ever.

The AS5163 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry.

4　Operation

The AS5163 operates at 5V ±10%, using two internal Low-Dropout (LDO) voltage regulators. For operation, the 5V supply is connected to pin **VDD**. While **VDD3** and **VDD5** (LDO outputs) must be buffered by 2.2µF capacitors, the **VDD** requires a 1µF capacitor. All capacitors (low ESR ceramic) are supposed to be placed close to the supply pins (see Figure 4).

The **VDD3** and **VDD5** outputs are intended for internal use only. It must not be loaded with an external load.
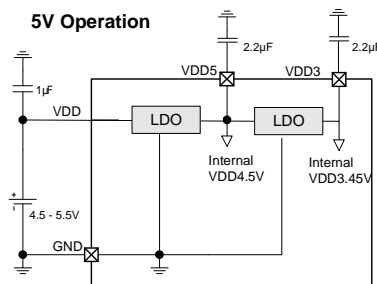
Figure 4: Connections for 5V supply voltages

Note: The pins **VDD3** and **VDD5** must always be buffered by a capacitor. It must not be left floating, as this may cause instable internal supply voltages which may lead to larger output jitter of the measured angle.

The supply pins are over voltage protected up to 27 V. In addition the device has a reverse polarity protection.

4.1　VDD Voltage Monitor

4.1.1　VDD Overvoltage Management

If the voltage applied to the VDD pin exceeds the over-voltage upper threshold for longer than the detection time the device enters a low power mode reducing the power consumption. When the overvoltage event has passed and the voltage applied

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to the VDD pin falls below the over-voltage lower threshold for longer than the recovery time the device enters the normal mode.

4.1.2 VDD5 Undervoltage Management

When the voltage applied to the VDD5 pin falls below the under-voltage lower threshold for longer than the VDD5_detection time the device stops the clock of the digital part and the output drivers are turned off to reduce the power consumption. When the voltage applied to the VDD5 pin exceeds the VDD5 undervoltage upper threshold for longer than the VDD5_recovery time the clock is restarted and the output drivers are turned on.

5 Analog Output

By default (after programmed **Mem_Lock_AMS** OTP bit) the analog output mode is selected. The pin **OUT** provides an analog voltage that is proportional to the angle of the rotating magnet and ratiometric to the supply voltage **VDD**. It can source or sink currents up to ±8mA in normal operation. Above this limit the short circuit operation mode is activated. Due to an intelligent approach a permanent short circuit will not damage the device. This is also feasible in a high voltage condition up to 27 V and at the highest specified ambient temperature.

After the digital signal processing (DSP) a 12-bit Digital-to-Analog converter and output stage provides the output signal.

The DSP maps the application range to the output characteristic. An inversion of the slope is also programmable to allow inversion of the rotation direction.

The reference voltage for the Digital-to-Analog converter (DAC) is taken internally from **VDD** / 2. In this mode, the output voltage is ratiometric to the supply voltage.

An on-chip diagnostic feature force the analog output in the desired failure band. This will happen in case of a broken supply, too high or low magnetic field, short circuit and overvoltage condition.

The Analog output is selected with the unprogrammed OTP bit **OP_MODE(0**).

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5.1 Programming Parameters

The analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be adjusted. The user can program the following application specific parameters:

T1   Mechanical angle start point

T2   Mechanical angle end point

T1Y   Voltage level at the T1 position

T2Y   Voltage level at the T2 position

CLL   Clamping Level Low

CLH   Clamping Level High

BP   Break point (transition point 0 to 360 degree)

These parameters are input parameters. Over the provided programming software and programmer these parameters are converted and finally written into the AS5163 128 bit OTP memory.

5.1.1   Application specific angular range programming

The application range can be selected by programming **T1** with a related **T1Y** and **T2** with a related **T2Y** into the AS5163. The internal gain factor is calculated automatically. The clamping levels **CLL** and **CLH** can be programmed independent from the **T1** and **T2** position and both levels can be separately adjusted.
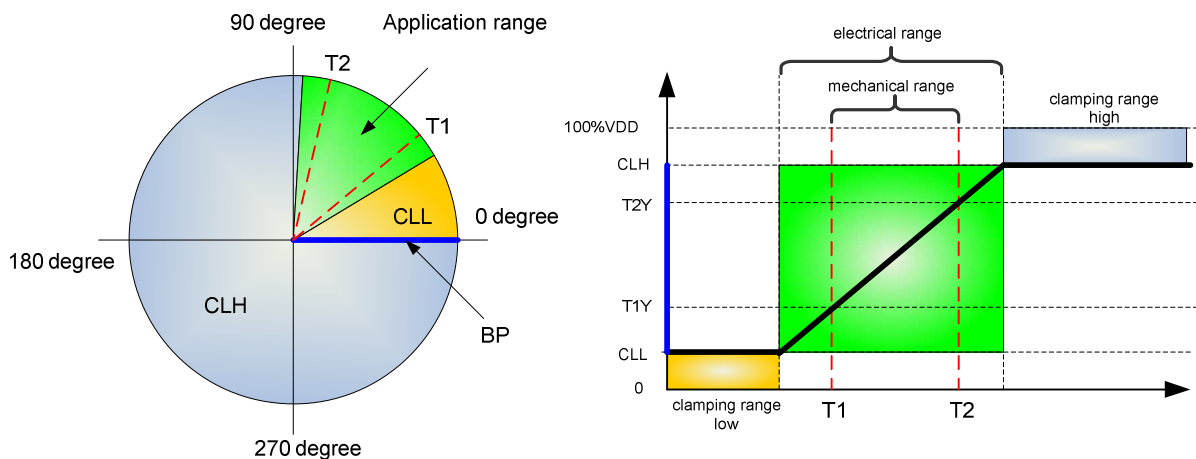
Figure 5: Programming of an individual application range

Figure 5 shows a simple example of the selection of the range. The mechanical starting point **T1** and the mechanical end point **T2** are defining the mechanical range. A sub range of the internal Cordic output range is used and mapped to the needed output characteristic. The analog output signal has 12 bit, hence the level **T1Y** and **T2Y** can be adjusted with this resolution. As a result of this level and the calculated slope the clamping region low is defined. The break point **BP** defines the transition between **CLL** and **CLH**. In this example the **BP** is set to 0 degree. The **BP** is also the end point of the clamping level high **CLH**. This range is defined by the level **CLH** and the calculated slope. Both clamping levels can be set independently form each other. The minimum application range is 10 degrees.

5.1.2   Application specific programming of the break point

The break point **BP** can be programmed as well with a resolution of 14 bits. This is important when the default transition point is inside the application range. In such a case the default transition point must be shifted out of the application range. The parameter **BP** defines the new position. The function can be used also for an on-off indication.
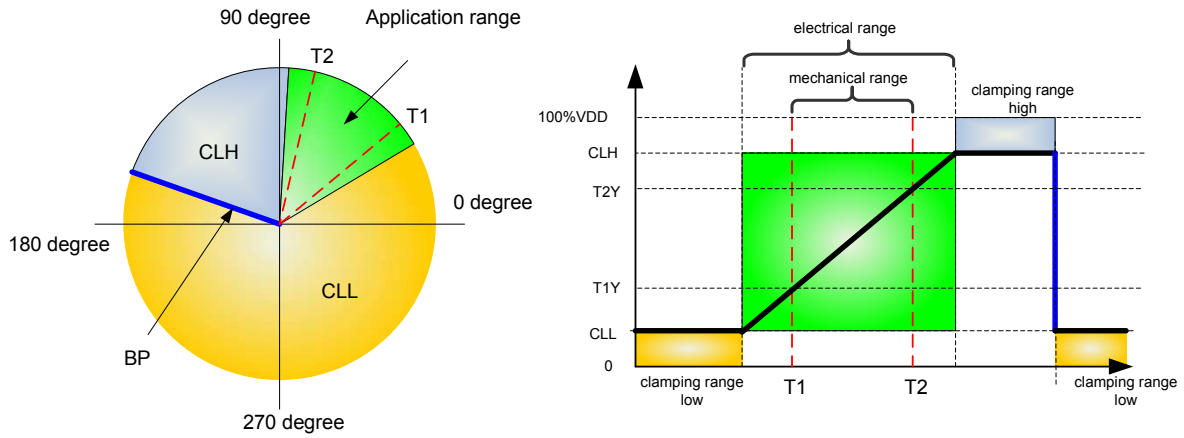
Figure 6: Individual programming of the break point BP

5.1.3 Full Scale Mode

Without programming the parameters **T1** and **T2** the AS5163 is in the full scale mode.
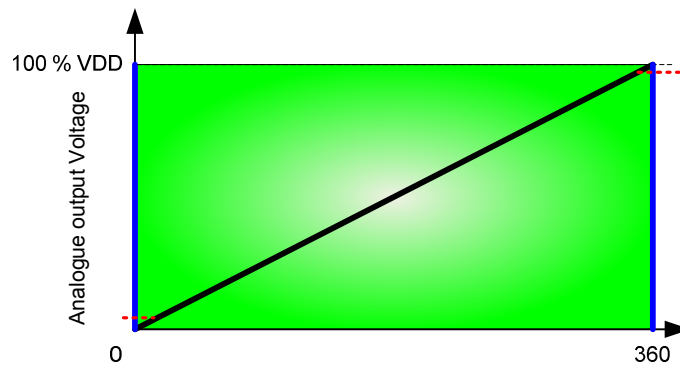
Figure 7: Full scale mode

For simplification, Figure 7 describes a linear output voltage from rail to rail (0V to VDD) over the complete rotation range. In practice, this is not feasible due to saturation effects of the output stage transistors. The actual curve will be rounded towards the supply rails (as indicated Figure 7).

5.1.4 Resolution of the Parameters

The programming parameters have a wide resolution up to 14 bits.

Parameter	Symbol	Resolution	Note
Mechanical angle start point	T1	14 bits	
Mechanical angle stop point	T2	14 bits	
Mechanical start voltage level	T1Y	12 bits	
Mechanical stop voltage level	T2Y	12 bits	
Clamping level low	CLL	7 bits	4096 LSBs is the max. level
Clamping level high	CLH	7 bits	31 LSBs is the min. level
Break point	BP	14 bits	

Table 6: Resolution of the programming parameters

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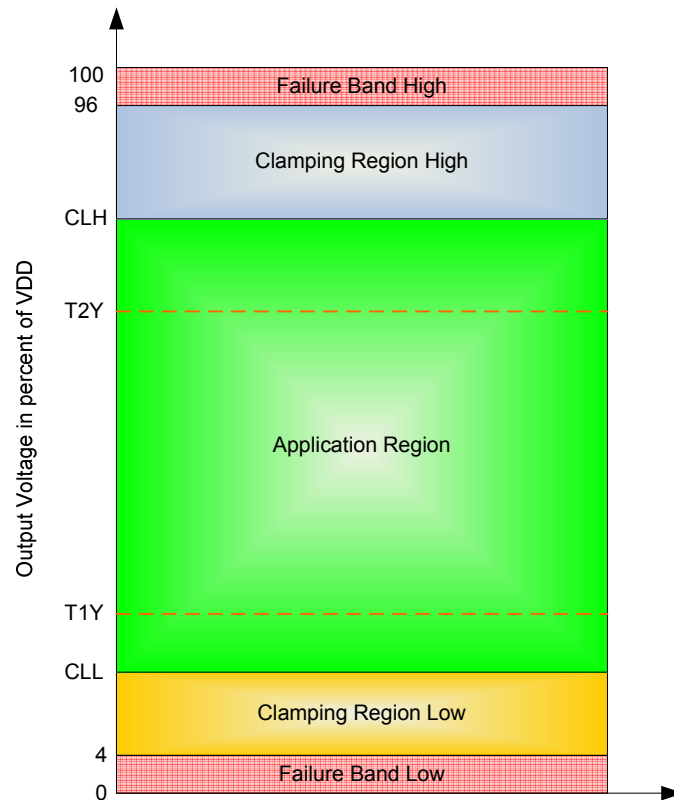
Figure 8: Overview about the angular output voltage

Figure 8 gives an overview about the different ranges. The failure bands are used to indicate a wrong operation of the AS5163. This can be caused due to a broken supply line. By using the specified load resistors the output level will remain in these bands during a fail. It is recommended to set the clamping level **CLL** above the lower failure band and the clamping level **CLH** below the higher failure band.

5.1.5   Analogue Output Diagnostic Mode

Due to the low pin count in the application a wrong operation must be indicated by the output pin **OUT**. This could be realized using the failure bands. The failure band is defined with a fixed level. The failure band low is specified from 0 to 4 % of the supply range. The failure band high is defined from 100 to 96 %. Several failures can happen during operation. The output signal remains in these bands over the specified operating and load conditions. All different failures can be grouped into the internal alarms (failures) and the application related failures.

$C_{LOAD} \leq 42$ nF, $R_{PU}= 2k...5.6kOhm$
$R_{PD}= 2k...5.6kOhm$ load pull-up

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Type	Failure mode	Symbol	Failure band	Note
Internal alarms (failures)	Out of magnetic range (too less or too high magnetic input)	MAGRng	High/Low	Could be switched off by one OTP bit **ALARM_DISABLE** Programmable by OTP bit **DIAG_HIGH.**
	Cordic overflow	COF	High/Low	Programmable by OTP bit **DIAG_HIGH**.
	Offset compensation finished	OCF	High/Low	Programmable by OTP bit **DIAG_HIGH**.
	Watch dog fail	WDF	High/Low	Programmable by OTP bit **DIAG_HIGH**.
	Oscillator fail	OF	High/Low	Programmable by OTP bit **DIAG_HIGH**.
Application related failures	Overvoltage condition	OV	High/Low	Dependent on the load resistor Pull up → failure band high Pull down→ failure band low
	Broken VDD	BVDD		
	Broken VSS	BVSS		
	Short circuit output	SCO	High/Low	Switch off → short circuit dependent

Table 7: different failure cases of AS5163

For efficient use of diagnostics it is recommended to program to clamping levels **CLL** and **CLH**.

5.2 Analog Output Driver Parameters

The output stage is configured in a push-pull output. Therefore it is possible to sink and source currents.

C_{LOAD}≤ 42 nF, R_{PU}= 2k…5.6kOhm
R_{PD}= 2k…5.6kOhm load pull-up

Parameter	Symbol	Min	Typ	Max	Unit	Note
Short circuit output current (low side driver)	IOUTSCL	8		32	mA	VOUT=27V
Short circuit output current (high side driver)	IOUTSCH	-8		-32	mA	VOUT=0V
Short circuit detection time	TSCDET	20		400	us	output stage turned off
Short circuit recovery time	TSCREC	1.5		15	ms	output stage turned on
Output Leakage current	ILEAKOUT	-20		20	uA	VOUT=5V; VDD=0V
Output voltage broken GND with pull-up	BGNDPU	96		100	%VDD	
Output voltage broken GND with pull-down	BGNDPD	0		4	%VDD	
Output voltage broken VDD with pull-up	BVDDPU	96		100	%VDD	
Output voltage broken VDD with ull-down	BVDDPD	0		4	%VDD	

Table 8: General Parameters Output Driver

Note: A Pull-Up/Down load up to 1kOhm with increased diagnostic bands from 0%-6% and 94%-100%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Voltage Range	VOUT	4		96	% VDD	
Output Integral nonlinearity	VOUTINL			10	LSB	
Output Differential nonlinearity	VOUTDNL	-10		10	LSB	
Output Offset	VOUTOFF	-50		50	mV	at 2048 LSB level
Update rate of the Output	VOUTUD		100		us	info parameter
Output Step Response	VOUTSTEP			555	us	Between 10% and 90 %, RPUOUT =1kOhm, CLOUT=1nF; VDD=5V
Output Voltage Temperature drift	VOUTDRIFT	-1		1	%	of value at mid code; info parameter
Output ratiometricity error	VOUTRATE	-1.5		1.5	%VDD	0.04*VDD≤VOUT≤0.96*VDD
Noise	VOUTNOISE			10	mVpp	1Hz…30kHz; at 2048 LSB level

Table 9: Electrical parameters for the analogue output stage

6 Pulse Width Modulation (PWM) Output

The AS5163 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. This output format is selectable over the OTP memory **OP_MODE(0)** bit. If output pin **OUT** is configured as open drain configuration an external load resistor (pull up) is required. The PWM frequency is internally trimmed to an accuracy of ±10% over full temperature range. This tolerance can be cancelled by measuring the ratio between the on and off state. In addition the programmed clamping levels **CLL** and **CLH** will also adjust the PWM signal characteristic.
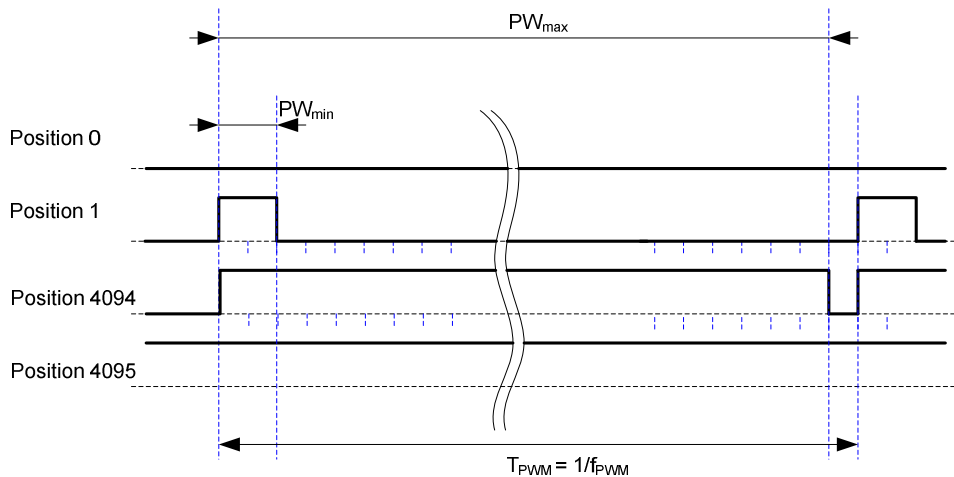

Figure 9: PWM output signal

The PWM frequency can be programmed by the OTP bits **PWM_frequency (1:0).** Therefore 4 different frequencies are possible.

Parameter	Symbol	Min	Typ	Max	Unit	Note
PWM frequency1	f_{PWM1}	123.60	137.33	151.06	Hz	**PWM_frequency (1:0)** = "00"
PWM frequency2	f_{PWM2}	247.19	274.66	302.13	Hz	**PWM_frequency (1:0)** = "01"
PWM frequency3	f_{PWM3}	494.39	549.32	604.25	Hz	**PWM_frequency (1:0)** = "10"
PWM frequency4	f_{PWM4}	988.77	1098.63	1208.50	Hz	**PWM_frequency (1:0)** = "11"
MIN pulse width	PW_{MIN}		$(1+1)*1/f_{PWM}$		µs	
MAX pulse width	PW_{MAX}		$(1+4094)*1/f_{PWM}$		ms	

Table 10: PWM signal parameters

Taking into consideration the AC characteristic of the PWM output including load it is recommended to use the clamping function. The 0 to 4 % and 96 to 100 % range is recommended.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output voltage low	PWMVOL	0		0.4	V	IOUT=8mA
Output leakage	ILEAK	-20		20	uA	VOUT=5V
PWM duty cycle range	PWMDC	4		96	%	
PWM slew rate	PWMSRF	1	2	4	V/us	Between 75 % and 25 % RPUOUT = 1kΩ, CLOUT= 1nF, VDD= 5V
Voltage difference between VDD of ASIC and pull-up load supply	ΔSUPP			100	mV	

Table 11: Electrical parameters for the PWM output mode

7 Kick Down function

The AS5163 provides a special compare function. Using a programmable angle value with a programmable hysteresis this function is implemented. It will be indicated over the open drain output pin **KDOWN.** If the actual angle is above the programmable value plus the hysteresis, the output is switched to low. The output will remain at low level until the value KD is reached in the reverse direction.
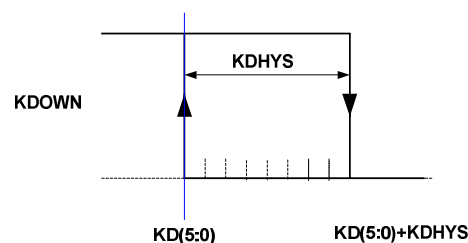

Figure 10: Kick Down Hysteresis implementation

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Parameter	Symbol	Resolution	Note
Kick down angle	**KD**	6 bits	
Kick down Hysteresis	**KDHYS**	2 bits	**KDHYS (1:0)** = "00" → 8 LSB hysteresis **KDHYS (1:0)** = "01" → 16 LSB hysteresis **KDHYS (1:0)** = "10" → 32 LSB hysteresis **KDHYS (1:0)** = "11" → 64 LSB hysteresis

Table 12: Programming parameters for the Kick Down function

Pull up resistance 1k to 5.6K to VDD
C_{load} max 42nF

Parameter	Symbol	Min	Typ	Max	Unit	Note
Short circuit output current (Low Side Driver)	IOUTSC	6		24	mA	VKDOWN=27V
Short circuit detection time	TSCDET	20		400	us	output stage turned off
Short circuit recovery time	TSCREC	1.5		15	ms	output stage turned on
Output voltage low	KDVOL	0		1.1	V	IKDOWN=6mA
Output leakage	KDILEAK	-20		20	uA	VKDOWN=5V
KDOWN slew rate (falling edge)	KDSRF	1	2	4	V/us	Between 75 % and 25 %, RPUKD = 1kΩ, CLKD= 1nF, VDD= 5V

Table 13: Electrical parameters of the KDOWN output

8 Programming the AS5163

The AS5163 programming is a one-time-programming (OTP) method, based on polysilicon fuses. The advantage of this method is that no additional programming voltage is needed. The internal LDO provides the current for programming.

The OTP consists of 128 bits; several bits are available for user programming. In addition factory settings are stored in the OTP memory. Both regions are independently lockable by build in lock bits.

A single OTP cell can be programmed only once. Per default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, as long as only unprogrammed "0"-bits are programmed to "1".

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command. This is possible only if the user lock bit is not programmed.

Due to the programming over the output pin the device will initially start in the communication mode. In this mode the digital angle value can be read with a specific protocol format. It is a bidirectional communication possible. Parameters can be written into the device. A programming of the device is triggered by a specific command. With another command (pass2func) the device can be switched into operation mode (analog or PWM output). In case of a programmed user lock bit the AS5163 automatically starts up in the functional operation mode. No communication of the specific protocol is possible after this.

8.1   Hardware Setup

For OTP memory access the pin OUT and the supply connection is required. Without the programmed **Mem_Lock_USER** OTP bit the device will start up in the communication mode and will remain into an IDLE operation mode. The pull up resistor $R_{Communication}$ is required during startup. Figure 1 shows the configuration of an AS5163.
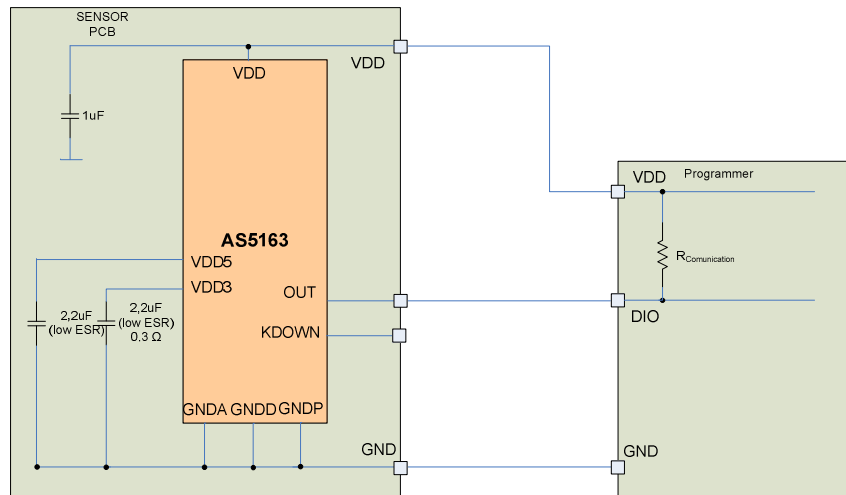

Figure 11: Programming schematic of the AS5163

8.2   Protocol timing and commands of single pin interface

During the communication mode the output level is defined by the external pull up resistor $R_{Communication}$. The output driver of the device is in tri-state. The bit coding (shown in Figure 12) has been chosen in order to allow the continuous synchronization during the communication, which can be required due to the tolerance of the internal clock frequency. Figure 12 shows how the different logic states '0' and '1' are defined. The period of the clock T_{CLK} is defined with 222.2 ns.

The voltage levels V_H and V_L are CMOS typical.

Each frame is composed by 20 bits. The 4 MSB (CMD) of the frame specifies the type of command that is passed to the AS5163. 16 data bits contains the communication data. There will be no operation in case of the usage of a not specified CMD. The sequence is oriented in a way that the LSB of the data is coming first followed by the command. Depending on the command the number of frames is different. The single pin programming interface block of the AS5163 can operate in slave communication or master communication mode. In the slave communication mode the AS5163 receives the data organized in frames. The programming tool is the driver of the single communication line and can pull down the level. In case of the master communication mode the AS5163 transmits data in the frame format. The single communication line can be pulled down by the AS5163.
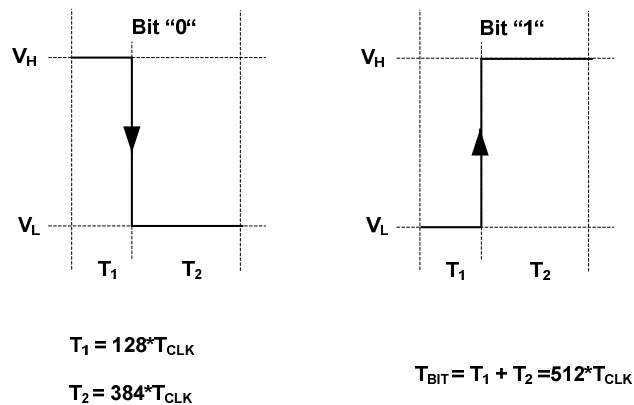

$$T_1 = 128*T_{CLK}$$

$$T_2 = 384*T_{CLK}$$

$$T_{BIT} = T_1 + T_2 = 512*T_{CLK}$$

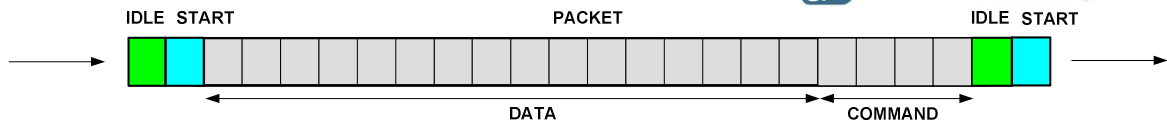**Figure 12: Bit coding of the single pin programming interface**

Figure 13: Protocol Definition

Possible Interface commands	Description	AS5X63 Communication Mode	Command CMD	Number of Frames
UNBLOCK	Resets the interface	SLAVE	0x0	1
WRITE128	Writes 128 bits (user + factory settings) into the device	SLAVE	0x9 (0x1)	8
READ128	Read 128 bits (user + factory settings) from the device	SLAVE and MASTER	0xA	9
UPLOAD	Transfers the register content into the OTP memory	SLAVE	0x6	1
DOWNLOAD	Transfers the OTP content to the register content	SLAVE	0x5	1
FUSE	Command for permanent programming	SLAVE	0x4	1
PASS2FUNC	Change operation mode from communication to operation	SLAVE	0x7	1
READ	Read related to the address the user data	SLAVE and MASTER	0xB	2
WRITE	Write related to the address the user data	SLAVE	0xC	1

Table 14: OTP commands and communication interface modes

Note: The command CMD 0x2 is reserved for AMS test purpose.

When single pin programming interface bus is in high impedance state the logical level of the bus is held by the pull up resistor $R_{Communication}$. Each communication begins by a condition of the bus level which is called START. This is done by forcing the bus in logical low level (done by the programmer or AS5163 depending on the communication mode). Afterwards the bit information of the command is transmitted as shown in Figure 14.

Figure 14: Bus timing for the WRITE128 command
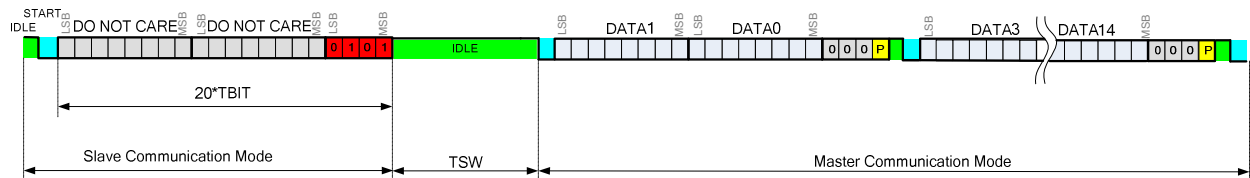
Figure 15: Bus timing for the READ128 command

In case of READ or READ128 command (Figure 15) the idle phase between the command and the answer is 10 TBIT (TSW).
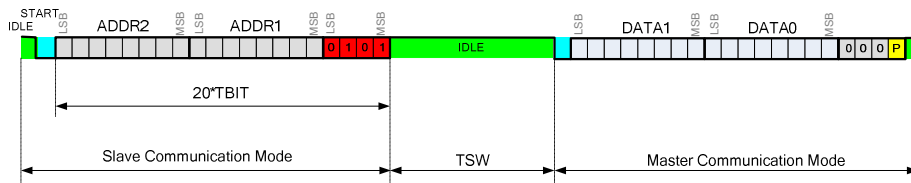
Figure 16: Bus timing for the READ commands

In case of a WRITE command, the device stays in slave communication mode and will not switch to master communication mode.

When using other commands like DOWNLOAD, UPLOAD, etc. instead of READ or WRITE, it does not matter what is written in the address fields (ADDR1, ADDR2).

8.2.1 Unblock

The Unblock command can be used to reset only the one-wire interface of the AS5163 in order to recover the possibility to communicate again without the need of a POR after a stacking event due to noise on the bus line or misalignment with the AS5163 protocol.

The command is composed by a not idle phase of at least 6 TBIT followed by a packet with all 20 bits at zero (see picture below).

Figure 17: Unblock sequence

8.2.2 WRITE128

Figure 18 shows the format of the frame and the command:

DATA1	DATA0	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 1** MSB

DATA3	DATA2	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

DATA5	DATA4	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

DATA7	DATA6	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

DATA9	DATA8	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

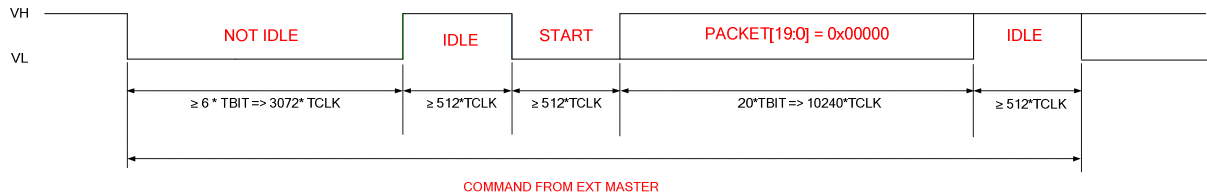| DATA11	DATA10	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

DATA13	DATA12	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

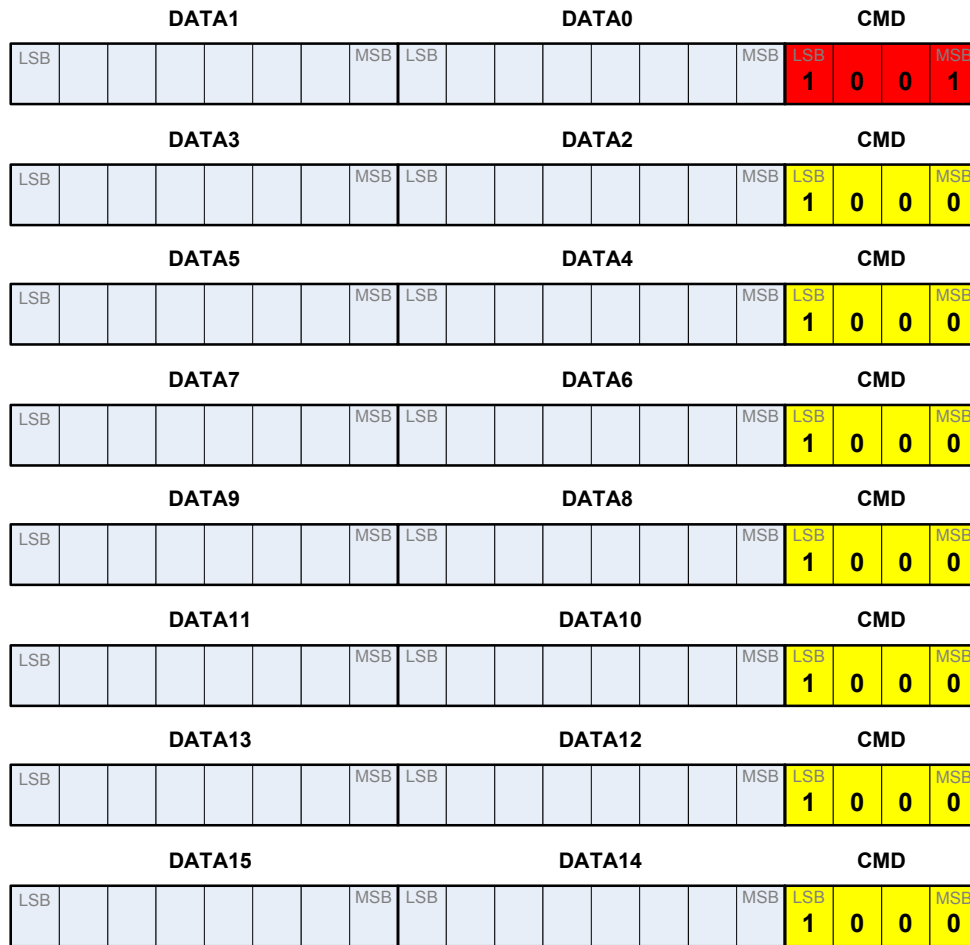| DATA15	DATA14	CMD
LSB … MSB	LSB … MSB	LSB **1 0 0 0** MSB

Figure 18: Frame organisation of the WRITE128 command

The command contains 8 frames. With this command the AS5163 is only receiving frames. This command will transfer the data in the special function registers (SFRs) of the device. The data is not permanent programmed using this command.

Table 15 and Table 16 describe the organization of the OTP data bits.

The access is performed with CMD field set to 0x9. The next 7 frames with CMD field set to 0x1. The 2 bytes of the first command will be written at address 0 and 1 of the SFRs, the 2 bytes of the second at address 2 and 3 and so on in order to cover all the 16 bytes of the 128 SFRs.

Note: It is important to complete always the command. All 8 frames are needed. In case of a wrong command or a communication error a power on reset must be performed.

The device will be delivered with the programmed **Mem_Lock_AMS** OTP bit. This bit locks the content of the factory settings. It is impossible to overwrite this particular region. The written information will be ignored.

8.2.3 READ128

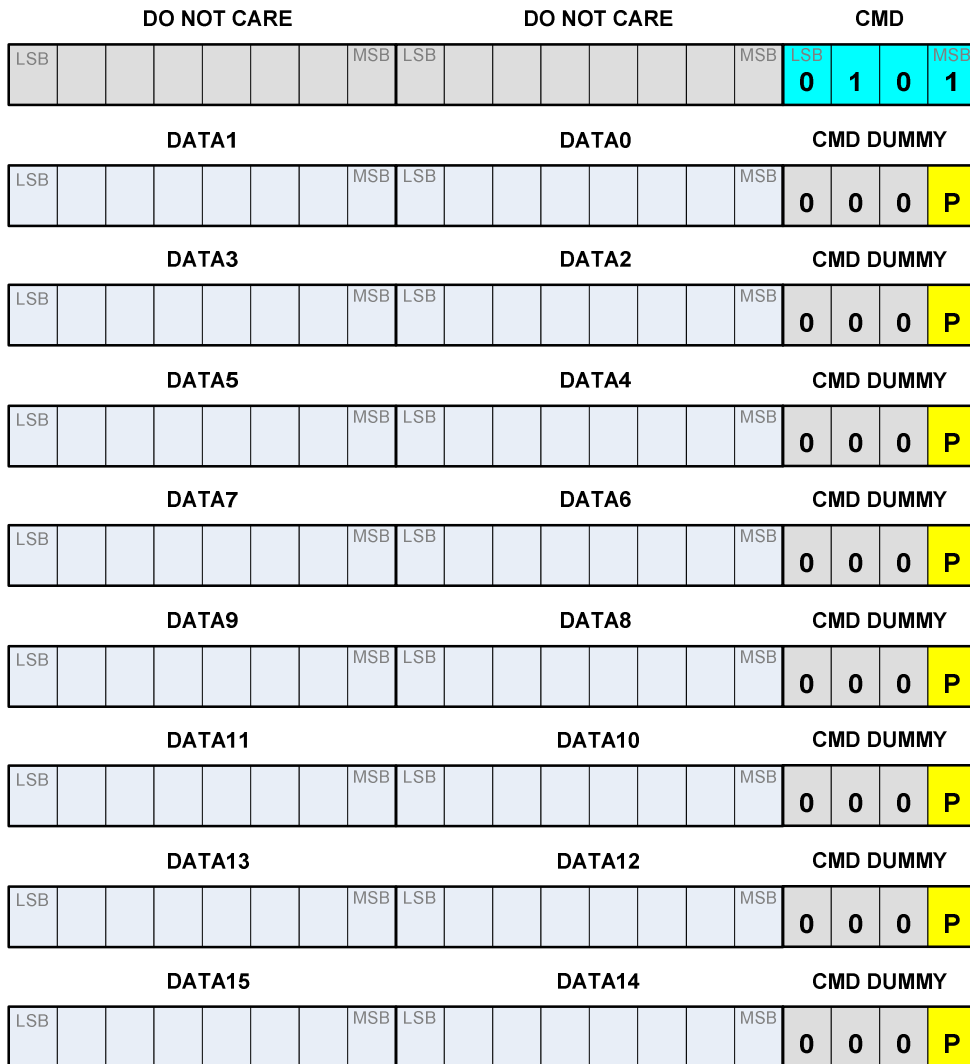Figure 19 shows the format of the frame and the command:

Figure 19: Frame organisation of the READ128 command

The command is composed by a first frame transmitted to the AS5163. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5163 starts to send 8 frames. This command will read the SFRs. The numbering of the data bytes correlates with the address of the related SFR.

An even parity bit is used to guarantee a correct data transmission. Each parity (P) is related to the frame data content of the 16 bit word. The MSB of the CMD dummy (P) is reserved for the parity information.

8.2.4 DOWNLOAD

Figure 20 shows the format of the frame.

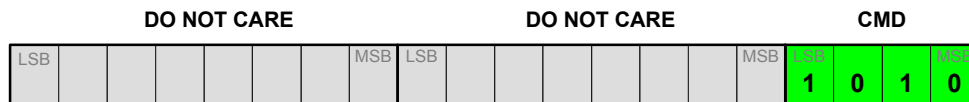|	DO NOT CARE							DO NOT CARE						CMD			
LSB						MSB	LSB						MSB	LSB			MSB
														1	0	1	0

Figure 20: Frame Organisation of the DOWNLOAD command

The command consists of one frame received by the AS5163 (slave communication mode). The OTP cell fuse content will be downloaded into the SFRs.

The access is performed with CMD field set to 0x5.

8.2.5 UPLOAD

Figure 21 shows the format of the frame:

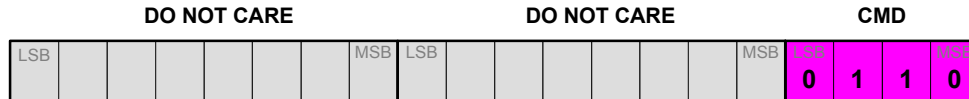|	DO NOT CARE							DO NOT CARE						CMD			
LSB						MSB	LSB						MSB	LSB			MSB
														0	1	1	0

Figure 21: Frame organisation of the UPLOAD command

The command consists of one frame received by the AS5163 (slave communication mode) and transfers the data from the SFRs into the OTP fuse cells. The OTP fuses are not permanent programmed using this command.

The access is performed with CMD field set to 0x6.

8.2.6 FUSE

Figure 22 shows the format of the frame:

	DO NOT CARE							DO NOT CARE						CMD			
LSB						MSB	LSB						MSB	LSB			MSB
														0	0	1	0

Figure 22: Frame organisation of the FUSE command

The command consists of one frame received by the AS5163 (slave communication mode) and it is giving the trigger to permanent program the non volatile fuse elements.

The access is performed with CMD field set to 0x4.

Note: After this command the device starts to program automatically the build in programming procedure. It is not allowed to send other commands during this programming time. This time is specified to 4ms after the last CMD bit.

8.2.7 PASS2FUNC

Figure 23 shows the format of the frame:

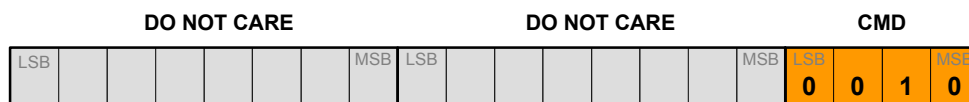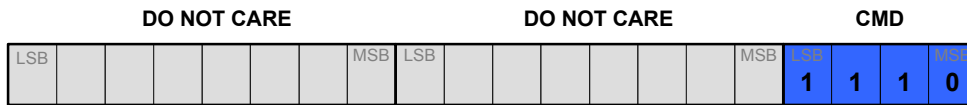| DO NOT CARE						DO NOT CARE						CMD			
LSB					MSB	LSB					MSB	LSB **1**	**1**	**1**	MSB **0**

Figure 23: Frame organisation of the PASS2FUNC command

The command consists of one frame received by the AS5163 (slave communication mode). This command stops the communication receiving mode, releases the reset of the DSP of the AS5163 device and starts to work in functional mode with the values of the SFR currently written.

The access is performed with CMD field set to 0x7.

8.2.8 READ

Figure 24 shows the format of the frame:

ADDR2						ADDR1						CMD			
LSB					MSB	LSB					MSB	LSB **1**	**1**	**0**	MSB **1**

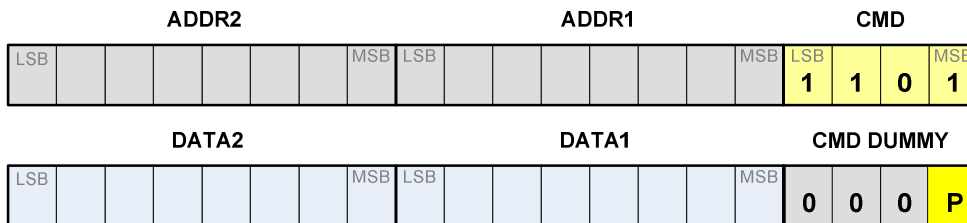| DATA2						DATA1						CMD DUMMY			
LSB					MSB	LSB					MSB	**0**	**0**	**0**	**P**

Figure 24: Frame organisation of the READ command

The command is composed by a first frame sent to the AS5163. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5163 starts to send the second frame transmitted by the AS5163.

The access is performed with CMD field set to 0xB.

When the AS5163 has received the first frame it sends a frame with data value of the address specified in the field of the first frame.

Table 17 shows the possible readable data information for the AS5163 device.

An even parity bit is used to guarantee a correct data transmission. The parity bit (P) is generated by the 16 data bits. The MSB of the CMD dummy (P) is reserved for the parity information.

8.2.9 WRITE

Figure 25 shows the format of the frame:

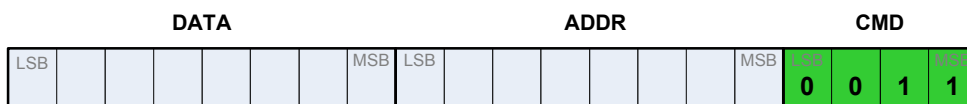| DATA						ADDR						CMD			
LSB					MSB	LSB					MSB	LSB **0**	**0**	**1**	MSB **1**

Figure 25: Frame organisation of the WRITE command

The command consists of one frame received by the AS5163 (slave communication mode). The data byte will be written to the address. The access is performed with CMD field set to 0xC.

Table 17 shows the possible write data information for the AS5163 device.

Note: It is not recommended to access OTP memory addresses using this command.

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8.3 OTP Programming Data

	Data Byte	Bit Nr.	Symbol	Default	Description
Factory Settings	DATA15 (0x0F)	0	AMS_Test	FS	AMS Test area
		1	AMS_Test	FS	
		2	AMS_Test	FS	
		3	AMS_Test	FS	
		4	AMS_Test	FS	
		5	AMS_Test	FS	
		6	AMS_Test	FS	
		7	AMS_Test	FS	
	DATA14 (0x0E)	0	AMS_Test	FS	
		1	AMS_Test	FS	
		2	AMS_Test	FS	
		3	AMS_Test	FS	
		4	ChipID<0>	FS	Chip ID
		5	ChipID<1>	FS	
		6	ChipID<2>	FS	
		7	ChipID<3>	FS	
	DATA13 (0x0D)	0	ChipID<4>	FS	
		1	ChipID<5>	FS	
		2	ChipID<6>	FS	
		3	ChipID<7>	FS	
		4	ChipID<8>	FS	
		5	ChipID<9>	FS	
		6	ChipID<10>	FS	
		7	ChipID<11>	FS	
	DATA12 (0x0C)	0	ChipID<12>	FS	
		1	ChipID<13>	FS	
		2	ChipID<14>	FS	
		3	ChipID<15>	FS	
		4	ChipID<16>	FS	
		5	ChipID<17>	FS	
		6	ChipID<18>	FS	
		7	ChipID<19>	FS	
		0	ChipID<20>	FS	
		1	MemLock_AMS	1	Lock of the Factory Setting Area
Customer Settings	DATA11 (0x0B)	2	KD<0>	0	Kick Down Threshold
		3	KD<1>	0	
		4	KD<2>	0	
		5	KD<3>	0	
		6	KD<4>	0	
		7	KD<5>	0	
	DATA10 (0x0A)	0	ClampLow<0>	0	Clamping Level Low
		1	ClampLow<1>	0	
		2	ClampLow<2>	0	
		3	ClampLow<3>	0	
		4	ClampLow<4>	0	
		5	ClampLow<5>	0	
		6	ClampLow<6>	0	
		7	DITH_DISABLE	0	DAC12/DAC10 Mode
	DATA9 (0x09)	0	ClampHi<0>	0	Clamping Level High
		1	ClampHi<1>	0	
		2	ClampHi<2>	0	
		3	ClampHi<3>	0	
		4	ClampHi<4>	0	
		5	ClampHi<5>	0	
		6	ClampHi<6>	0	
		7	DIAG_HIGH	0	Diagnostic Mode, default =0 for Failure Band Low
	DATA8 (0x08)	0	OffsetIn<0>	0	Offset
		1	OffsetIn<1>	0	
		2	OffsetIn<2>	0	
		3	OffsetIn<3>	0	
		4	OffsetIn<4>	0	
		5	OffsetIn<5>	0	
		6	OffsetIn<6>	0	
		7	OffsetIn<7>	0	

Table 15: OTP Data Organisation Part 1

Note: Factory settings (FS) are used for testing and programming at AMS. These settings are locked (only read access possbile).

DATA7 (0x07)	0	OffsetIn<8>	0	Offset	
	1	OffsetIn<9>	0		
	2	OffsetIn<10>	0		
	3	OffsetIn<11>	0		
	4	OffsetIn<12>	0		
	5	OffsetIn<13>	0		
	6	OP_Mode<0>	0	Selection of Analog="00" or PWM="01"	
	7	OP_Mode<1>	0		
DATA6 (0x06)	0	OffsetOut<0>	0	Output Offset	
	1	OffsetOut<1>	0		
	2	OffsetOut<2>	0		
	3	OffsetOut<3>	0		
	4	OffsetOut<4>	0		
	5	OffsetOut<5>	0		
	6	OffsetOut<6>	0		
	7	OffsetOut<7>	0		
DATA5 (0x05)	0	OffsetOut<8>	0		
	1	OffsetOut<9>	0		
	2	OffsetOut<10>	0		
	3	OffsetOut<11>	0		
	4	KDHYS<0>	0	Kick Down Hysteresis	
	5	KDHYS<1>	0		
	6	PWM Frequency<0>	0	select the PWM frequency (4 frequencies)	
	7	PWM Frequency<1>	0		
DATA4 (0x04)	0	BP<0>	0	Break Point	
	1	BP<1>	0		
	2	BP<2>	0		
	3	BP<3>	0		
	4	BP<4>	0		
	5	BP<5>	0		
	6	BP<6>	0		
	7	BP<7>	0		
DATA3 (0x003)	0	BP<8>	0		
	1	BP<9>	0		
	2	BP<10>	0		
	3	BP<11>	0		
	4	BP<12>	0		
	5	BP<13>	0		
	6	FAST_SLOW	0	Output Data Rate	
	7	EXT_RANGE	0	enables a wider z-Range	
DATA2 (0x02)	0	Gain<0>	0	Gain	
	1	Gain<1>	0		
	2	Gain<2>	0		
	3	Gain<3>	0		
	4	Gain<4>	0		
	5	Gain<5>	0		
	6	Gain<6>	0		
	7	Gain<7>	0		
DATA1 (0x01)	0	Gain<8>	0		
	1	Gain<9>	0		
	2	Gain<10>	0		
	3	Gain<11>	0		
	4	Gain<12>	0		
	5	Gain<13>	0		
	6	Invert_slope	0	Clockwise/counterclockwise rotation	
	7	Lock_OTPCUST	0	Customer Memory Lock	
DATA0 (0x00)	0	redundancy<0>	0	Redundancy Bits	
	1	redundancy<1>	0		
	2	redundancy<2>	0		
	3	redundancy<3>	0		
	4	redundancy<4>	0		
	5	redundancy<5>	0		
	6	redundancy<6>	0		
	7	redundancy<7>	0		

Table 16: OTP Data Organisation Part 2

Data Content:

- **Redundancy (7:0):** For a better programming reliability a redundancy is implemented. In case, the programming of one bit failed this function can be used. With an address (7:0) one bit can be selected and programmed.

- **Lock_OTPCUST** = 1, locks the customer area in the OTP and the device is starting up from now on in operating mode.

- **Invert_Slope** = 1, inverts the output characteristic in analog output mode.

- **Gain (7:0):** With this value one can adjust the steepness of the output slope.

- **EXT_RANGE** = 1, provides a wider z-Range of the magnet by turning off the alarm function.

- **FAST_SLOW** = 1, improves the noise performance due to internal filtering.

- **BP (13:0):** The breakpoint can be set with resolution of 14 bit.

- **PWM Frequency (1:0):** 4 different frequency settings possible. Please refer to Table 10.

- **KDHYS (1:0)** avoids flickering at the KDOWN output (pin 11). For settings refer to Table 12.

- **OffsetOut (11:0)** Output characteristic parameter

- **ANALOG_PWM** = 1, selects the PWM output mode.

- **OffsetIn (13:0)** Output characteristic parameter

- **DIAG_HIGH** = 1: In case of an error, the signal goes into high failure-band.

- **ClampHI (6:0)** sets the clamping level high with respect to VDD.

- **DITH_DISABLE** disables filter at DAC

- **ClampLow (6:0)** sets the clamping level low with respect to VDD.

- **KD (5:0)** sets the kick-down level with respect to VDD.

8.4   Read/Write user data

Area Region	Address	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W USER DATA	0x10	16	CORDIC_OUT[7:0]							
	0x11	17	0	0	CORDIC_OUT[13:8]					
	0x12	18	OCF	COF	0	0	0	0	DSP_RES	R1K_10K
	0x17	23	AGC_VALUE[7:0]							

Read only
Read and Write

Table 17: Read/Write data

Data Content:

Data only for read:

- **CORDIC_OUT(13:0):** 14 bit absolute angular position data.

- **OCF** (**O**ffset **C**ompensation **F**inished): logic high indicates the finished Offset Compensation Algorithm. As soon as this bit is set, the AS5163 has completed the startup and the data is valid.

- **COF** (**C**ordic **O**verflow): Logic high indicates an out of range error in the CORDIC part. When this bit is set, the CORDIC_OUT(13:0) data is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

- **AGC_VALUE (7:0)** magnetic field indication.

Data for write and read:

- **DSP_RES** resets the DSP part of the AS5163 the default value is 0. This is active low. The interface is not affected by this reset.

- **R1K_10K** defines the threshold level for the OTP fuses. Can bit can be changed for verification purpose. A verification of the programming of the fuses is possible. The verification is mandatory after programming.

8.5   Programming Procedure

- Pull-up on out pin;
- VDD=5V;
- Wait startup time, device enters communication mode;
- Write128 command: the trimming bits are written in the SFR memory;
- Read128 command: the trimming bits are read back;
- Upload command: the SFR memory is transferred into the OTP RAM;
- Fuse command: the OTP RAM is written in the Poly Fuse cells.
- Wait fuse time (6 ms);
- Write command (R1K_10K=1): Poly Fuse cells are transferred into the RAM cells compared with 10KOhm resistor;
- Download command: the OTP RAM is transferred into the SFR memory;
- Read128 command: the fused bits are read back;
- Write command (R1K_10K=0): Poly Fuse cells are transferred into the RAM cells compared with 1KOhm resistor;
- Download command: the OTP RAM is transferred into the SFR memory;
- Read128 command: the fused bits are read back;
- Pass2Func command: go back in normal mode.

For Further information please refer to Application Note AN_AS5163-10.

9   Choosing the Proper Magnet

The AS5163 works with a variety of different magnets in size and shape. A typical magnet could be 6mm in diameter and ≥2.5mm in height. Magnetic materials such as rare earth AlNiCo/SmCo5 or NdFeB are recommended. The magnetic field strength perpendicular to the die surface has to be in the range of ±30mT...±70mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic field B_v at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±30mT...±70mT (see Figure 26).
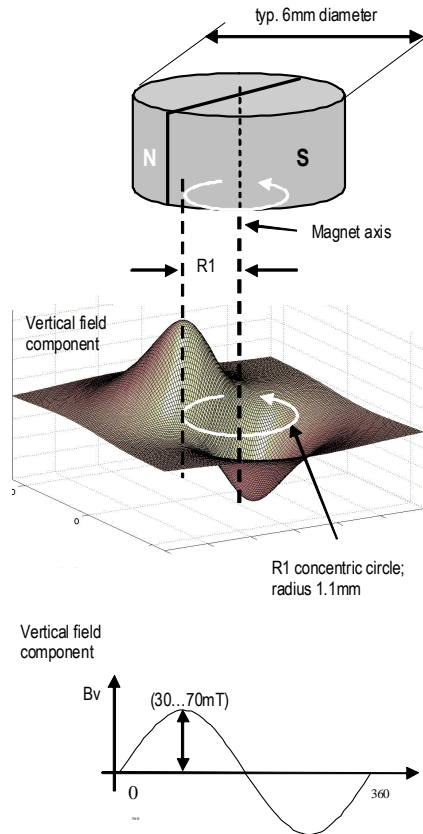
Figure 26: Typical magnet (6x3mm) and magnetic field distribution

9.1 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below:
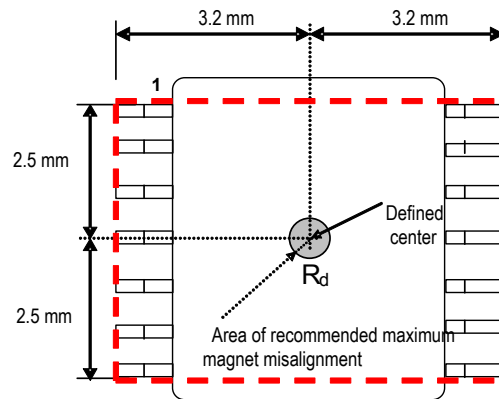
Figure 27: Defined chip center and magnet displacement radius

9.2 Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm (larger magnets allow more displacement) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 27). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by an alarm forcing the output into the failure band.
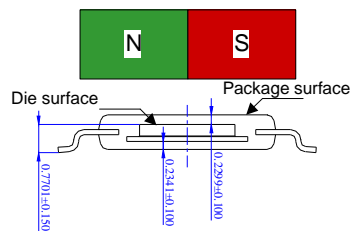
Figure 28: Vertical placement of the magnet

10 Package Drawings and Markings

14-Lead Thin Shrink Small Outline Package TSSOP-14
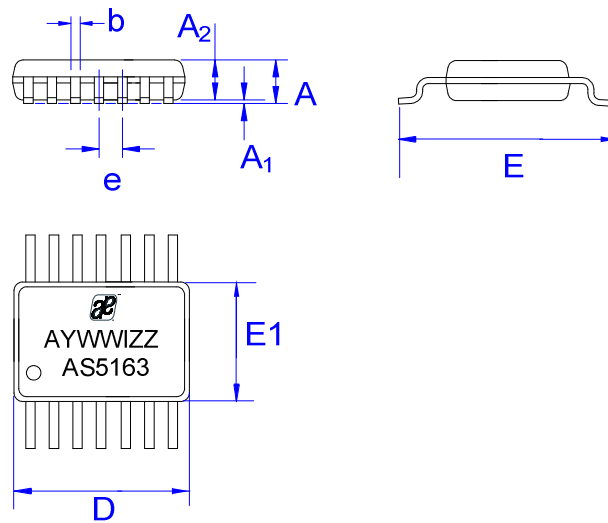
Figure 29: Package Dimensions and Marking

Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			.047
A1	0.05	0.10	0.15	.002	.004	.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e	0.65			.0256		

Table 18: Package Dimensions

Marking: AYWWIZZ

A: Pb-Free Identifier

Y: Last Digit of Manufacturing Year

WW: Manufacturing Week

I: Plant Identifier

ZZ: Traceability Code

JEDEC Package Outline Standard:
MO - 153

Thermal Resistance $R_{th(j-a)}$:
89 K/W in still air, soldered on PCB

11 Ordering Information

The devices are available as standard products, shown in Table 19.

Model	Description	Delivery Form	Package
AS5163HTSU	12 –Bit Programmable Magnetic Rotary Encoder	Tubes	TSSOP 14

Table 19: Ordering Information

12 Revision History

Revision	Date	Owner	Description
1.1	04-Nov-2008	rfu, mub	First draft
1.2	23-Feb-2009	rfu	Timing in communication-protocol, corrections of OTP-table, new structure of chapters
2.02	19-May-2009	rfu, mub	Draft for ES2 + Errata Sheet
2.1	14-July-2009	rfu	rename ALARM_DISABLE to EXT_RANGE, add Rev.History table
2.2	05-Nov-2009	rfu	Update of Digital Protocol (Chapter 7)
2.3	27-Nov-2009	rfu	Remove Digital Protocol (Chapter 7)
2.4	10-Dec-2009	rfu	Update of *Benefits*

Contact

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