National Semiconductor

CLC505
High-Speed, Programmable-Supply Current, Monolithic Op Amp

General Description

The CLC505 is a monolithic, high-speed op amp with a unique combination of high performance, low power consumption, and flexibility of operation. With a 10 to 1 range of supply current programmability (not preset currents, but rather a continuous range "programmed" with a single external resistor, R_p), this amplifier can be used in a wide variety of high-performance applications. Performance (typical) at any supply current is exceptional:

parameter	Supply Current (I_{cc}) 1mA	3.4mA	9mA	Units
-3dB bandwidth	50	100	150	MHz
settling time	35	14	12	nsec
slew rate	800	1200	1700	V/µsec
output current	7	25	45	mA

Even at 10mW power consumption, the CLC505 provides performance far beyond other monolithic op amps, many of which consume nearly 100 times as much power.

The CLC505's combination of high performance, low power consumption, and large signal performance makes the CLC505 ideal for many demanding applications in which power consumption must be minimized. Examples include a variety of remote site equipment such as battery-powered test instrumentation and communications gear. Power is also critical in applications requiring many channels, such as video switching matrices, ATE, and phased-array radar systems.

The CLC505 has been designed for ease of use and has been specified for design confidence and predictability. **The following pages include three complete data sheets, one for operation at 1mA supply current, one at 3.4mA, and one at 9mA.** The CLC505 is also available in several versions specified by the three-letter suffix:

CLC505AJE	-40°C to +85°C	8-pin plastic SOIC
CLC505ALC	-40°C to +85°C	dice

Contact factory for other packages and DESC SMD number.

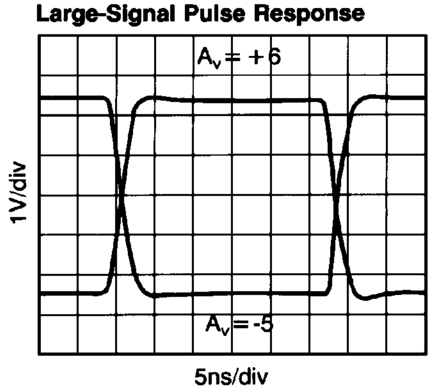
Features

- 10mW power consumption with 50MHz BW
- Single-resistor programming of supply current
- 3.4mA I_{cc} provides 100MHz bandwidth and 14ns settling (0.05%)
- Fast disable capability
- 0.04% differential gain at I_{cc} = 3.4mA
- 0.06% differential phase at I_{cc} = 3.4mA

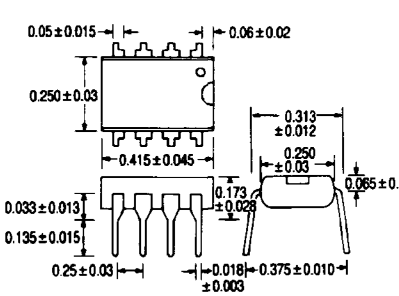
Applications

- Low-power/battery applications
- Remote site instrumentation
- Mobile communications gear
- Video switching matrix
- Phased-array radar

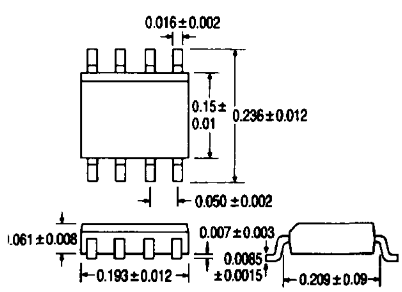
Large-Signal Pulse Response



Package Dimensions



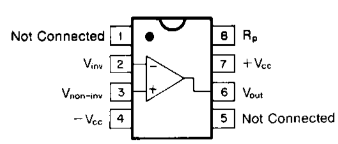
8-pin plastic DIP



8-pin plastic SOIC

Pinout

DIP & SOIC



CLC505 Electrical Characteristics (A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, C_p = 100pF; unless specified)

		SUPPLY CURRENT I_{CC} (TYP) = 9mA R_P = 33kΩ, R_L = 250Ω					
PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC505AJ	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	Vout<$2V_{pp}$	150	>115	>115	>100	MHz	SSBW
-3dB large signal	Vout<$5V_{pp}$	135	>95	>95	>80	MHz	LSBW
gain flatness	Vout<$2V_{pp}$						
peaking	<25/20/10MHz**	0	<0.4	<0.3	<0.4	dB	GFPL
peaking	>25/20/10MHz**	0	<0.6	<0.5	<0.6	dB	GFPH
rolloff	<50/40/20MHz**	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 50/40/20MHz**	0.6	<1.0	<1.0	<1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.3	<3.0	<3.0	<3.5	ns	TRS
	5V step	2.6	<3.7	<3.7	<4.4	ns	TRL
settling time to 0.1/0.05/0.05%**	2V step	12	<16	<16	<16	ns	TSP
overshoot	2V step	5	<15	<12	<15	%	OS
slew rate (for A_v +2)[2]		1700	>1000	>1200	>1200	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	$2V_{pp}$, 20/10/5MHz**	−50	<−40	<−45	<−45	dBc	HD2
3rd harmonic distortion	$2V_{pp}$, 20/10/5MHz**	−65	<−55	<−55	<−55	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−156	<−154	<−154	<−153	dBm(1Hz)	SNF
integrated noise	1MHz to 200/200/100MHz**	50	<65	<65	<70	μV	INV
differential gain[3]		0.04	—	—	—	%	DG
differential phase[3]		0.06	—	—	—	°	DP
STATIC, DC PERFORMANCE							
* input offset voltage		2	<±12.8	<±8.0	<±14	mV	VIO
average temperature coefficient		30	<±50	—	<±50	μV/°C	DVIO
* input bias current	non-inverting	8	<±36	<±18	<±18	μA	IBN
average temperature coefficient		80	<±225	—	<±100	nA/°C	DIBN
* input bias current	inverting	10	<±60	<±38	<±40	μA	IBI
average temperature coefficient		80	<±275	—	<±125	nA/°C	DIBI
power supply rejection ratio		50	>45	>48	>45	dB	PSRR
common mode rejection ratio		50	>45	>48	>45	dB	CMRR
* **supply current**	**no load, quiescent**	**9**	**<11**	**<11**	**<12**	**mA**	**ICC**
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	1200	>400	>800	>1600	kohm	RIN
	capacitance	1	<2	<2	<2	pF	CIN
output impedance	at DC	0.2	<1.2	<0.3	<0.2	ohm	RO
output voltage range	no load	±3.3	>±2.8	>±3.0	>±3.0	V	VO
common mode input range	for rated performance	±2.2	>±1.5	>±1.8	>±2.0	V	CMIR
output current	−40°C to +85°C	±45	>±20	>±36	>±36	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{CC}		±7V
I_{out}	is short circuit protected to ground, maximum reliability maintained if I_{out} does not exceed (except A8 should not exceed 35mA over military temperature range.)	60mA
common mode input voltage		$\pm V_{CC}$
differential input voltage		10V
junction temperature range		+150°C
operating temperature range		
	AJ:	−40°C to + 85°C
storage temperature range		−65°C to + 150°C
lead solder duration (+300°C)		10 sec
ESD (human body model)		2000V

Miscellaneous Ratings

Recommended gain range: +2 to +21, -1 to -20

NOTES:

* AJ	100% tested at +25°C at Icc = 3.4mA.
note 1:	Not applicable due to output current limitations.
note 2:	See text on the back page of the data sheet
note 3:	Differential gain and phase is characterized with a $1V_{pp}$ equivalent video signal, 0-100 IRE, 40 IRE_{pp}, and 0IRE = 0V at the load resistor and 3.58 MHz.

CLC505 Electrical Characteristics ($A_V = +6, V_{CC} = \pm 5V, R_f = 1000\Omega, C_p = 100pF$; unless specified)

SUPPLY CURRENT I_{CC} (TYP) = 3.4mA $R_p = 100k\Omega, R_L = 500\Omega$				SUPPLY CURRENT I_{CC} (TYP) = 1mA $R_p = 300k\Omega, R_L = 1000\Omega$					
TYP	MAX & MIN RATINGS			TYP	MAX & MIN RATINGS			UNITS	SYMBOL
+25°C	−40°C	+25°C	+85°C	+25°C	−40°C	+25°C	+85°C		
100	>80	>80	>65	50	>30	>35	>30	MHz	SSBW
80	>50	>50	>40	33	—[1]	>20	>18	MHz	LSBW
0	<0.3	<0.2	<0.3	0	<0.2	<0.1	<0.2	dB	GFPL
0	<0.5	<0.4	<0.5	0	<0.3	<0.2	<0.3	dB	GFPH
0.2	<1.0	<1.0	<1.3	0.5	<1.0	<1.0	<1.3	dB	GFR
0.5	<1.0	<1.0	<1.2	0.3	<0.8	<0.8	<1.0	°	LPD
3.5	<4.4	<4.4	<5.4	7	<12	<10	<12	ns	TRS
4.4	<7.0	<7.0	<8.8	9	—[1]	<18	<20	ns	TRL
14	<22	<22	<22	35	<70	<60	<60	ns	TSP
2	<12	<10	<12	0	<8	<5	<8	%	OS
1200	>700	>800	>800	800	>500	>600	>600	V/µs	SR
−55	<−40	<−45	<−45	−55	<−40	<−45	<−45	dBc	HD2
−65	<−55	<−55	<−55	−65	<−55	<−55	<−55	dBc	HD3
−155	<−153	<−153	<−152	−152	<−150	<−150	<−149	dBm(1Hz)	SNF
56	<70	<70	<80	55	<70	<70	<80	µV	INV
0.04	—	—	—	0.1	—	—	—	%	DG
0.06	—	—	—	0.1	—	—	—	°	DP
3	<±11.8	<±7.0	<±13	3	<±13.0	<±7.0	<±14.5	mV	VIO
40	<±60	—	<±60	50	<±75	—	<±75	µV/°C	DVIO
2	<±12	<±6	<±6	1	<±5.0	<±2.5	<±2.5	µA	IBN
30	<±75	—	<±50	10	<±32	—	<±30	nA/°C	DIBN
4	<±22	<±14	<±15	2	<±10.0	<±7.0	<±8.0	µA	IBI
40	<±100	—	<±60	20	<±38	—	<±35	nA/°C	DIBI
50	>45	>48	>45	50	>45	>48	>45	dB	PSRR
50	>45	>48	>45	50	>45	>48	>45	dB	CMRR
3.4	**<3.8**	**<3.8**	**<4.2**	**1.0**	**<1.4**	**<1.3**	**<1.4**	**mA**	**ICC**
3000	>1000	>2000	>4000	7500	>2500	>5000	>10000	kohm	RIN
1	<2	<2	<2	1	<2	<2	<2	pF	CIN
0.2	<1.6	<0.5	<0.2	0.5	<3.0	<1.0	<0.5	ohm	RO
±3.3	>±2.8	>±2.7	>±3.0	±3.3	>±2.5	>±3.0	>±3.0	V	VO
±2.2	>±1.5	>±1.8	>±2.0	±2.2	>±1.5	>±1.8	>±2.0	V	CMIR
±25	>±10	>±18	>±18	±7	>±3.0	>±5	>±5	mA	IO
±25	>±9	>±18	>±18	±7	>±2.5	>±5	>±5	mA	IO

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
AJE	60°C/W	140°C/W

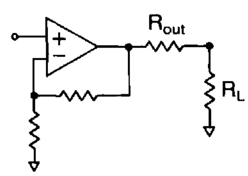
Reliability Information

Transistor Count	30

Notes

Conditions are different for the three supply currents:

I_{CC}	R_L	R_{OUT}	A_V
9mA	75Ω	75Ω	+2
3.4mA	500Ω	0Ω	+6
1mA	1000Ω	0Ω	+6

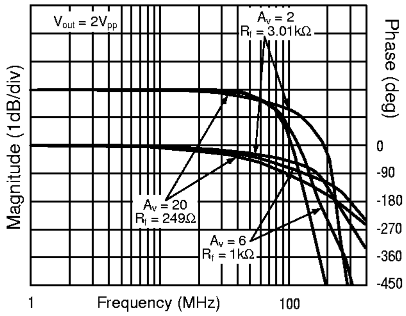


**** xx/yy/zz MHz indicates that the CLC505 is specified at xxMHz for I_{cc} = 9mA, yyMHz for I_{cc}=3.4mA, and zzMHz for I_{cc}=1mA.**

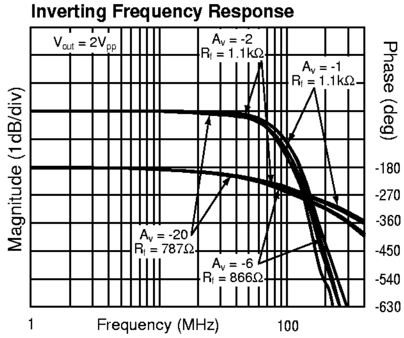
Typical Performance Characteristics (T_A = 25°, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)

I_{CC} = 9mA, R_L = 250Ω

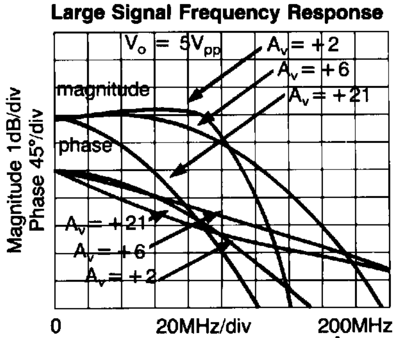
Non-Inverting Frequency Response



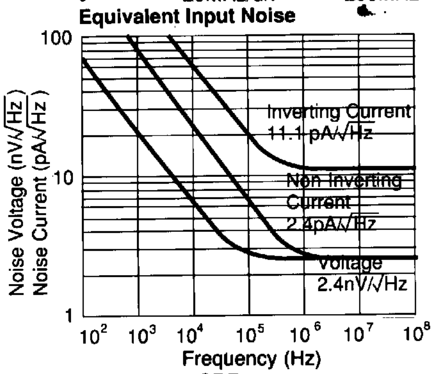
Inverting Frequency Response



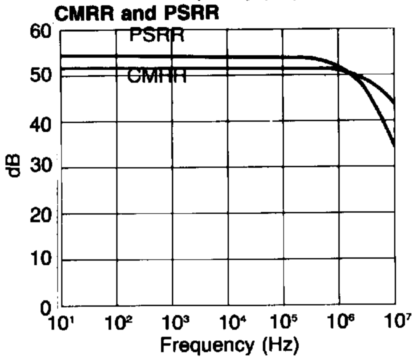
Large Signal Frequency Response



Equivalent Input Noise

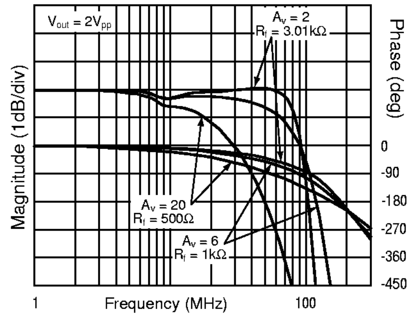


CMRR and PSRR

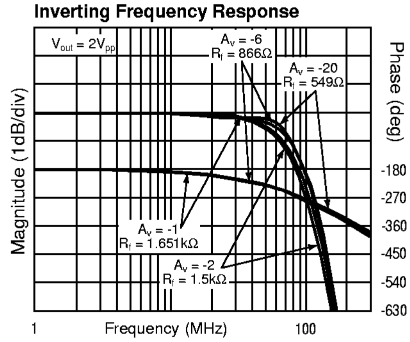


I_{CC} = 3.4mA, R_L = 500Ω

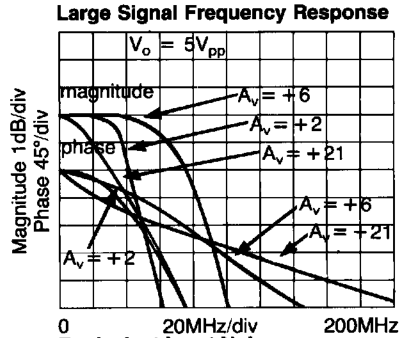
Non-Inverting Frequency Response



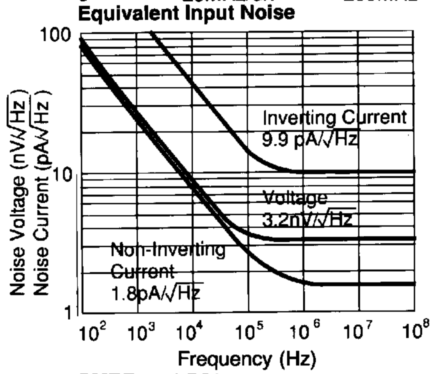
Inverting Frequency Response



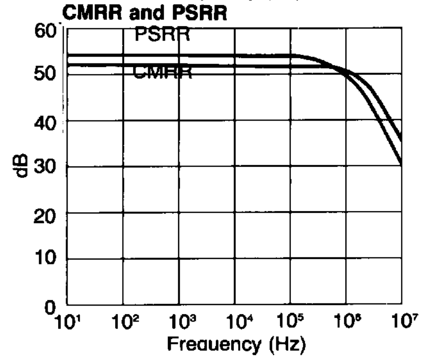
Large Signal Frequency Response



Equivalent Input Noise

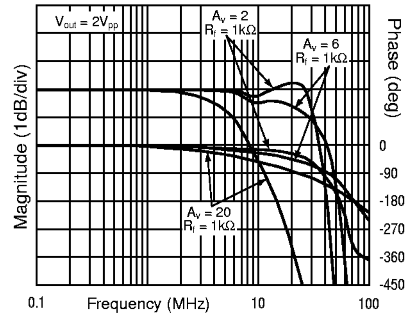


CMRR and PSRR

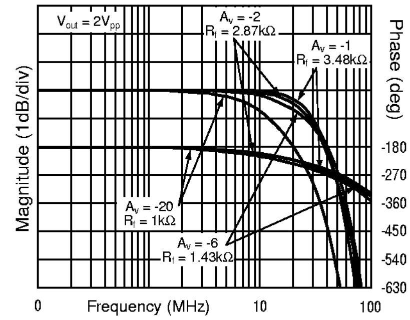


I_{CC} = 1mA, R_L = 1000Ω

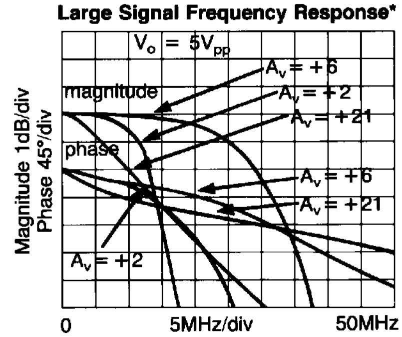
Non-Inverting Frequency Response



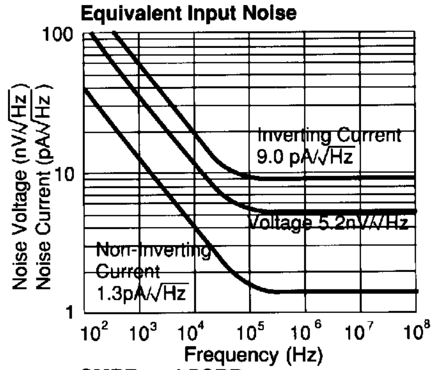
Inverting Frequency Response



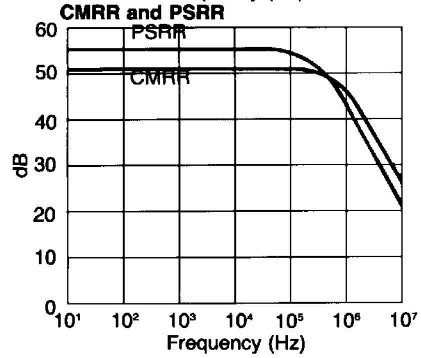
Large Signal Frequency Response*



Equivalent Input Noise



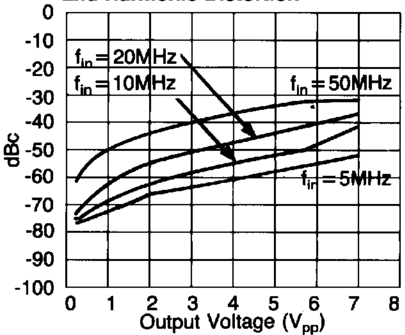
CMRR and PSRR



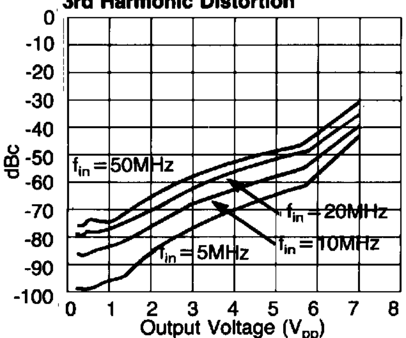
Typical Performance Characteristics ($T_A = 25°$, $A_V = +6$, $V_{CC} = \pm5V$, $R_f = 1000\Omega$, $V_H = +3V$, $C_p = 100pF$)

$I_{cc} = 9mA$, $R_L = 250\Omega$

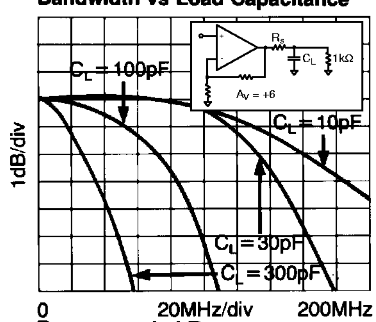
2nd Harmonic Distortion



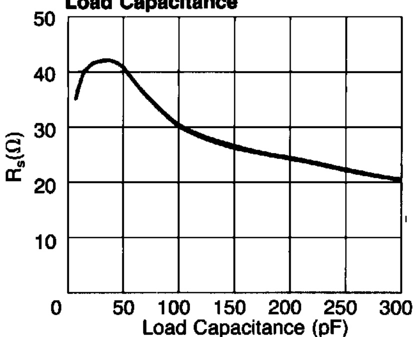
3rd Harmonic Distortion



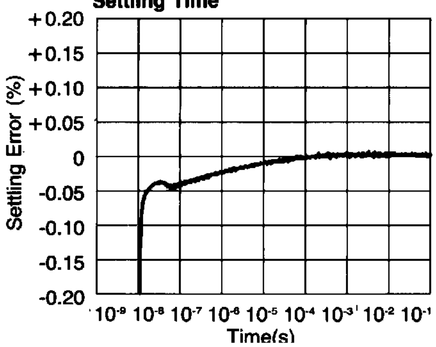
Bandwidth vs Load Capacitance



Recommended R_s vs Load Capacitance

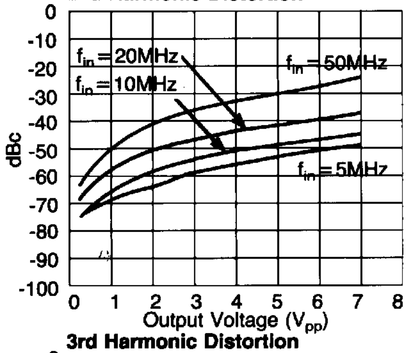


Settling Time

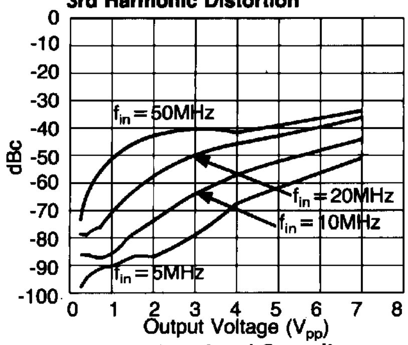


$I_{cc} = 3.4mA$, $R_L = 500\Omega$

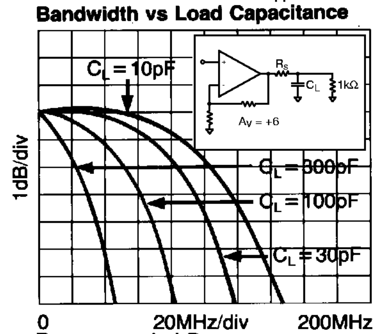
2nd Harmonic Distortion



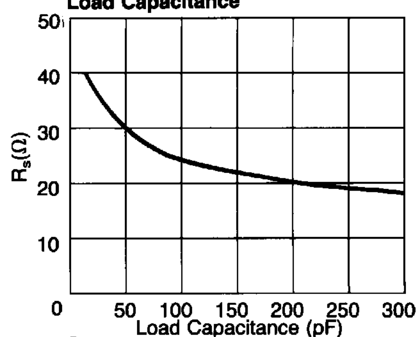
3rd Harmonic Distortion



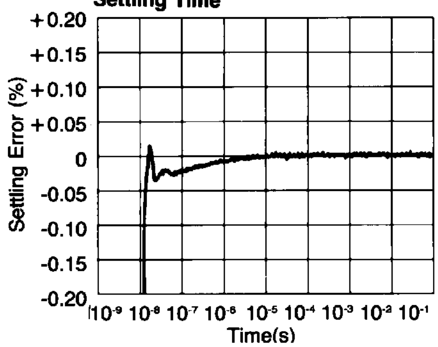
Bandwidth vs Load Capacitance



Recommended R_s vs Load Capacitance

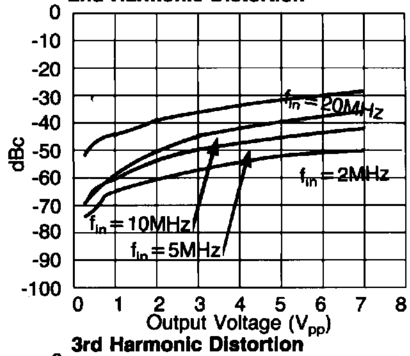


Settling Time



$I_{cc} = 1mA$, $R_L = 1000\Omega$

2nd Harmonic Distortion



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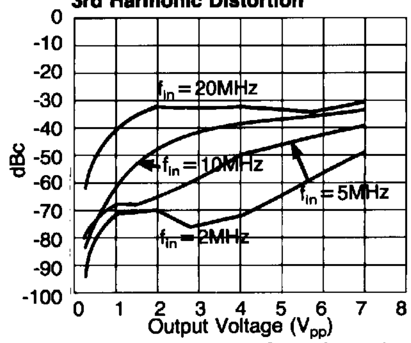
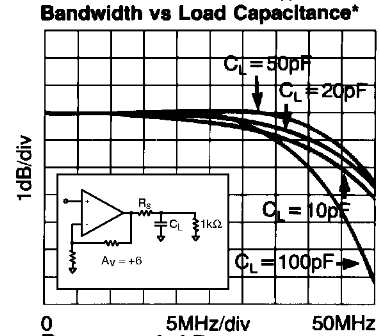
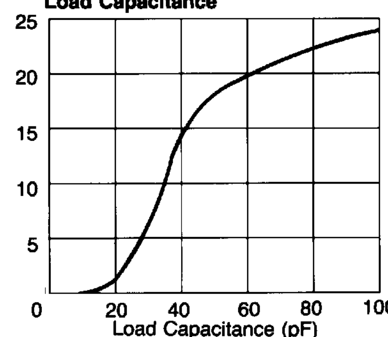


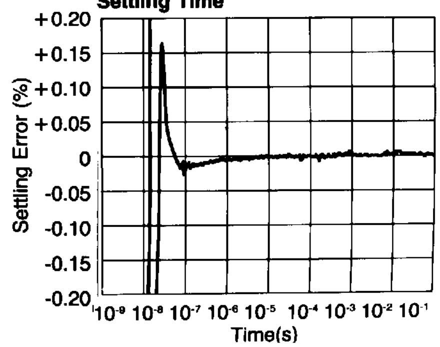
Bandwidth vs Load Capacitance*



Recommended R_s vs Load Capacitance



Settling Time



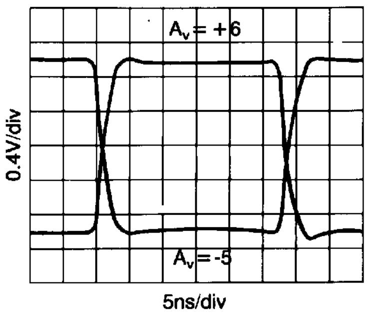
Typical Performance Characteristics (T_A = 25°, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)

I_{cc} = 9mA, R_L = 250Ω

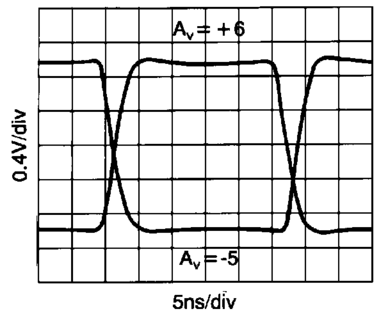
I_{cc} = 3.4mA, R_L = 500Ω

I_{cc} = 1mA, R_L = 1000Ω

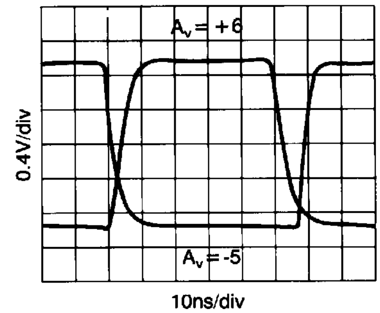
Small-Signal Pulse Response



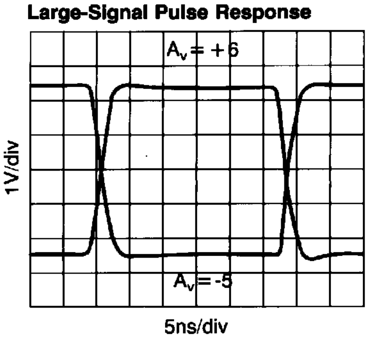
Small-Signal Pulse Response



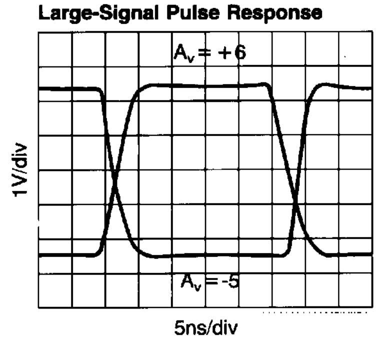
Small-Signal Pulse Response*



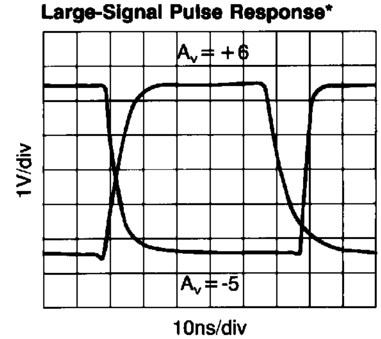
Large-Signal Pulse Response



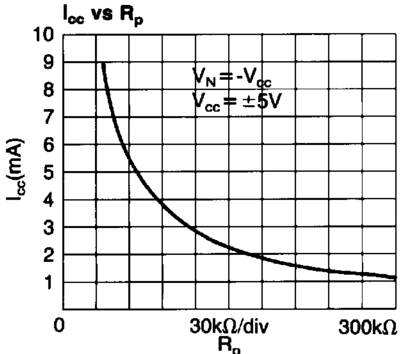
Large-Signal Pulse Response



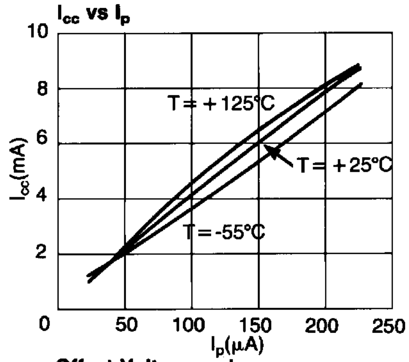
Large-Signal Pulse Response*



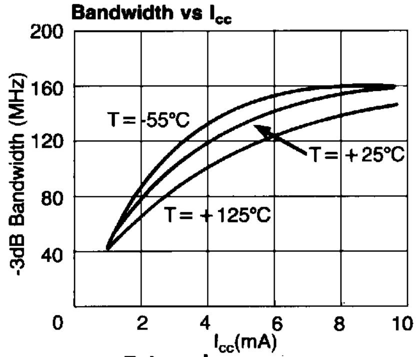
I_{cc} vs R_p



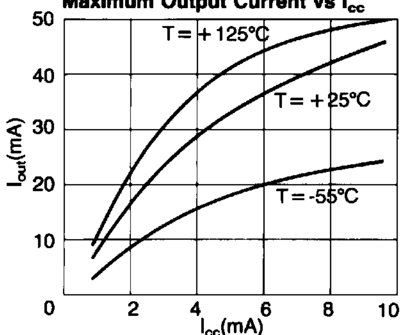
I_{cc} vs I_p



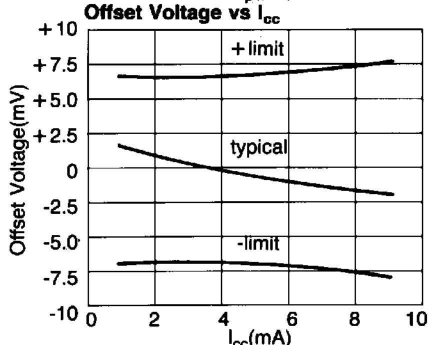
Bandwidth vs I_{cc}



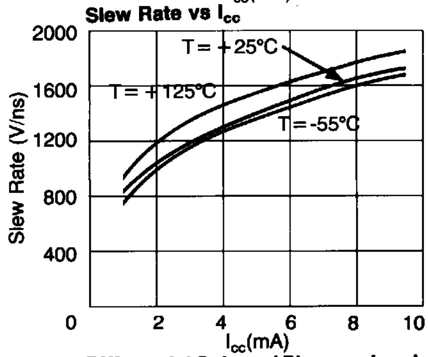
Maximum Output Current vs I_{cc}



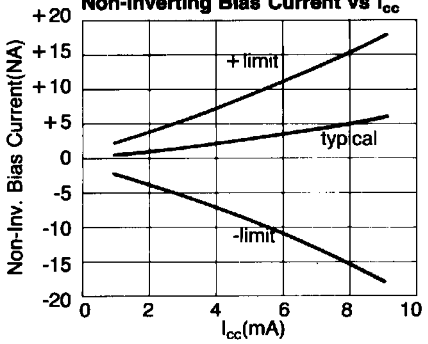
Offset Voltage vs I_{cc}



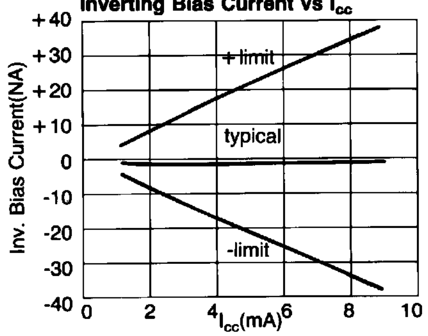
Slew Rate vs I_{cc}



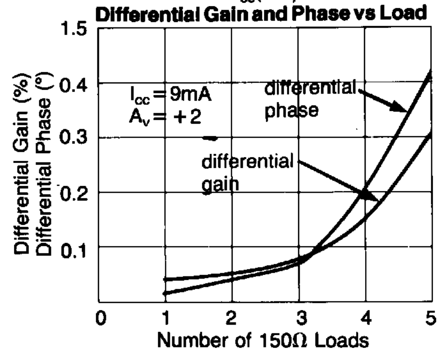
Non-Inverting Bias Current vs I_{cc}

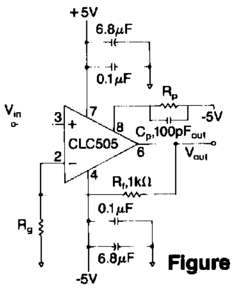


Inverting Bias Current vs I_{cc}



Differential Gain and Phase vs Load

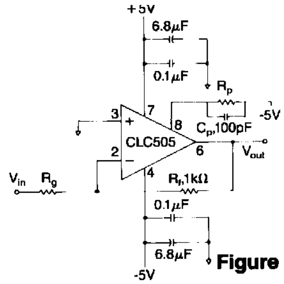




$$A_V = 1 + \frac{R_f}{R_g}$$

note: C_p may also be connected from pin 8 to ground

Figure 1: recommended non-inverting gain circuit



$$A_V = \frac{-R_f}{R_g}$$

note: C_p may also be connected from pin 8 to ground

Figure 2: recommended inverting gain circuit

Description

The CLC505 is a progammable-supply current, current-feedback operational amplifier. Supply current and consequently dynamic performance can be easily adjusted by selecting the value of a single external resistor (R_p). This capability is reflected in the datasheet by three complete sets of specifications, each at a different value of supply current.

Selecting an Operating Point

The operating point is determined by the supply current, which in turn is determined by current (I_p) flowing out of pin 8. As the supply current is reduced the following effects will be observed:

Specification	**Effect as I_{cc} decreases**
bandwidth	decreases
rise time	increases
output drive	decreases
input bias current	decreases
input impedance	increases (see source impedance discussion)

Both the specification pages and the plot pages illustrate these effects to help make the supply current vs. performance tradeoff. Performance is specified and tested at I_{cc}=1mA, 3.4mA, and 9mA as indicated in the data sheet. (Note some test conditions and especially the load resistance are different for the three supply current settings.) The performance plots show typical performance for all three supply current levels (again, with different load resistors for the various supply currents). Finally, the last set of plots show graphically the relationship between the supply current (I_{cc}) and various performance parameters, as well as I_{cc} vs. the programming current, I_p.

When making the supply current vs. performance tradeoff, it is first a good idea to see if one of the standard operating points (I_{cc}=9mA, 3.4mA, or 1mA) fits your application. If it does, performance guaranteed on the specification pages will apply directly to your application. In addition, the value of R_p may be obtained directly from the specification page.

The following discussion will assist in selecting I_{cc} for applications that cannot operate at one of the specified supply current settings.

The typical performance plots should be used to select a value of I_{cc} suitable to your application's TYPICAL requirement for critical specifications. Then, use the performance plots and the max/min limits on the specification pages to interpolate between values of I_{cc} to estimate max/min values in your application.

From the selected value of I_{cc}, the "programming current" (I_p) may be easily calculated:

$$I_p = I_{cc} / 39$$

The plot of I_{cc} vs I_p in the plot pages shows this relationship graphically. Knowing I_p leads to a direct calculation of R_p

$$R_p = [(+V_{cc}-1.6)-V_n] / I_p$$

$$R_p = 8.4/I_p \text{ (for } +V_{cc} = +5V \text{ and } V_n = -5V)$$

V_n is the voltage externally applied to R_p. (Throughout the data sheet and in most applications, V_n is $-V_{cc}$ or more specifically, -5V.) The term ($+V_{cc}$-1.6V) is the voltage at pin 8.

Since the op amp side of R_p is very nearly at a fixed voltage (V_{cc}-1.6V), I_p is a function of V_n and R_p. V_n, therefore does not have to be connected to $-V_{cc}$ as long as R_p is chosen accordingly. This is beneficial in applications where non-standard supply voltages are used or when there is a need to power down the op amp via digital logic control.

First, an operating point needs to be established as discussed above. From this, I_p is obtained. I_p, in concert with the available V_n, determines R_p.

Example

An application requires that V_{cc}= +/-3V and performance in the 1mA operating point range. The required I_p can therefore be determined as discussed above.

$$I_p = 26\mu A$$

R_p is connected from pin 8 to $-V_{cc}$ and V_{cc}= +/-3V. Now calculate R_p under new conditions:

$$R_p = [(+V_{cc}-1.6V)-(-V_{cc})] / I_p$$

$$R_p = [(+3V-1.6V)-(-3V)] / 26\mu A$$

$$R_p = 169k\Omega$$

The CLC505 will have performance similar to R_p=300kΩ shown on the datasheet, but with 40% less power dissipation due to the reduced supply voltages. (The op-amp will also have a more restricted common-mode range and output swing.) This calculation is approximate and a prudent design would include substantial performance margin for max/min limits. Comlinear application engineers are available for assistance.

Dynamic Shutdown Capability

The CLC505 may be powered on and off very quickly by controlling the voltage applied to R_p. If R_p is connected between pin 8 and the output of a CMOS gate powered from +/-5V supplies, the gate can be used to turn the amplifier on and off. This is shown in figure 3 below:

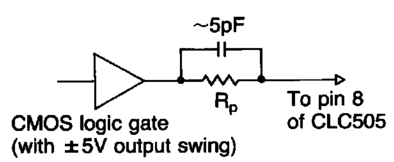


Figure 3: dynamic control of power consumption

When the gate output is switched from high to low, the CLC505 will turn on. In the off state, the supply current typically reduces to 0.2mA or less. The speed with which the CLC505 turns on or off is limited by the capacitance at pin 8. To improve switching time, a speed up capacitor from the gate output to pin 8 is recommended. The value of this capacitor will depend on the total capacitance connected to pin 8 and is best established experimentally. Turn-on and turn-off times of 100ns to 200ns are achievable with ordinary CMOS gates.

Example:

An open collector logic device is used to dynamically control the power dissipation of the circuit. Here, the desired connection for R_p is from pin 8 to the open collector logic device.

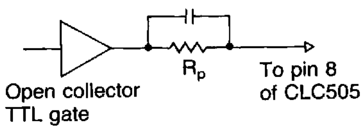


Figure 4: controlling power on state with TTL logic

When the logic gate goes low, the CLC505 is turned on. Performance desired is that given for $I_{cc}=3.4mA$ under standard conditions. From the I_{cc} vs I_p plot, $I_p=84\mu A$. Then calculating R_p:

$$R_p = [(+V_{cc}-1.6V)-(V_n)]/I_p$$
$$R_p = [(+5V-1.6V)-(0)]84\mu A$$
$$R_p = 40k\Omega$$

NOTE: The rapid turn on and off ability of the CLC505 is not recommended for signal isolation applications (such as multiplexing). While the power dissipation of the amplifier drops in the off state, the amplifier may still have some gain at low frequencies.

Slew Rate

Slew rate limiting is a nonlinear response which occurs in amplifiers when the output voltage swing approaches hard, abrupt limits in the speed at which it can change. In most applications, this results in an easily identifiable "slew rate" as well as a dramatic increase in distortion for large signal levels. The CLC505 has been designed to provide enough slew rate to avoid slew rate limiting in most circuit configurations. The large signal ($5V_{pp}$) bandwidth of 80MHz at $I_{cc}=3.4mA$, therefore, is only slightly less than the 100MHz small signal bandwidth. The result is a low-distortion, linear system for both small signals *and* large signals.

The CLC505 reaches slew rate limits only for low non-inverting gains. In other words, slew rate limiting is constrained by common mode voltage swings at the input. (This is different from traditional slew rate constraints.) The large-signal frequency response plot at a gain of +2 shows a break in the response, which shows that a slew rate limit has been reached. Note also that the frequency response plots at gain of +21 show that the large signal and small signal responses are nearly identical.

Differential Gain and Phase

Differential gain and phase are measurements useful primarily in composite video channels. They are measured by monitoring the gain and phase changes of a high frequency carrier (3.58MHz typically) as the output of the amplifier is swept over a range of DC voltages.

Specifications for the CLC505 include differential gain and phase. The test signals used are based on a $1V_{pp}$ video level. Test conditions used are the following:

DC sweep range:	0 to 100 IRE units (black to white)
Carrier:	3.58MHz at 40 IRE units peak to peak

The amplifier conditions are significantly different for the three values of supply current specified. At $I_{cc}=9mA$, the amplifier is specified for a gain of +2 and 150Ω load (for a backmatched 75Ω system). IRE amplitudes at $I_{cc}=9mA$, are referred to the 75Ω load resistor.

At $I_{cc}=1mA$ and $I_{cc}=3.4mA$, the CLC505 is less capable of driving a 150Ω load due to output current limitations. For this reason lighter loads are used and a termination resistor is omitted. The gain and load resistance for $I_{cc}=3.4mA$ are $A_v=+6$ and $R_L=500\Omega$. The gain and load resistance for $I_{cc}=1mA$ are $A_v=+6$ and $R_L=1K\Omega$.

Source Impedance

For best results, source impedance in the non-inverting circuit configuration (see Figure 1) should be kept below 5kΩ. Above 5kΩ it is possible for oscillation to occur, depending on other circuit parasitics. For high signal source impedances, a resistor with a value of less than 5kΩ may be used to terminate the non-inverting input to ground.

Feedback Resistor

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value resistor. The CLC505 provides optimum performance with a 1kΩ feedback resistor. Furthermore, the specifications shown on the previous pages are valid only when a 1kΩ feedback resistor is used. Selection of an incorrect value can lead to severe rolloff in frequency response (if the resistor value is too large) or peaking or oscillation (if the value is too low).

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC505 are available.