19-0587; Rev 0; 8/06

High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications

General Description

The MAX8660/MAX8661 power management ICs (PMICs) power Intel XScale® applications processors in smart cellular phones, PDAs, Internet appliances, and other portable devices.

Four step-down DC-DC outputs, three linear regulators, and an 8th always-on LDO are integrated with power-management functions. Two dynamically controlled DC-DC outputs power the processor core and internal memory. Two other DC-DC converters power I/O, memory, and other peripherals. Additional functions include on/off control for outputs, low-battery detection, reset output, and a 2-wire I^2C† serial interface. The MAX8661 functions the same as the MAX8660, except it lacks the REG1 step-down regulator and the REG7 linear regulator.

All step-down DC-to-DC outputs use fast 2MHz PWM switching and tiny external components. They automatically switch from PWM to high-efficiency light-load operation to reduce operating current and extend battery life. In addition, a forced PWM option allows low-noise operation at all loads. Overvoltage lockout protects the device against inputs up to 7.5V.

Applications

PDAs, Palmtops, and Wireless Handhelds

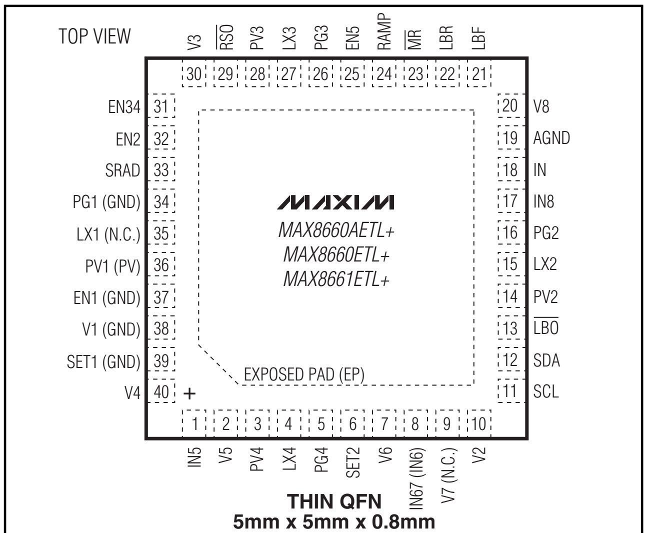
Smart Cell Phones

Personal Media Players

Portable GPS Navigation

Digital Cameras

Pin Configuration



THIN QFN
5mm x 5mm x 0.8mm

( ) ARE FOR THE MAX8661

Features

- ♦ **Optimized for Intel XScale Processors**
- ♦ **Protected to 7.5V—Shutdown Above 6.3V**
- ♦ **Four Synchronous Step-Down Converters**
  REG1, REG2, REG3, REG4
- ♦ **Four LDO Regulators**
  REG5, REG6, REG7, REG8
- ♦ **2MHz Switching Allows Small Components**
- ♦ **Low, 20µA Deep-Sleep Current**
- ♦ **Low-Battery Monitor and Reset Output**

Ordering Information

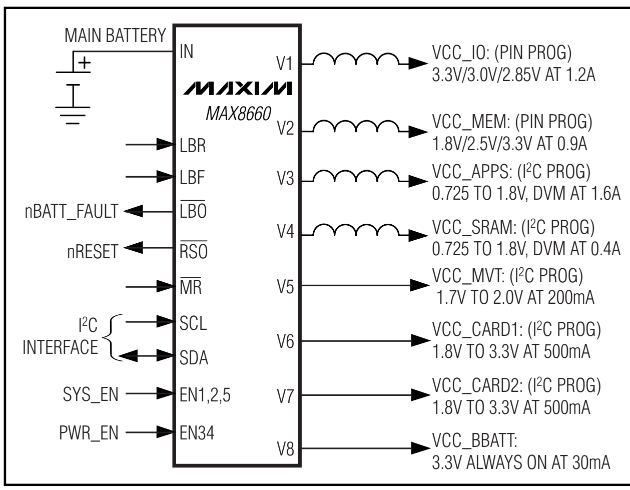
PART	PIN-PACKAGE	PKG CODE	OPTIONS
MAX8660ETL+	40 Thin QFN 5mm x 5mm	T4055-1	V1: 3.3V, 3.0V, 2.85V V2: 3.3V, 2.5V, 1.8V
MAX8660AETL+*	40 Thin QFN 5mm x 5mm	T4055-1	V1: 2.5V, 2.0V, 1.8V V2: 2.5V, 2.0V, 1.8V
MAX8661ETL+	40 Thin QFN 5mm x 5mm	T4055-1	No REG1 and REG7 V2: 3.3V, 2.5V, 1.8V

Note: *All devices are specified over the -40°C to 85°C operating temperature range.*

+Denotes lead-free package.

**Future product—contact factory for availability.*

Simplified Functional Diagram



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications

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ABSOLUTE MAXIMUM RATINGS

IN, IN5, IN6, IN67, EN2, EN34, EN5, $\overline{LBO}$, $\overline{RSO}$, $\overline{MR}$, SET1, SET2, V1, V2, V3, V4, SCL, SDA, SRAD to AGND....-0.3V to +7.5V
LBF, LBR, EN1, RAMP to AGND ....-0.3V to (V_{IN} + 0.3V)
V8 to AGND....-0.3V to (V_{IN8} + 0.3V)
V5 to AGND....-0.3V to (V_{IN5} + 0.3V)
V6, V7 to AGND....-0.3V to (V_{IN67} + 0.3V)
PV1 to PG1 ....-0.3V to +7.5V
PV2 to PG2 ....-0.3V to +7.5V
PV3 to PG3 ....-0.3V to +7.5V
PV4 to PG4 ....-0.3V to +7.5V
PV, PV1, PV2, PV3, PV4, IN8 to IN ....-0.3V to +0.3V
LX1 Continuous RMS Current (Note 1) 2.3A
LX2 Continuous RMS Current (Note 1) 2.0A
LX3 Continuous RMS Current (Note 1) 2.6A
LX4 Continuous RMS Current (Note 1) 1.0A
PG1, PG2, PG3, PG4, EP to AGND....-0.6V to +0.6V
GND to AGND ....-0.3V to +0.3V
All REGx Output Short-Circuit Duration....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 35.7mW/°C above +70°C)....2857mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: LX_ has internal clamp diodes to PG_ and PV_. Applications that forward bias these diodes must take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PV1, PV2, PV3, PV4, IN, IN8 Supply Voltage Range	V_{IN}	PV1, PV2, PV3, PV4, IN, and IN8 must be connected together externally		2.6		6.0	V
IN Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising		2.250	2.400	2.550	V
		V_{IN} falling		2.200	2.350	2.525	
IN Overvoltage-Lockout Threshold	V_{OVLO}	V_{IN} rising		6.20	6.35	6.50	V
		V_{IN} falling		6.00	6.15	6.30	
Input Current	I_{IN}+ I_{PV1}+I_{PV2}+ I_{PV3}+I_{PV4}+ I_{IN5}+ I_{IN67}+ I_{IN8}	No load; SDA = SCL = V8	Only V8 on (deep-sleep power mode)		20		µA
			V1, V2, and V8 on; V1 and V2 in normal (skip) operating mode		50		
			V1, V2, V5, and V8 on (sleep power mode); V1 and V2 in normal (skip) operating mode		90		
			V1, V2, V3, V4, V5, and V8 on (run power mode); V1, V2, V3, and V4 in normal (skip) operating mode		140		
			V1, V2, V3, V4, V5, V6, V7, and V8 (all on); V1, V2, V3, and V4 in normal (skip) operating mode		250		
		Undervoltage lockout, V_{IN} = 2.2V			1.5		
		Overvoltage lockout, V_{IN} = 6.5V			25		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}			1.9	2.0	2.1	MHz
REG1—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER (MAX8660, MAX8660A only)							
V1 Voltage Accuracy—MAX8860	V1	SET1 = IN, V_{PV1} = 4.2V, load = 600mA		3.250	3.300	3.350	V
		SET1 not connected = V_{PV1} = 3.6V, load = 600mA		2.955	3.000	3.045	
		SET1 = AGND, V_{PV1} = 3.6V, load = 600mA		2.807	2.850	2.893	
V1 Voltage Accuracy—MAX8660A	V1	SET1 = IN, V_{PV1} = 4.2V, load = 600mA		2.463	2.500	2.538	V
		SET1 not connected, V_{PV1} = 3.6V, 600mA		1.970	2.000	2.030	
		SET1 = AGND, 3.6V, load = 600mA		1.773	1.800	1.827	
V1 Load Regulation		Load = 0 to 1200mA			-1.5		%/A
V1 Line Regulation					0.15		%/V
SET1 Input Leakage Current					0.01		µA
V1 Dropout Voltage		Load = 800mA (Notes 3, 4)			150		mV
		Load = 1200mA (Notes 3, 4)			200		
p-Channel On-Resistance					0.12		Ω
n-Channel On-Resistance					0.15		Ω
p-Channel Current-Limit Threshold				1.5	1.8	2.2	A
n-Channel Zero-Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-975		mA
REG1 Maximum Output Current	I_{OUT1}	2.6V ≤ V_{PV1} ≤ 6V (Note 5)		1.2			A
V1 Bias Current					5		µA
LX1 Leakage Current		V_{PV1} = 6V, LX1 = PG1 or PV1, V_{EN1} = 0V	T_A = +25°C	-2	±0.03	+2	µA
			T_A = +85°C		±0.2		
Soft-Start Ramp Rate—MAX8660		To V1 = 3.3V (total ramp time is 450µs for all V1 output voltages)		5	7	9	mV/µs
Soft-Start Ramp Rate—MAX8660A		To V1 = 2.5V (total ramp time is 450µs for all V1 output voltages)		3	5	7	mV/µs
V5 to V1 Enable Time	$t_{VMHVSH1}$	Figure 6			350		µs
Internal Off-Discharge Resistance					650		Ω
Minimum Duty Cycle		Forced-PWM mode only, min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{IN5} = V_{IN67} = V_{IN8}$ = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REG2—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER							
V2 Voltage Accuracy—MAX8660	V2	SET2 = IN, V_{PV2} = 4.2V, load = 600mA		3.250	3.300	3.350	V
		SET2 not connected, V_{PV2} = 3.6V, load = 600mA		2.463	2.500	2.538	
		SET2 = AGND, V_{PV2} = 3.6V, load = 600mA		1.773	1.800	1.827	
V2 Voltage Accuracy—MAX8660A	V2	SET2 = IN, V_{PV2} = 4.2V, load = 600mA		2.463	2.500	2.538	V
		SET2 not connected, V_{PV2} = 3.6V, load = 600mA		1.970	2.000	2.030	
		SET2 = AGND, V_{PV2} = 3.6V, load = 600mA		1.773	1.800	1.827	
V2 Load Regulation		Load = 0 to 900mA			-1.7		%/A
V2 Line Regulation					0.15		%/V
SET2 Input Leakage Current					0.01		µA
V2 Dropout Voltage		Load = 900mA (Notes 3, 4)			225		mV
p-Channel On-Resistance					0.18		Ω
n-Channel On-Resistance					0.15		Ω
p-Channel Current-Limit Threshold				1.10	1.30	1.50	A
n-Channel Zero Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-800		mA
REG2 Maximum Output Current	I_{OUT2}	2.6V ≤ V_{PV2} ≤ 6V (Note 5)		0.9			A
V2 Bias Current					5		µA
LX2 Leakage Current		V_{PV2} = 6V, LX2 = PG2 or PV2, V_{EN2} = 0V	T_A = +25°C	-2	±0.03	+2	µA
			T_A = +85°C		0.2		
Soft-Start Ramp Rate		To V2 = 1.8V (total ramp time is 450µs for all V2 output voltages)		2	4	6	mV/µs
V5 to V2 Enable Time	$t_{VMHVSH2}$	Figure 6			350		µs
Internal Off-Discharge Resistance					650		Ω
Minimum Duty Cycle		Forced-PWM mode only; min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%
REG3—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER							
V3 Output Voltage Accuracy	V3	REG3 default output voltage, V_{PV3} = 3.6V, load = 600mA		1.379	1.400	1.421	V
		REG3 serial programmed from 0.9V to 1.8V, load = 600mA (Note 6)		-1.5		+1.5	%
V3 Load Regulation		Load = 0 to 1600mA			-17		mV/A
V3 Line Regulation		(Note 7)			0.05		%/V
p-Channel On-Resistance					0.12		Ω
n-Channel On-Resistance					0.08		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
p-Channel Current-Limit Threshold				1.85	2.15	2.45	A
n-Channel Zero-Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-0.8		A
REG3 Maximum Output Current	I_{OUT3}	2.6V ≤ $V_{PV3\_}$ ≤ 6V (Note 5)		1.6			A
V3 Bias Current					0.01		µA
LX3 Leakage Current		V_{PV3} = 6V, LX3 = PG3 or PV3, V_{EN34} = 0V	T_A = +25°C	-2	+0.03	+2	µA
			T_A = +85°C		0.24		
Soft-Start Ramp Rate		R_{RAMP} = 56kΩ to 1.4V			8		mV/µs
V3 Dynamic-Change Ramp Rate		R_{RAMP} = 56kΩ			10		mV/µs
EN34 to V3 Enable Time	$t_{PHLVTH3}$	Powering up to 1.4V, Figure 6, R_{RAMP} = 56kΩ			400		µs
Internal Off-Discharge Resistance					550		Ω
Minimum Duty Cycle		Forced-PWM mode only, min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%
REG4—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER							
V4 Output Voltage Accuracy	V4	REG4 default output voltage, V_{PV3} = 3.6V, load = 200mA		1.379	1.400	1.421	V
		REG4 serial programmed from 0.9V to 1.8V, load = 200mA (Note 6)		-1.5		+1.5	%
V4 Load Regulation		Load = 0 to 400mA			-40		mV/A
V4 Line Regulation		(Note 7)			0.1		%/V
p-Channel On-Resistance					0.37		Ω
n-Channel On-Resistance					0.3		Ω
p-Channel Current-Limit Threshold				0.05	0.78	0.90	A
n-Channel Zero-Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-975		mA
REG4 Maximum Output Current	I_{OUT4}	2.6V ≤ V_{PV3} ≤ 6V (Note 5)		0.4			A
V4 Bias Current					0.01		µA
LX4 Leakage Current		V_{PV4} = 6V, LX4 = PG4 or PV4, V_{EN34} = 0V	T_A = +25°C	-2	±0.02	+2	µA
			T_A = +85°C		0.12		
Soft-Start Ramp Rate		R_{RAMP} = 56kΩ to 1.4V			8		mV/µs
V4 Dynamic-Change Ramp Rate		R_{RAMP} = 56kΩ			10		mV/µs
EN34 to V4 Enable Time	$t_{PHLVTH4}$	Powering up to 1.4V, Figure 6, R_{RAMP} = 56kΩ			400		µs
Internal Off-Discharge Resistance					550		Ω
Minimum Duty Cycle		Forced-PWM mode only, min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REG5 LDO						
IN5 Input Voltage Range	V_{IN5}		2.35		V_{IN}	V
V5 Output Voltage	V5	REG5 default output voltage, 2.35V ≤ V_{IN5} ≤ 6V, load = 0 to 200mA	1.764	1.800	1.836	V
		REG5 serial programmed from 1.7V to 2.0, 2.35V ≤ V_{IN5} ≤ 6V, load = 0 to 200mA	-2		+2	%
V5 Output Current Limit	I_{OUT5}		225	350	500	mA
V5 Output-Voltage Noise		10Hz to 100kHz, I_{OUT5} = 10mA		160		µV_{RMS}
V5 Power-Supply Rejection		V_{IN5} = (V5 + 1V), I_{OUT5} = 10mA, f = 10kHz		40		dB
V5 Soft-Start Ramp Rate		Powering up to 1.8V (total ramp time is 225µs for all V5 output voltages)	5	7	9	mV/µs
EN5 to V5 Enable Time	t_{SEHVMH}	Figure 6		290		µs
V5 Dynamic-Change Ramp Rate		R_{RAMP} = 56kΩ		10		mV/µs
Internal Off-Discharge Resistance				2		kΩ
REG6, REG7 LDOs						
IN67 Input Voltage Range	V_{IN67}		2.35		V_{IN}	V
REG6 and REG7 Output Voltage (POR Default to 0V, Set by Serial Input)	V6 V7	Setting from 1.8V to 3.3V in 0.1V steps, load = 0 to 300mA	-3		+3	%
V6, V7 Dropout Voltage		3V mode, load = 300mA (Note 3)		55	100	mV
V6, V7 Output Current Limit	I_{OUT6} I_{OUT7}	V_{IN67} = 3.6V		750		mA
V6, V7 Soft-Start Ramp Rate		Powering up to 3.3V, (total ramp time is 450µs for all V6/V7 output voltages)	5	7	9	mV/µs
Internal Off-Discharge Resistance				350		Ω
REG8 ALWAYS-ON LDO						
V8 Output Voltage	V8	Load = 0 to 15mA	3.168	3.300	3.432	V
		Load = 30mA	2.800	3.2	3.432	
V8 Dropout Voltage		Load = 15mA (Note 3)		180		mV
V8 Output Current Limit	I_{OUT8}	V8 = 2.5V	30	70	135	mA
Internal Off-Discharge Resistance				1.5		kΩ
LOW-BATTERY DETECTOR (LBF, LBR, $\overline{LBO}$)						
Low-Battery Falling Threshold	V_{LBFTH}		1.182	1.200	1.218	V
Low-Battery Rising Threshold	V_{LBRTH}		1.231	1.250	1.268	V
$\overline{LBO}$, $\overline{RSO}$ Output-High Leakage Current		V_{IN} = 6V, T_A = +25°C			0.2	µA
$\overline{LBO}$ Output Low Level		2.6V ≤ V_{IN} ≤ 6V, sinking 3mA			0.2	V
		V_{IN} = 1V, sinking 100µA			0.4	
Minimum V_{IN} for $\overline{LBO}$ Assertion		$\overline{LBO}$ is forced low when the device is in UVLO	1			V

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{IN5} = V_{IN67} = V_{IN8}$ = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{LBO}$ Deassert Delay	t_{VBHBFH}	Figure 6	0	3		µs
LBF and LBR Input Bias Current		T_A = +25°C	-50	0	+50	nA
		T_A = +85°C		0.5		
RESET ($\overline{MR}$, $\overline{RSO}$)						
$\overline{RSO}$ Threshold	V_{RSOTH}	Voltage on V8, falling, hysteresis is 5% (typ)	2.1	2.2	2.3	V
$\overline{RSO}$ Deassert Delay	$t_{VBHRSTH}$	Figure 6	20	24	28	ms
$\overline{RSO}$ Output-High Leakage Current		V_{IN} = 6V, T_A = +25°C			0.2	µA
$\overline{RSO}$ Output Low Level		2.6V ≤ V_{IN} ≤ 6V, sinking 3mA			0.2	V
		V_{IN} = 1V, sinking 100µA			0.4	
Minimum V_{IN} for $\overline{RSO}$ Assertion		$\overline{RSO}$ is forced low when the device is in UVLO	1			V
$\overline{MR}$ Input High Level		2.6V ≤ V_{IN} ≤ 6V	1.4			V
$\overline{MR}$ Input Low Level		2.6V ≤ V_{IN} ≤ 6V			0.4	V
$\overline{MR}$ Input Leakage Current		V_{IN} = 6V, T_A = +25°C	-0.2		+0.2	µA
$\overline{MR}$ Minimum Pulse Width	t_{MR}			1		µs
THERMAL-OVERLOAD PROTECTION						
Thermal-Shutdown Temperature		T_J rising		+160		°C
Thermal-Shutdown Hysteresis				15		°C
ENABLE INPUTS (EN1, EN2, EN34, EN5)						
EN_ Input High Level		2.6V ≤ V_{IN} ≤ 6V	1.4			V
EN_ Input Low Level		2.6V ≤ V_{IN} ≤ 6V			0.4	V
EN_ Input Leakage Current		V_{IN} = 6V, T_A = +25°C	-0.2		+0.2	µA
I^2C LOGIC (SDA, SCL, SRAD)						
SCL, SDA Input High Voltage			1.4			V
SCL, SDA Input Low Voltage					0.4	V
SCL, SDA Input Hysteresis				0.1		V
SCL, SDA Input Current		T_A = +25°C, IN = AGND, V_{IN} = 6V	-10		+10	µA
SDA Output Low Voltage		2.6V ≤ V_{IN} ≤ 6V, sinking 3mA			0.2	V
SRAD Input High Level		2.6V ≤ V_{IN} ≤ 6V	1.4			V
SRAD Input Low Level		2.6V ≤ V_{IN} ≤ 6V			0.4	V
SRAD Input Leakage Current		V_{IN} = 6V, T_A = +25°C	-0.2		+0.2	µA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{IN5} = V_{IN67} = V_{IN8}$ = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING						
Clock Frequency	f_{SCL}				400	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	Figure 8	0.6			µs
CLK Low Period	t_{LOW}		1.3			µs
CLK High Period	t_{HIGH}		0.6			µs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	Figure 8	0.6			µs
DATA Hold Time	$t_{HD;DAT}$	Figure 9	0			µs
DATA Set-Up Time	$t_{SU;DAT}$	Figure 9	100			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	Figure 8	0.6			µs
Bus-Free Time Between STOP and START	t_{BUF}		1.3			µs
Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA and CLK Signals				50		ns

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 3: The dropout voltage is defined as $V_{IN} - V_{OUT}$ when V_{OUT} is 100mV below the nominal value of V_{OUT}.

Note 4: Dropout voltage (V_{DO}) is a function of the p-channel switch resistance (R_{PCH}) and the inductor resistance (R_L). The given values assume R_L = 50mΩ for the REG1 inductor and 67mΩ for the REG2 inductor:

$$V_{DO} = I_{LOAD}\,(R_P + R_L)$$

Note 5: The maximum output current ($I_{OUT(MAX)}$) is:

$$I_{OUT(MAX)} = \frac{I_{LIM} - \dfrac{V_{OUT}(1-D)}{2 \times f \times L}}{1 + (R_N + R_L)\dfrac{(1-D)}{2 \times f \times L}}$$

where:

R_N = n-channel synchronous rectifier RDS (on)
R_P = p-channel power switch RDS (on)
R_L = external inductor ESR
$I_{OUT(MAX)}$ = maximum output current provided by the PMIC
$I_{OUT(TARGET)}$ = maximum desired output current
f = operating frequency minimum
L = external inductor value

Note 6: Tested at 1.4V, default output voltage.

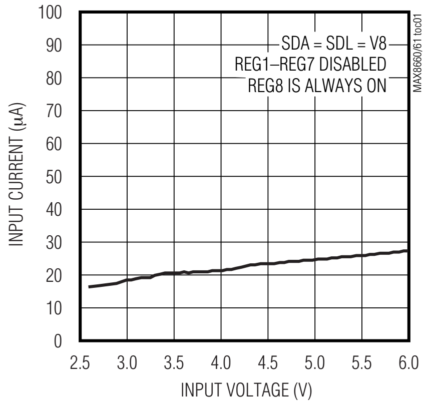
Note 7: All output voltages are possible in normal mode. In forced-PWM mode, the minimum output voltage is limited by 0.167 x V_{IN}. For example, with V_{IN} = 5.688V, the minimum output is 0.95V.

High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

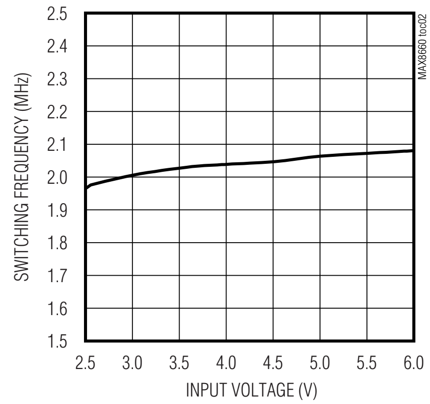
Typical Operating Characteristics

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

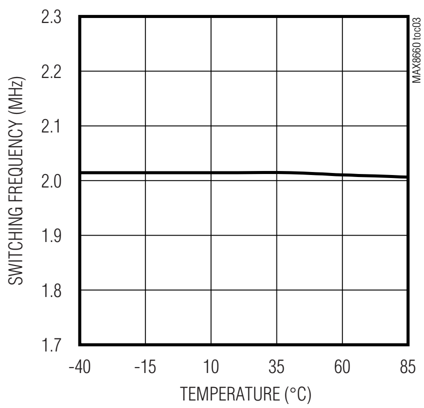
QUIESCENT CURRENT vs. INPUT VOLTAGE



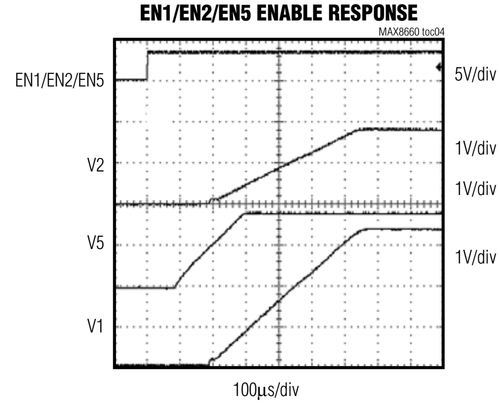
SWITCHING FREQUENCY vs. INPUT VOLTAGE



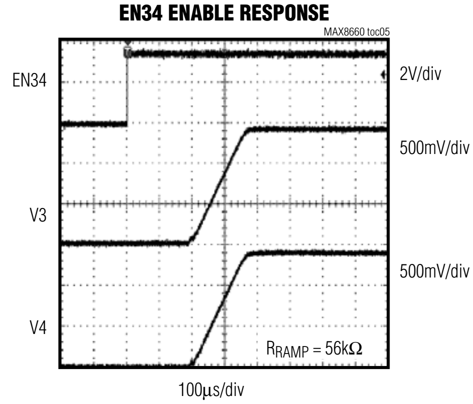
SWITCHING FREQUENCY vs. TEMPERATURE



EN1/EN2/EN5 ENABLE RESPONSE



EN34 ENABLE RESPONSE

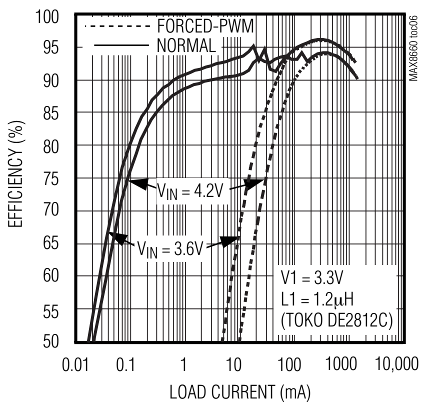


High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

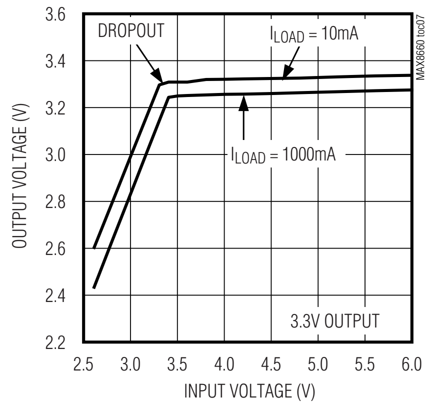
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

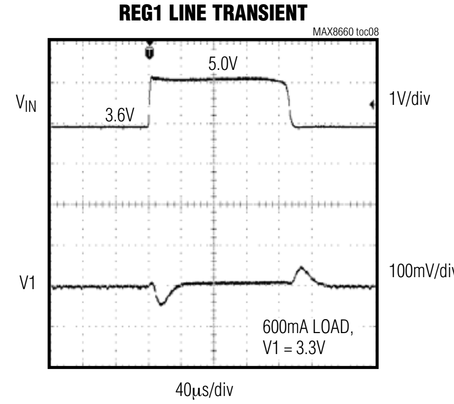
REG1 EFFICIENCY vs. LOAD CURRENT



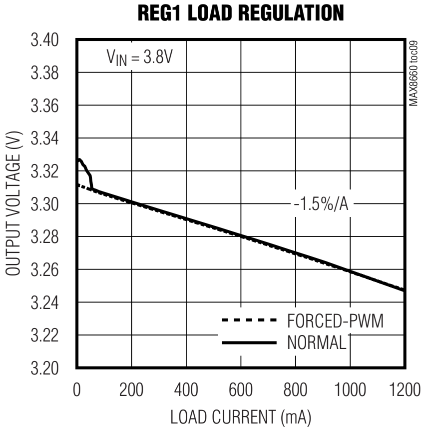
REG1 OUTPUT VOLTAGE vs. INPUT VOLTAGE



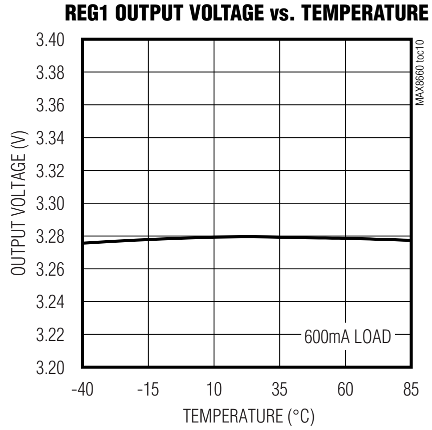
REG1 LINE TRANSIENT



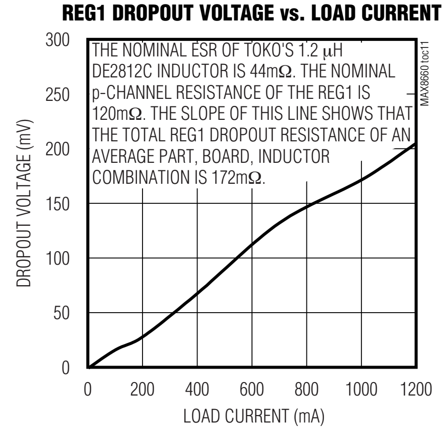
REG1 LOAD REGULATION



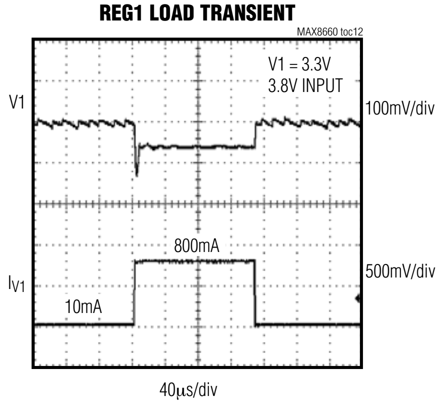
REG1 OUTPUT VOLTAGE vs. TEMPERATURE



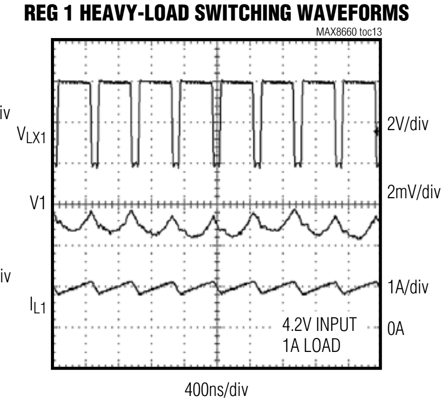
REG1 DROPOUT VOLTAGE vs. LOAD CURRENT



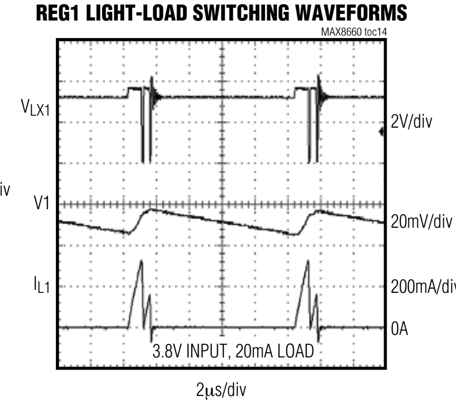
REG1 LOAD TRANSIENT



REG 1 HEAVY-LOAD SWITCHING WAVEFORMS



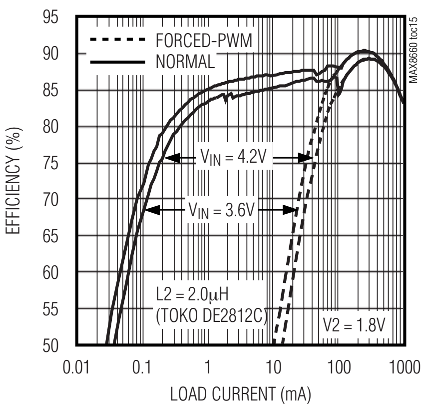
REG1 LIGHT-LOAD SWITCHING WAVEFORMS



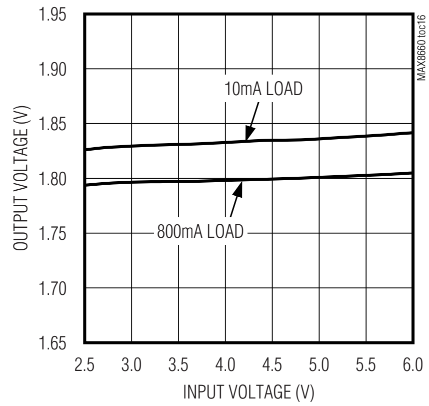
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

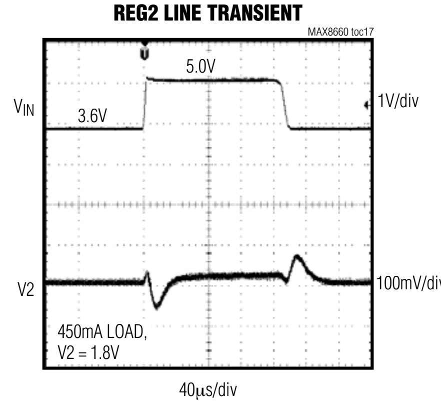
REG2 EFFICIENCY vs. LOAD CURRENT



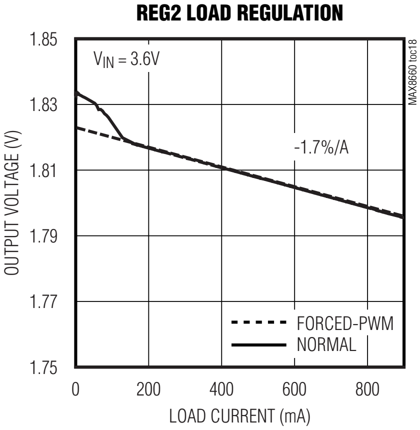
REG2 OUTPUT VOLTAGE vs. INPUT VOLTAGE



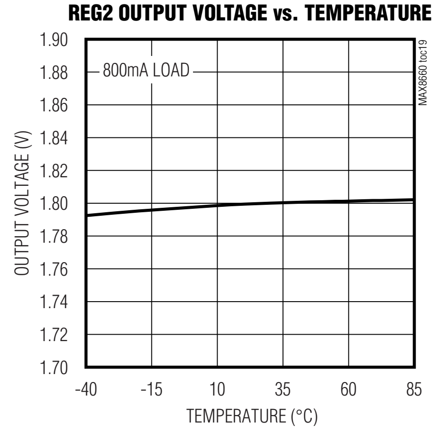
REG2 LINE TRANSIENT



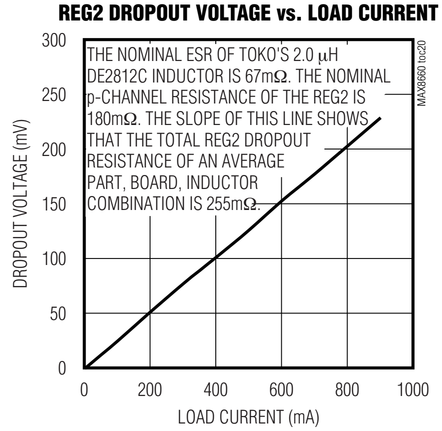
REG2 LOAD REGULATION



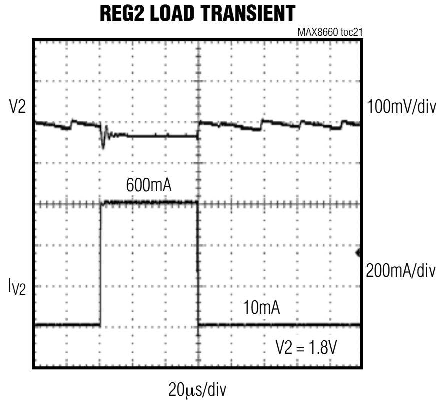
REG2 OUTPUT VOLTAGE vs. TEMPERATURE



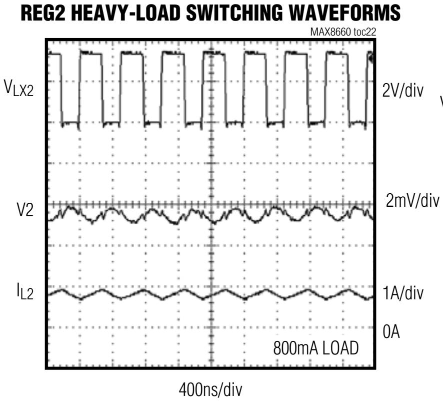
REG2 DROPOUT VOLTAGE vs. LOAD CURRENT



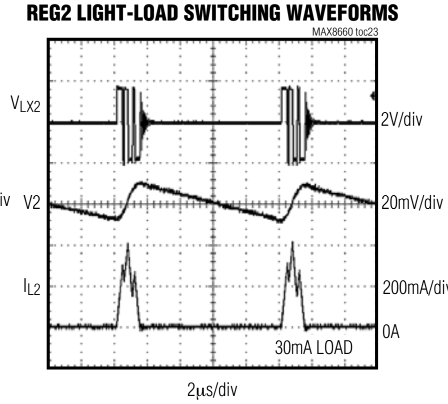
REG2 LOAD TRANSIENT



REG2 HEAVY-LOAD SWITCHING WAVEFORMS



REG2 LIGHT-LOAD SWITCHING WAVEFORMS

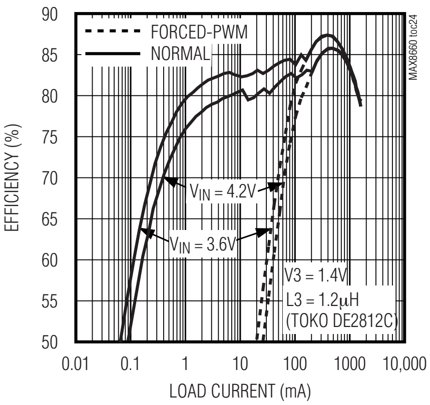


High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications

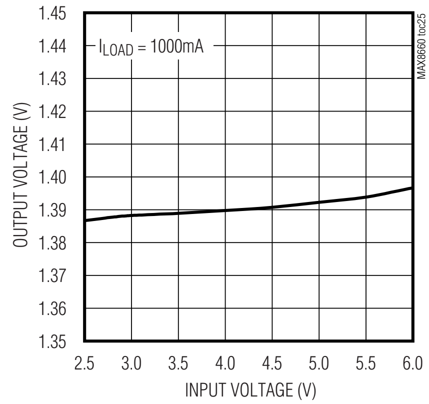
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

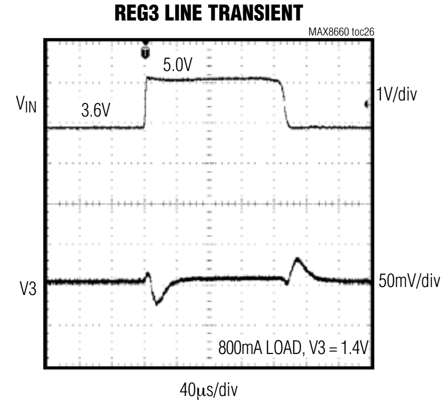
REG3 EFFICIENCY vs. LOAD CURRENT



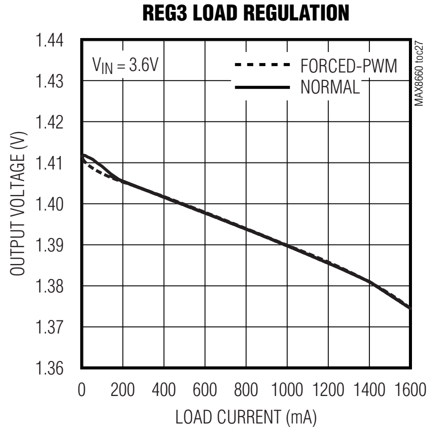
REG3 OUTPUT VOLTAGE vs. INPUT VOLTAGE



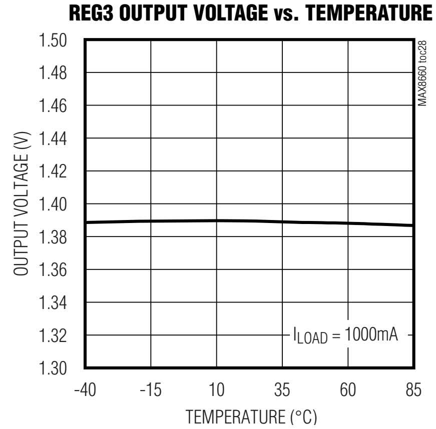
REG3 LINE TRANSIENT



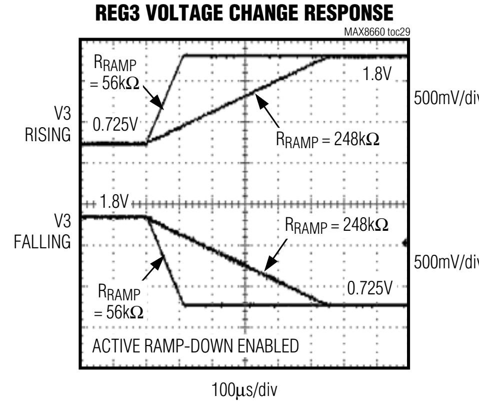
REG3 LOAD REGULATION



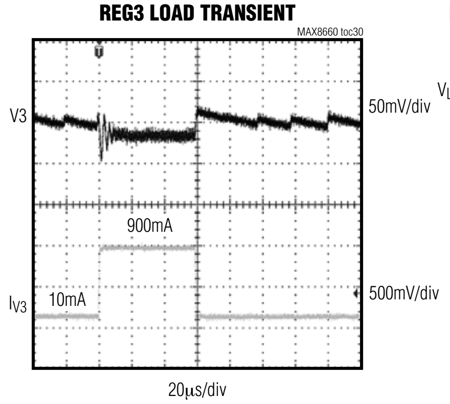
REG3 OUTPUT VOLTAGE vs. TEMPERATURE



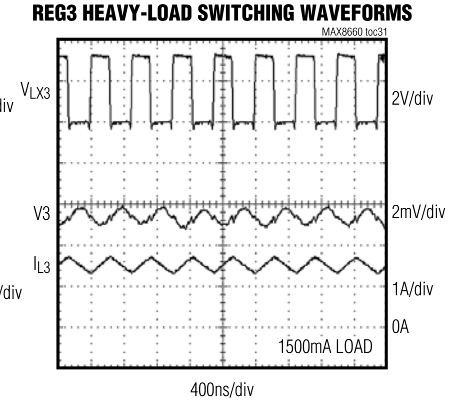
REG3 VOLTAGE CHANGE RESPONSE



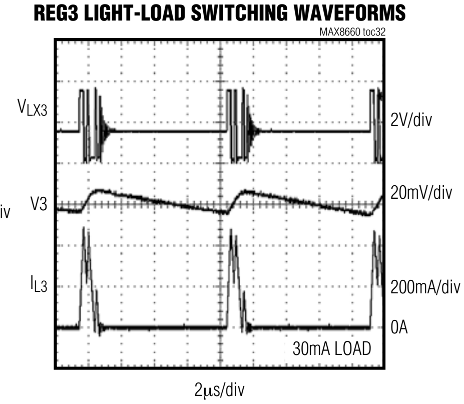
REG3 LOAD TRANSIENT



REG3 HEAVY-LOAD SWITCHING WAVEFORMS



REG3 LIGHT-LOAD SWITCHING WAVEFORMS

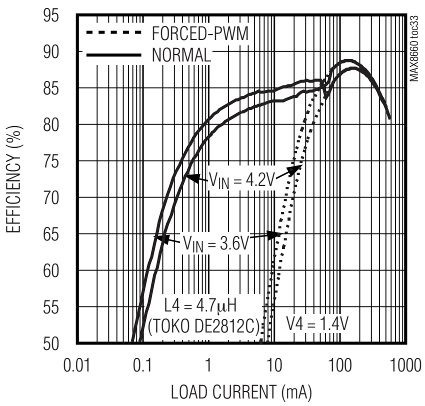


High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications

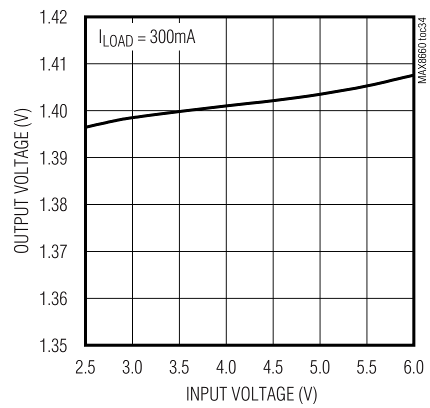
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

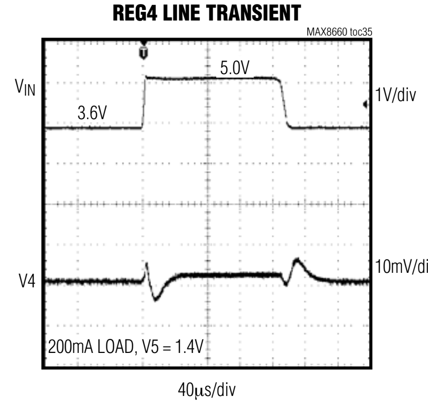
REG4 EFFICIENCY vs. LOAD CURRENT



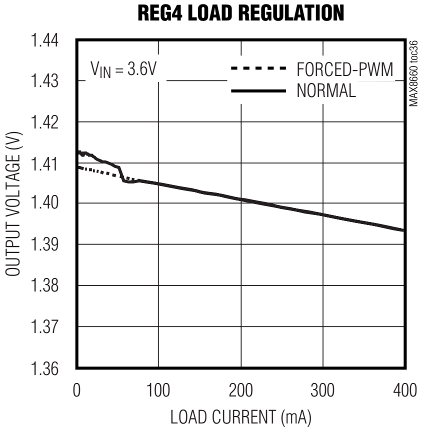
REG4 OUTPUT VOLTAGE vs. INPUT VOLTAGE



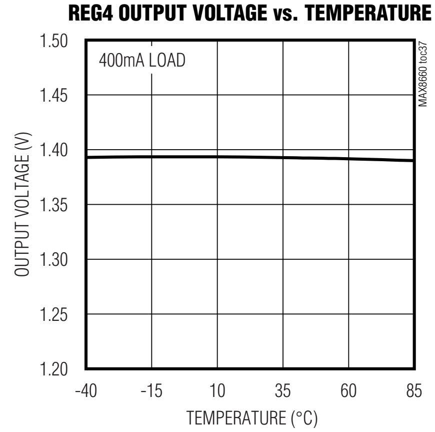
REG4 LINE TRANSIENT



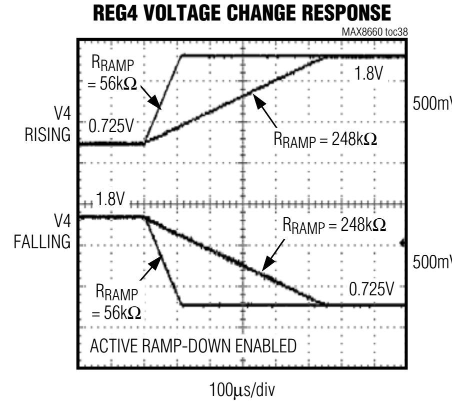
REG4 LOAD REGULATION



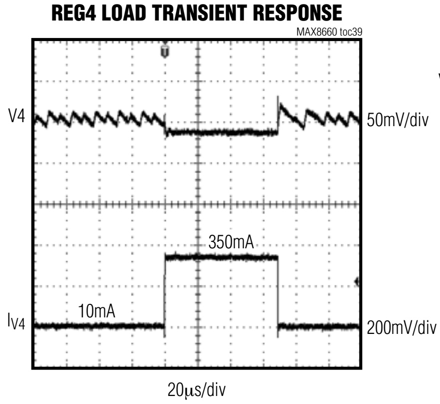
REG4 OUTPUT VOLTAGE vs. TEMPERATURE



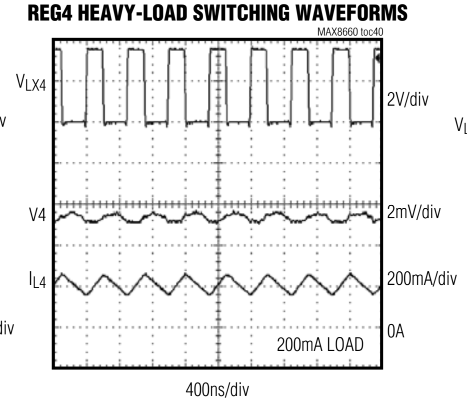
REG4 VOLTAGE CHANGE RESPONSE



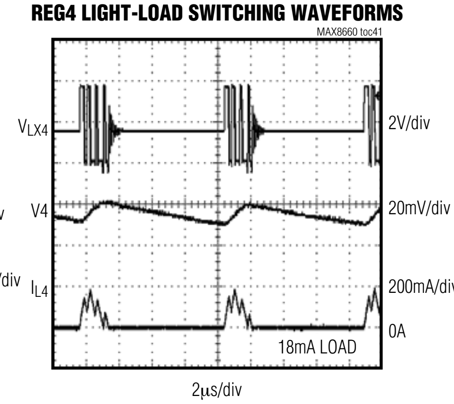
REG4 LOAD TRANSIENT RESPONSE



REG4 HEAVY-LOAD SWITCHING WAVEFORMS



REG4 LIGHT-LOAD SWITCHING WAVEFORMS



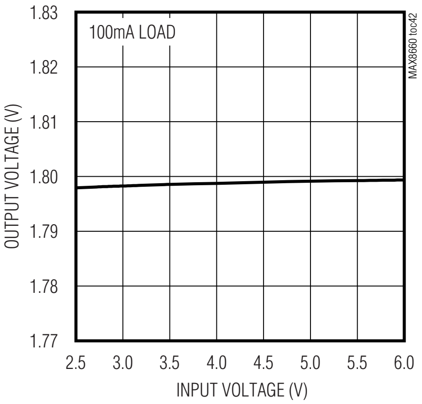
MAX8660/MAX8661

High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

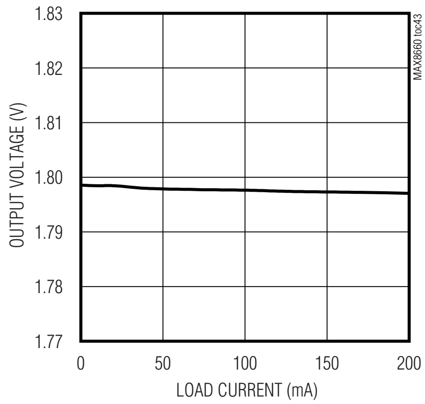
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

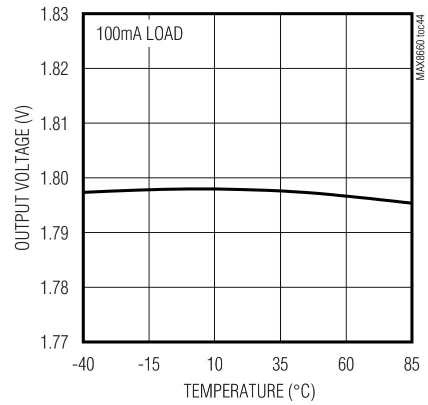
REG5 OUTPUT VOLTAGE vs. INPUT VOLTAGE



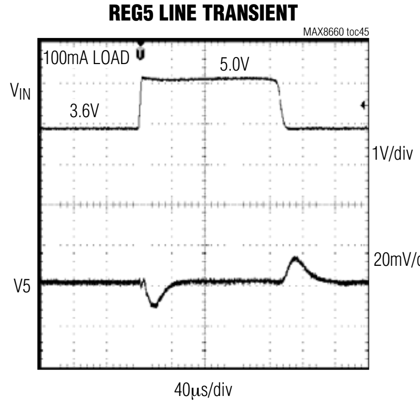
REG5 OUTPUT VOLTAGE vs. LOAD CURRENT



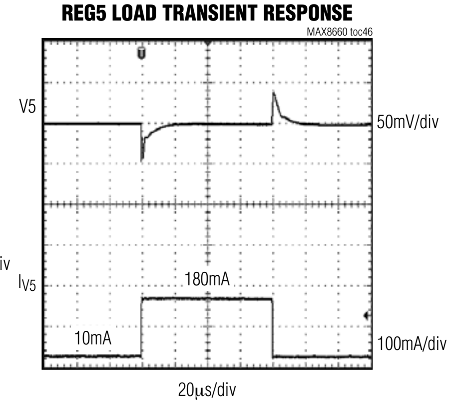
REG5 OUTPUT VOLTAGE vs. TEMPERATURE



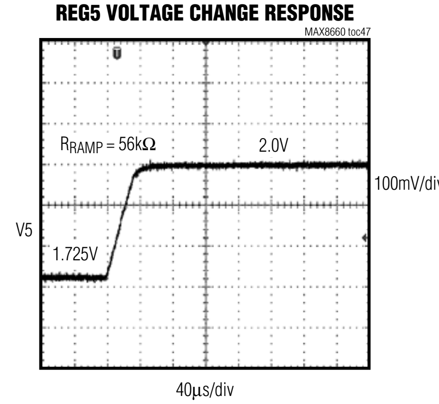
REG5 LINE TRANSIENT



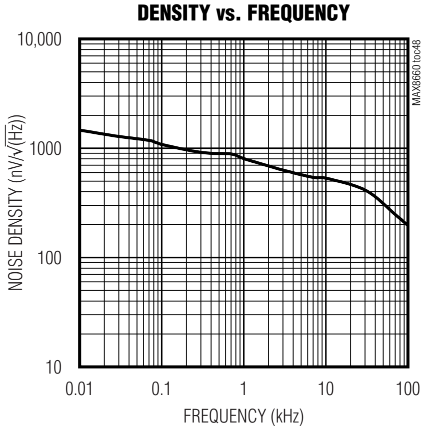
REG5 LOAD TRANSIENT RESPONSE



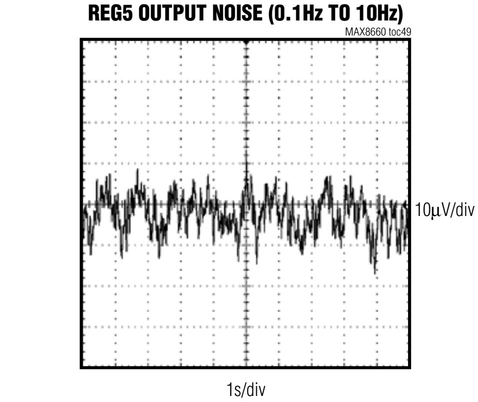
REG5 VOLTAGE CHANGE RESPONSE



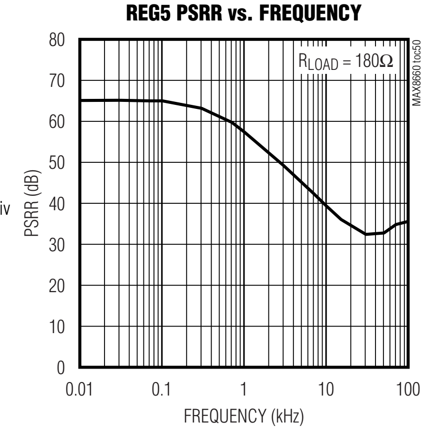
REG5 OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



REG5 OUTPUT NOISE (0.1Hz TO 10Hz)

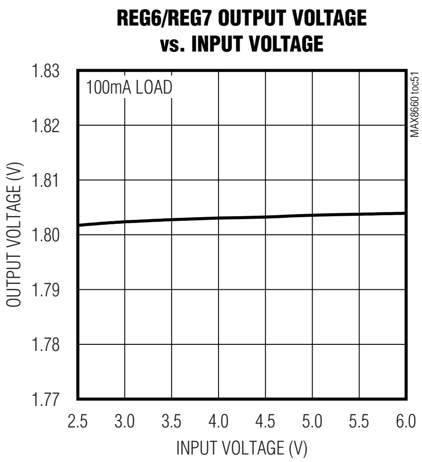


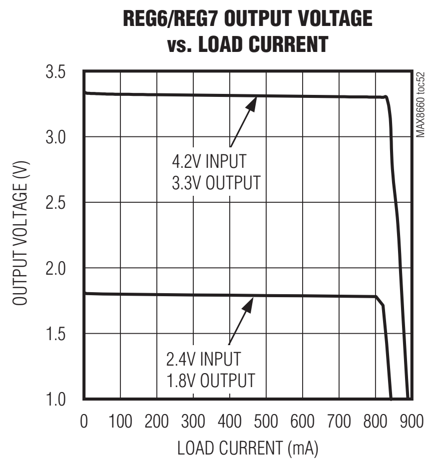
REG5 PSRR vs. FREQUENCY

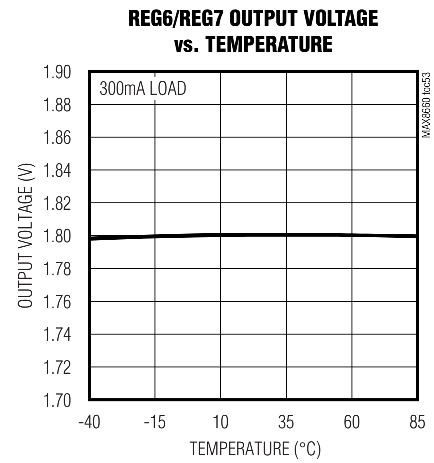


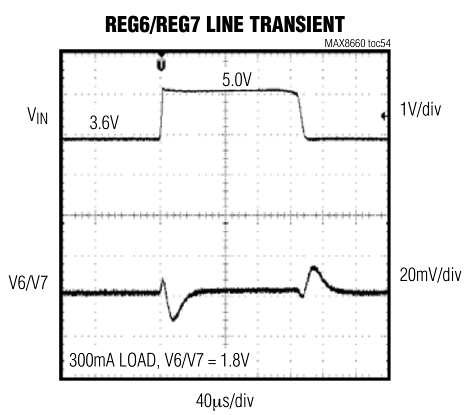
Typical Operating Characteristics (continued)

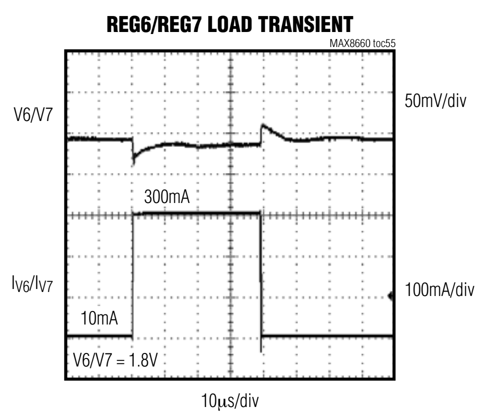
(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

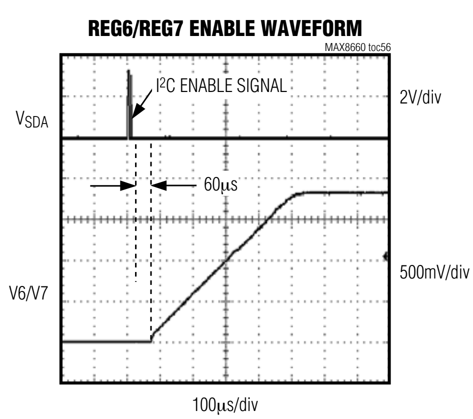


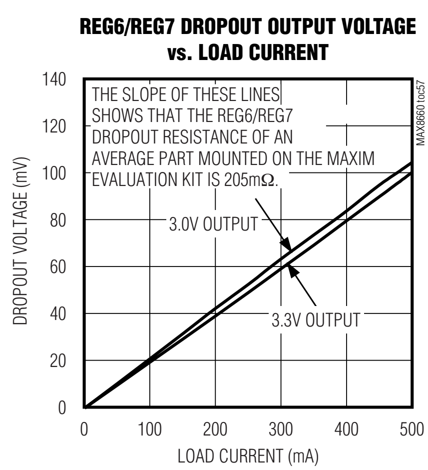








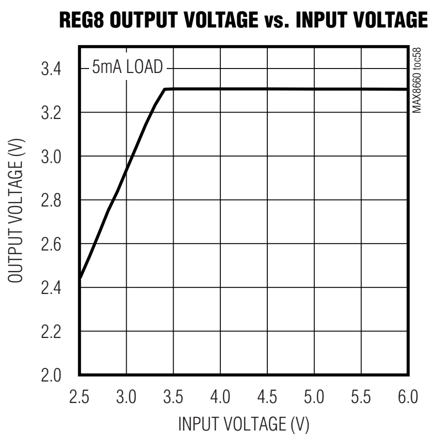


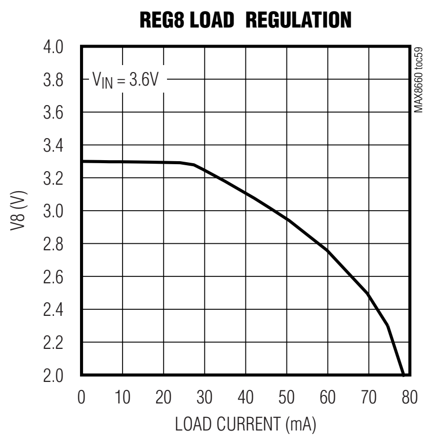


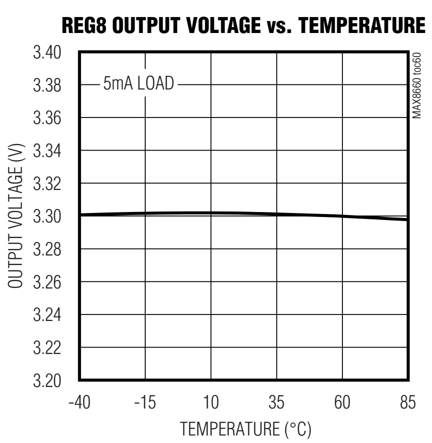
High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

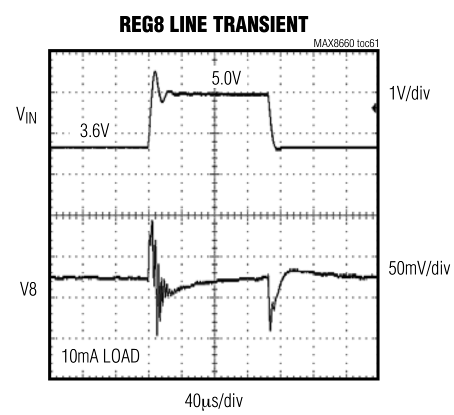
Typical Operating Characteristics (continued)

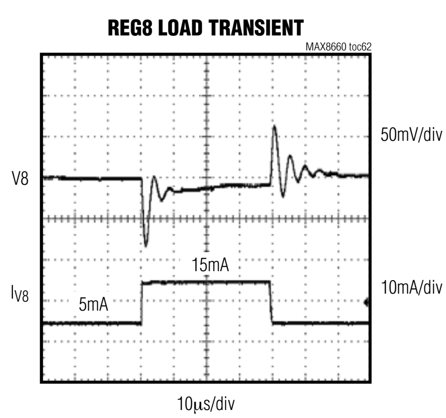
(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

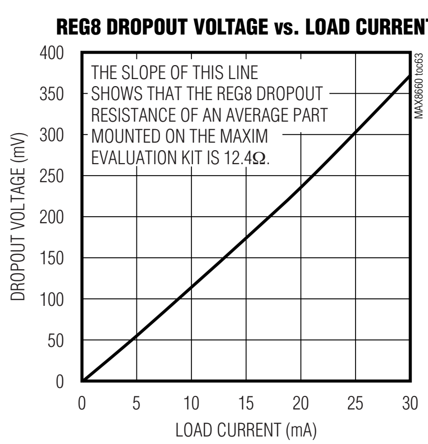












Pin Description

PIN	NAME		FUNCTION
	MAX8660	MAX8661	
1	IN5	IN5	REG5 Power Input. Connect IN5 to IN to ensure V5 rises first to meet Intel sequencing requirements. If adherence to Intel specifications is not required, IN5 can be connected to V1, V2, or another supply between 2.35V and V_{IN}. See the *Linear Regulators (REG5–REG8)* section for more information.
2	V5	V5	REG5 Linear-Regulator Output. V5 defaults to 1.8V and is adjustable from 1.7V to 2.0V through the serial interface. The input to the V5 regulator is IN5. Use V5 to power *VCC_MVT, VCC_BG, VCC_OSC13M,* and *VCC_PLL* on Intel XScale processors. V5 is internally pulled to AGND through 2kΩ when REG5 is shut down.
3	PV4	PV4	REG4 Power Input. Connect a 4.7µF ceramic capacitor from PV4 to PG4. All PV pins and IN must be connected together externally.
4	LX4	LX4	REG4 Switching Node. Connect LX4 to the REG4 inductor. LX4 is high impedance when REG4 is shut down.
5	PG4	PG4	REG4 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
6	SET2	SET2	REG2 Voltage Select Input. SET2 is a tri-level logic input. Connect SET2 to select the V2 output voltage as detailed in Table 4. The REG2 output voltage selected by SET2 is latched at the end of the REG2 soft-start period. Changes to SET2 after the startup period have no effect.
7	V6	V6	REG6 Linear-Regulator Output. REG6 is activated and programmed through the serial interface to output from 1.8V to 3.3V in 0.1V steps. REG6 is off by default. V6 is internally pulled to AGND through 350Ω when REG6 is shut down. V6 optionally powers *VCC_CARD1* on Intel XScale processors.
8	IN67	—	REG6 and REG7 Power Input. IN67 is typically connected to IN. IN67 can also be connected to any supply between 2.35V to V_{IN}.
	—	IN6	REG6 Power Input. IN6 is typically connected to IN. IN6 can also be connected to any supply between 2.35V to V_{IN}.
9	V7	—	REG7 Linear-Regulator Output. REG7 is activated and programmed through the serial interface to output from 1.8V to 3.3V in 0.1V steps. REG7 is off by default. V7 is internally pulled to AGND through 350Ω when REG7 is shut down. V7 optionally powers *VCC_CARD2* on Intel XScale processors.
	—	N.C.	No Internal Connection
10	V2	V2	REG2 Voltage Sense Input. Connect V2 directly to the REG2 output voltage. The output voltage of REG2 is selected by SET2. V2 is internally pulled to AGND through 650Ω when REG2 is shut down. V2 powers *VCC_MEM* on Intel XScale processors.
11	SCL	SCL	Serial-Clock Input. See the *I²C Interface* section.
12	SDA	SDA	Serial-Data Input. See the *I²C Interface* section.
13	$\overline{LBO}$	$\overline{LBO}$	Low-Battery Output. $\overline{LBO}$ is an open-drain output that pulls low when LBF is below its threshold. $\overline{LBO}$ typically connects to the *nBATT_FAULT* input of the Intel XScale processor to indicate that the battery has been removed or discharged.
14	PV2	PV2	REG2 Power Input. Connect a 4.7µF ceramic capacitor from PV2 to PG2. All PV pins and IN must be connected together externally.
15	LX2	LX2	REG2 Switching Node. Connect LX2 to the REG2 inductor. LX2 is high impedance when REG2 is shut down.
16	PG2	PG2	REG2 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
17	IN8	IN8	REG8 Input Power Connection. IN8 must be connected to IN.
18	IN	IN	Main Battery Input. This input provides power to the IC. Connect a 0.47µF ceramic capacitor from IN to AGND.

High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications

Pin Description (continued)

PIN	NAME		FUNCTION
	MAX8660	MAX8661	
19	AGND	AGND	Analog Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
20	V8	V8	REG8 Always-On 3.3V LDO Output. REG8 is the first regulator that powers up in the MAX8660/MAX8661. REG8 is supplied from IN and supplies up to 30mA. V8 is internally pulled to AGND through 1.5kΩ during IN undervoltage or overvoltage lockout. Connect V8 to *VCC_BBATT* on Intel XScale processors.
21	LBF	LBF	Low-Battery Detect Falling Input. The LBF threshold is 1.20V. Connect LBF to LBR for 50mV hysteresis. Use a three-resistor voltage-divider for larger hysteresis. LBF sets the falling voltage at which $\overline{\text{LBO}}$ goes low. See the *Low-Battery Detector ($\overline{\text{LBO}}$, LBF, LBR)* section for more information.
22	LBR	LBR	Low-Battery Detect Rising Input. The LBR threshold is 1.25V. Connect LBF to LBR for 50mV hysteresis. Use a three-resistor voltage-divider for larger hysteresis. LBR sets the rising voltage at which $\overline{\text{LBO}}$ goes high. See the *Low-Battery Detector ($\overline{\text{LBO}}$, LBF, LBR)* section for more information.
23	$\overline{\text{MR}}$	$\overline{\text{MR}}$	Manual Reset Input. A low $\overline{\text{MR}}$ input causes $\overline{\text{RSO}}$ to go low and resets all serial programmed registers to their default values. See the *Reset Output ($\overline{\text{RSO}}$) and $\overline{\text{MR}}$ Input* section for more information.
24	RAMP	RAMP	Ramp-Rate Input. Connect a resistor from RAMP to AGND to set the regulator ramp rates. See the *Ramp-Rate Control (RAMP)* section for more information.
25	EN5	EN5	REG5 Enable Input. Drive EN5 high to turn on REG5. EN5 has hysteresis so an RC can be used to implement manual sequencing with respect to other inputs. EN5 is typically driven by the *SYS_EN* output of an Intel XScale processor.
26	PG3	PG3	REG3 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
27	LX3	LX3	REG3 Switching Node. Connect LX3 to the REG3 inductor. LX3 is high impedance when REG3 is shut down.
28	PV3	PV3	REG3 Power Input. Connect a 4.7μF ceramic capacitor from PV3 to PG3. All PV pins and IN must be connected together externally.
29	$\overline{\text{RSO}}$	$\overline{\text{RSO}}$	Open-Drain Reset Output. $\overline{\text{RSO}}$ typically connects to the nRESET input on an Intel XScale processor. An output low from the MAX8660/MAX8661 $\overline{\text{RSO}}$ resets all serial programmed registers to their default values and causes the processor to enter its reset state. See the *Reset Output ($\overline{\text{RSO}}$) and $\overline{\text{MR}}$ Input* section for more information.
30	V3	V3	REG3 Voltage Sense Input. Connect V3 directly to the REG3 output voltage. The output voltage defaults to 1.4V and is adjustable from 0.725V to 1.8V through the serial interface. V3 is internally pulled to AGND through 550Ω when REG3 is shut down. V3 connects to *VCC_APPS* on Intel XScale processors.
31	EN34	EN34	REG3 and REG4 Active-High Hardware Enable Input. Drive EN34 high to enable both REG3 and REG4. Drive EN34 low to allow the serial interface to enable REG3 and REG4 independently. EN34 has hysteresis so an RC can be used to implement manual sequencing with respect to other inputs. EN34 is typically driven by the *PWR_EN* output of an Intel XScale processor. See the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information.
32	EN2	EN2	REG2 Enable Input. Drive EN2 high to turn on REG2. EN2 has hysteresis so that an RC can be used to implement manual sequencing with respect to other inputs. EN2 is typically driven by the *SYS_EN* output of an Intel XScale processor.
33	SRAD	SRAD	Serial-Address Input. Connect SRAD to AGND for a 7-bit slave address of 0110 100 (0x68). Connect SRAD to IN to change the address to 0110 101 (0x6A). The eighth slave address bit is always zero since the MAX8660/MAX8661 are write-only. See the *Slave Address* section for more information.
34	PG1	—	REG1 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
	—	GND	Ground. Connect all GND pins to EP.

Pin Description (continued)

PIN	NAME		FUNCTION
	MAX8660	MAX8661	
35	LX1	—	REG1 Switching Node. Connect LX1 to the REG1 inductor. LX1 is high impedance when REG1 is shutdown.
	—	N.C.	No Internal Connection
36	PV1	—	REG1 Power Input. Connect a 4.7µF ceramic capacitor from PV1 to PG1. All PV pins and IN must be connected together externally.
	—	PV	Power Input. All PV pins and IN must be connected together externally.
37	EN1	—	REG1 Enable Input. Drive EN1 high to turn on REG1. EN1 has hysteresis so that an RC can be used to implement manual sequencing with respect to other inputs. EN1 is typically driven by the *SYS_EN* output of an Intel XScale processor.
	—	GND	Ground. Connect all GND pins to EP.
38	V1	—	REG1 Voltage Sense Input. Connect V1 directly to the REG1 output voltage. The output voltage of REG1 is selected by SET1. Connect V1 to *VCC_IOx* for Intel XScale processors. V1 is internally pulled to AGND through 650Ω when REG1 is shut down.
	—	GND	Ground. Connect all GND pins to EP.
39	SET1	—	REG1 Voltage Select Input. SET1 is a tri-level logic input. Connect SET1 to select the V1 output voltage as detailed in Table 3. The REG1 output voltage selected by SET1 is latched at the end of the REG1 soft-start period. Changes to SET1 after the startup period have no effect.
	—	GND	Ground. Connect all GND pins to EP.
40	V4	V4	REG4 Feedback Sense Input. Connect V4 directly to the REG4 output voltage. The REG4 output voltage defaults to 1.4V and is adjustable from 0.725V to 1.8V with the serial interface. V4 is internally pulled to AGND through 550Ω when REG4 is shut down. V4 powers *VCC_SRAM* on Intel XScale processors.
EP	EP	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PG1, PG2, PG3, PG4, and AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX8660/MAX8661 PMICs are optimized for devices using the next-generation Intel XScale processors, including smart cellular phones, PDAs, Internet appliances, and other portable devices requiring substantial computing and multimedia capability and low power consumption. The MAX8660/MAX8661 comply with Intel XScale processor specifications.

As shown in Figure 2, the MAX8660 integrates eight high-performance, low-operating-current power supplies. REG1–REG4 are step-down DC-DC converters, and REG5–REG8 are linear regulators. Other functions include low-battery detection ($\overline{LBO}$), a reset output ($\overline{RSO}$), a manual reset input ($\overline{MR}$), and a 2-wire I^2C serial interface. The MAX8661 functions the same as the MAX8660, but does not have the REG1 step-down regulator and the REG7 linear regulator.

The operating input voltage range is from 2.6V to 6.0V, allowing use with a 1-cell Li+ battery, 3-cell NiMH, or a 5V input. Input protection is provided with undervoltage and overvoltage lockouts. Overvoltage lockout protects the device against inputs up to 7.5V.

Maxim vs. Intel Terminology

The MAX8660/MAX8661 are compatible with Intel's next-generation XScale processor. Figure 1 shows one of many possible connections between the Intel XScale processor and the MAX8660/MAX8661. To facilitate system development with Intel processors, this document uses both Maxim and Intel terminology. Intel terminology appears in parentheses and italics. For example, this document refers to "V8 (*VCC_BBATT)*" because the MAX8660 V8 output powers the Intel *VCC_BBATT* power domain. Tables 1 and 2 outline Maxim and Intel terminology.

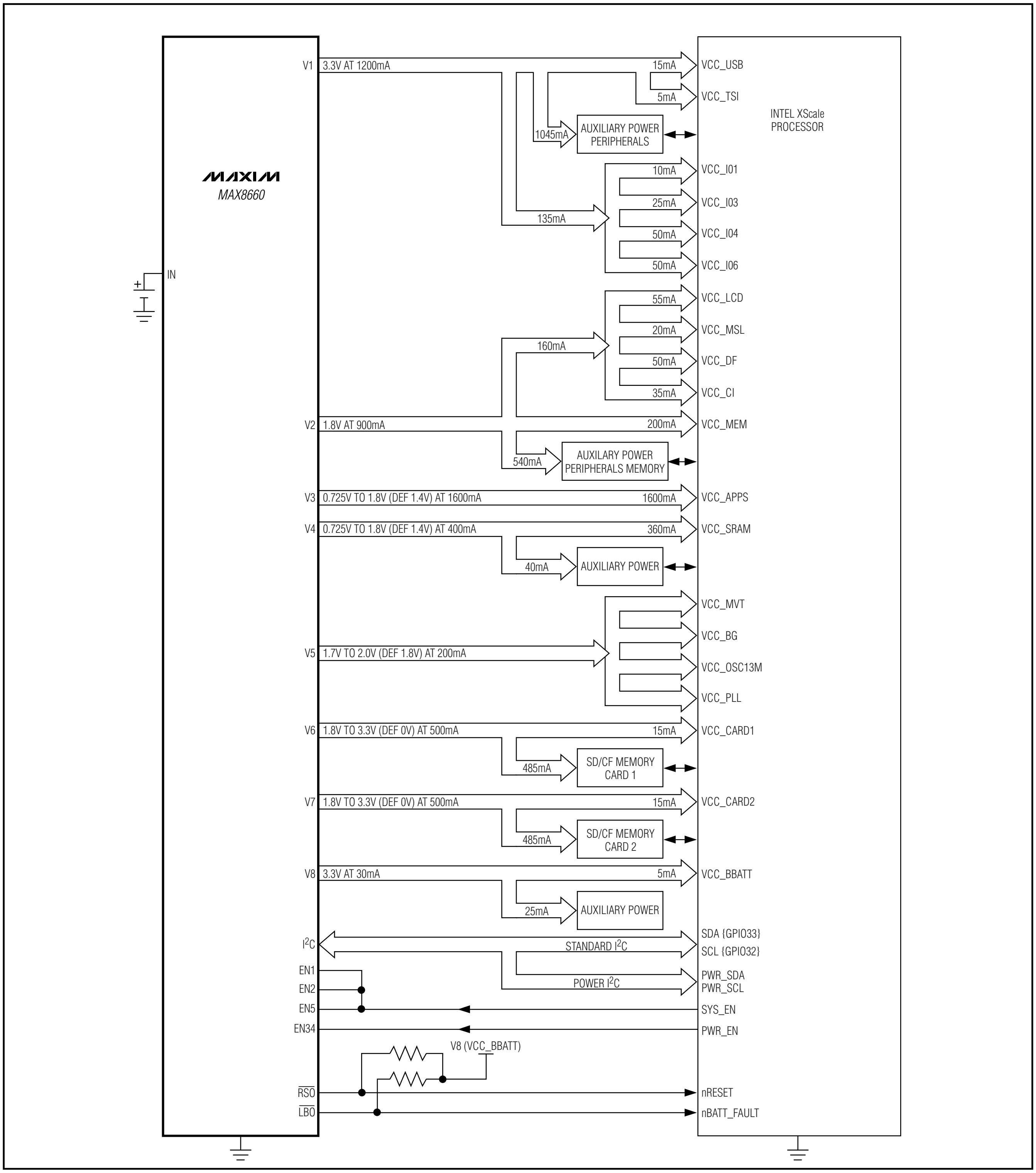


Figure 1. Example MAX8660 Connection to Intel XScale Processor. This is one example only. Other connections are also supported.

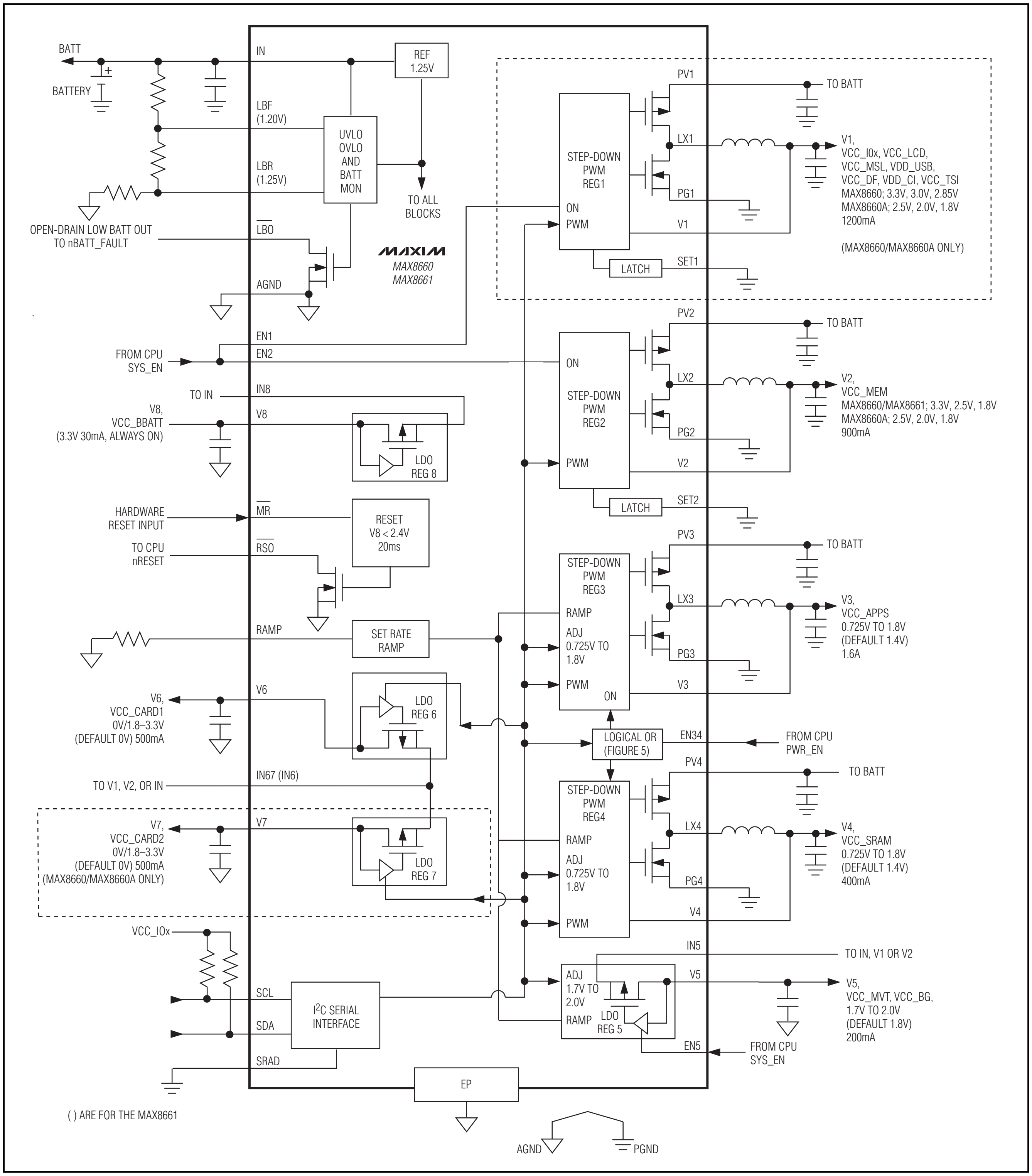


Figure 2. Functional Diagram

High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

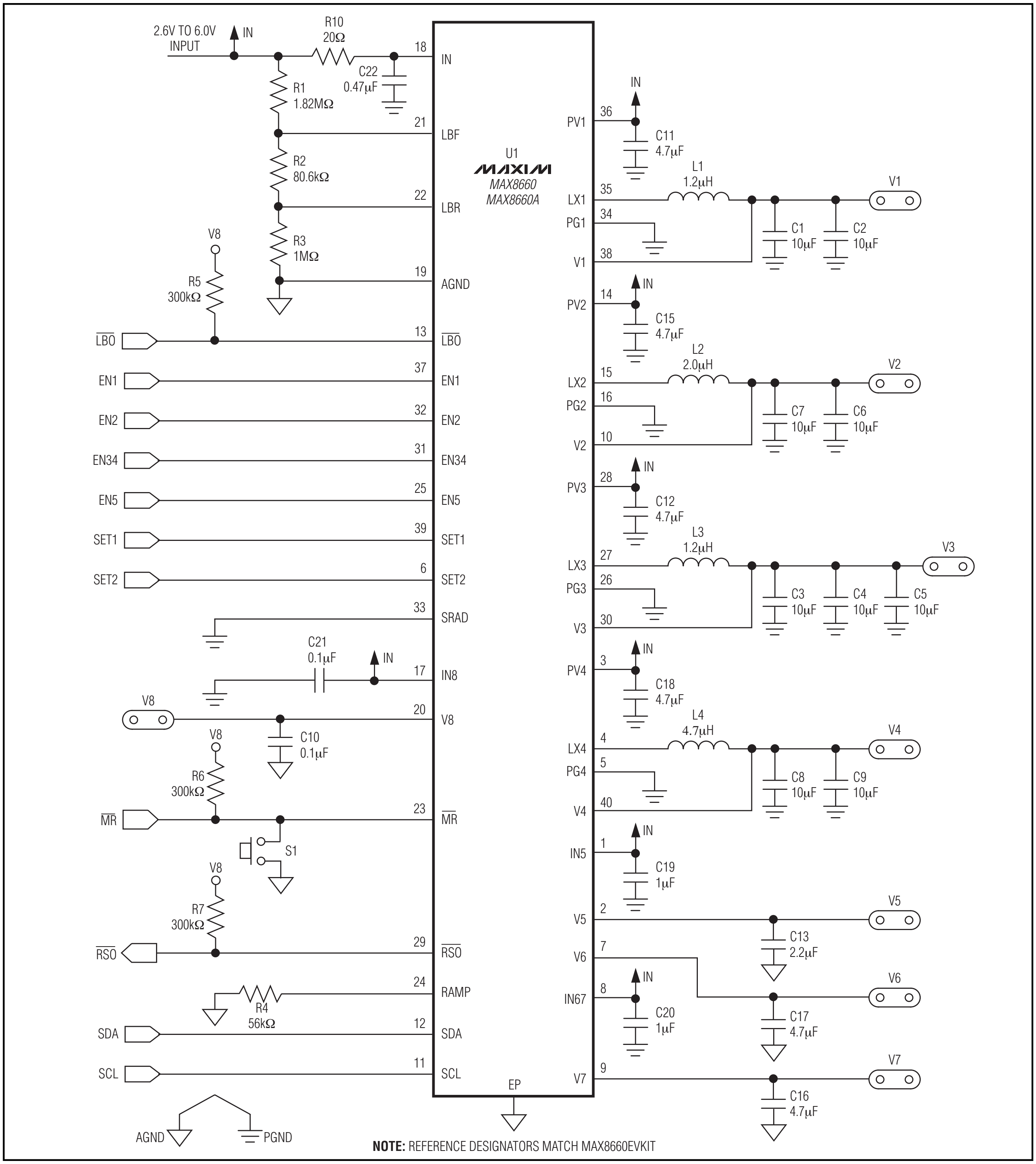


Figure 3. Typical Applications Circuit

Table 1. Maxim and Intel Power Domain Terminology

INTEL POWER DOMAIN	INTEL POWER DOMAIN ACCEPTABLE VOLTAGE	COMPATIBLE MAXIM POWER DOMAIN	DESCRIPTION
VCC_IO1 *VCC_IO3* *VCC_IO4* *VCC_IO6*	1.8V ±10% or 3.0V ±10% or 3.3V ±10%	V1 or V2	• Peripheral I/O supply for UARTs, standard I^2C, power I^2C, audio interface, SSPs, PWMs, etc. (*VCC_IO1,VCC_IO3, VCC_IO4, VCC_IO6*)
VCC_LCD *VCC_MSL* *VCC_CI* *VCC_DF*	1.8V ±10% or 3.0V ±10%	V1 or V2	• LCD interface logic (*VCC_LCD*) • Fast serial interface (*VCC_MSL*) • Camera flash interface (*VCC_CI*) • Data flash interface (*VCC_DF*)
VCC_MEM	1.8V ±100mV	V2	• I/O supply for high-speed memory
VCC_APPS	0.95V to 1.41V ±5%	V3	• Main processor core
VCC_SRAM	1.08V to 1.41V ±100mV	V4	• Internal SRAM memory
VCC_MVT *VCC_BG* *VCC_OSC13M* *VCC_PLL*	1.8V ±100mV	V5	• Internal logic and I/O blocks (*VCC_MVT*) • Bandgap reference (*VCC_BG*) • 13MHz oscillator (VCC_OSC13M) • Phase-locked loop (PLL) and oscillator (*VCC_PLL*)
VCC_CARD1	1.8V ±10% or 3.0V ±10% or 3.3V ±10%	V6	• Removable storage and USIM card supply
VCC_CARD2	1.8V ±10% or 3.0V ±10% or 3.3V ±10%	V7	• Removable storage and USIM card supply
VCC_BBATT	3.0V ±1V	V8	• Regulated battery voltage
VCC_USB	3.3V ±300mV	V1 or V2 (if programmed to 3.3V)	• Universal serial bus (*VCC_USB*)
VCC_TSI	3.3V ±300mV	V1 or V2 (if programmed to 3.3V)	• Touch-screen interface (*VCC_TSI*)

Step-Down DC-DC Converters (REG1–REG4)

REG1 (VCC_IO) Step-Down DC-DC Converter (MAX8660 Only)

REG1 is a high-efficiency (REG1 + REG8 I_Q = 40µA) 2MHz current-mode step-down converter that outputs up to 1200mA with efficiency up to 96% (see *the Typical Operating Characteristics*). The output voltage (V1) is selected with the SET1 input as shown in Table 3. The REG1 output voltage selection is latched at the end of the REG1 soft-start period. Changes in SET1 after the startup period have no effect.

EN1 is a dedicated enable input for REG1. Drive EN1 high to enable REG1 or drive EN1 low to disable REG1.

Table 2. Maxim and Intel Digital Signal Terminology

MAXIM	INTEL	DESCRIPTION
EN34	*PWR_EN*	Active-High Enable Signal for Processor Core Power. The Intel XScale processor drives this *PWR_EN* signal high to exit sleep mode. The processor's PWR_EN logic is powered by the MAX8660/MAX8661 "always on" V8 (*VCC_BBATT*) regulator during sleep mode.
EN1, EN2, EN5	*SYS_EN*	Active-High Enable Signal for Peripheral Power Supplies. The Intel XScale processor drives this SYS_EN signal high to enter run mode.
$\overline{RSO}$	*nRESET*	Active-Low Reset. The MAX8660/MAX8661 drive this signal low to reset the processor. When $\overline{RSO}$ goes low, the MAX8660/MAX8661 I²C registers are reset to their default values.
$\overline{LBO}$	*nBATT_FAULT*	Active-Low Battery Fault. The MAX8660/MAX8661 drive this signal low to signal the processor that the battery has been removed or discharged.
SDA	*GPIO33* *PWR_SDA*	I²C Serial-Data Input/Output. The MAX8660/MAX8861 SDA generally connects to both the XScale processor's standard I²C data line (*GPIO33*) and its dedicated power I²C data line. This connection operates as an I²C multimaster system with the MAX8660/MAX8661 accepting commands from both the standard I²C and the power I²C.
SCL	*GPIO32* *PWR_SCL*	I²C Serial Clock. The MAX8660/MAX8661 SCL generally connects to both the XScale processor's standard I²C clock line (*GPIO32*) and its dedicated power I²C clock line. This connection operates as an I²C multimaster system with the MAX8660/MAX8661 accepting commands from both the standard I²C and the power I²C.

Table 3. SET1 Logic

SET1*	MAX8660: V1 (V)	MAX8660A: V1 (V)
IN	3.3	2.5
UNCONNECTED	3.0	2.0
GROUND	2.85	1.8

**SET1 is latched after REG1 startup.*

Table 4. SET2 Logic

SET2*	MAX8660, MAX8661: V2 (V)	MAX8660A: V2 (V)
IN	3.3	2.5
UNCONNECTED	2.5	2.0
GROUND	1.8	1.8

**SET2 is latched after REG2 startup.*

EN1 has hysteresis so that an RC may be used to implement manual sequencing with respect to other inputs. In systems based on Intel XScale processors, EN1, EN2, and EN5 are typically connected to *SYS_EN* (Table 2).

The REG1 step-down regulator operates in either normal or forced-PWM mode. See the *REG1–REG4 Step-Down DC-DC Converter Operating Modes* section for more information.

REG1 has an on-chip synchronous rectifier. See the *REG1–REG4 Synchronous Rectification* section for more information.

The REG1 regulator allows 100% duty-cycle operation. See the *REG1/REG2 100% Duty-Cycle Operation (Dropout)* section for more information.

REG2 (VCC_IO, VCC_MEM) Step-Down DC-DC Converters

REG2 is a high-efficiency (REG2 + REG8 I_Q = 40µA) 2MHz current-mode step-down DC-DC converter that outputs up to 900mA with efficiency up to 96%. The output voltage is selected with the SET2 input as shown in Table 4. The REG2 output voltage selection is latched at the end of the REG2 soft-start period. Changes in SET2 after the startup period have no effect.

EN2 is a dedicated enable input for REG2. Drive EN2 high to enable REG2 or drive EN2 low to disable REG2. EN2 has hysteresis so that an RC may be used to implement manual sequencing with respect to other inputs. In systems based on Intel processors, EN1, EN2, and EN5 are typically connected to *SYS_EN* (Table 2).

The REG2 step-down regulator operates in either normal or forced-PWM mode. See the *REG1–REG4 Step-Down DC-DC Converter Operating Modes* section for more information.

The REG2 regulator has an on-chip synchronous rectifier. See the *REG1–REG4 Synchronous Rectification* section for more information.

The REG2 regulator allows 100% duty-cycle operation. See the *REG1/REG2 100% Duty-Cycle Operation (Dropout)* section for more information.

REG3 (VCC_APPS) Step-Down DC-DC Converters

REG3 is a high-efficiency (REG3 + REG8 I_Q = 45µA) 2MHz current-mode step-down converter that has an I²C-adjustable output voltage from 0.725V to 1.800V in 25mV increments with efficiency up to 92%. The default REG3 output voltage is 1.4V (contact factory for other default voltages). REG3 delivers up to 1.6A. See the *I²C Interface* section for details on how to adjust the output voltage.

REG3 has an I²C enable bit (EN3) and a shared hardware enable pin (EN34). See the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information.

The REG3 step-down regulator operates in either normal or forced-PWM mode. See the *REG1–REG4 Step-Down DC-DC Converter Operating Modes* section for more information.

The REG3 regulator has an on-chip synchronous rectifier. See the *REG1–REG4 Synchronous Rectification* section for more information.

REG4 (VCC_SRAM) Step-Down DC-DC Converters

REG4 is a high-efficiency (REG4 + REG8 I_Q = 45µA) 2MHz current-mode step-down converter that has an I²C-adjustable output voltage from 0.725V to 1.800V in 25mV increments with efficiency up to 92%. The default REG4 output voltage is 1.4V (contact factory for other default voltages). REG4 delivers up to 400mA. See the *I²C Interface* section for details on how to adjust the output voltage.

REG4 has an I²C enable bit (EN4) and a shared hardware enable pin (EN34). See the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information.

The REG4 step-down regulator operates in either normal or forced-PWM mode. See the *REG1–REG4 Step-Down DC-DC Converter Operating Modes* section for more information.

The REG4 regulator has an on-chip synchronous rectifier. See the *REG1–REG4 Synchronous Rectification* section for more information.

REG1–REG4 Step-Down DC-DC Converter Operating Modes

REG1–REG4 independently operate in one of two modes: normal or forced PWM. At power-up or after a reset, REG1–REG4 default to normal operation. Activate forced-PWM mode by setting bits in the FPWM register (Table 9) with the I²C interface. The FPWM bits can be changed at any time.

In forced-PWM mode, a converter operates with a constant 2MHz switching frequency regardless of output load. The MAX8660/MAX8661 regulate the output voltage by modulating the switching duty cycle. Forced-PWM mode is ideal for low-noise systems because output voltage ripple is small (< 10mV_{PP}) and switching harmonics occur at multiples of the constant-switching frequency and are easily filtered. However, light-load power consumption in forced-PWM mode is higher than that of normal mode (Table 7).

Normal operation offers improved efficiency at light loads by switching only as necessary to supply the load. With moderate to heavy loading, the regulator switches at a fixed 2MHz switching frequency as it does in forced-PWM mode. This transition to fixed-frequency switching occurs at the load current specified in the following equation:

$$I_{OUT} \cong \frac{V_{IN} - V_{OUT}}{2 \times L} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

REG1–REG4 Synchronous Rectification

Internal n-channel synchronous rectifiers eliminate the need for external Schottky diodes and improve efficiency. The synchronous rectifier turns on during the second half of each switching cycle (off-time). During this time, the voltage across the inductor is reversed, and the inductor current ramps down. In PWM mode, the synchronous rectifier turns off at the end of the switching cycle. In normal mode, the synchronous rectifier turns off when the inductor current falls below 25mA or at the end of the switching cycle, whichever occurs first.

REG1/REG2 100% Duty-Cycle Operation (Dropout)

The REG1 and REG2 step-down DC-DC converters operate with 100% duty cycle when the supply voltage approaches the output voltage. This allows these converters to maintain regulation until the input voltage falls below the desired output voltage plus the dropout voltage specification of the converter. During 100% duty-cycle operation, the high-side p-channel MOSFET turns on constantly, connecting the input to the output through the inductor. The dropout voltage (V_{DO}) is calculated as follows:

$$V_{DO} = I_{LOAD} (R_P + R_L)$$

where:

R_P = p-channel power switch $R_{DS(on)}$
R_L = external inductor ESR

The REG1 dropout voltage is 200mV with a 1200mA load (with inductor resistance = 50mΩ). The REG2 dropout voltage is 225mV with a 900mA load (with inductor resistance = 67mΩ).

Linear Regulators (REG5–REG8)

REG5 (VCC_MVT, VCC_BG, VCC_OSC13M, VCC_PLL)

REG5 is a linear regulator with an I²C-adjustable output voltage from 1.700V to 2.000V in 25mV increments (REG5 + REG8 I_Q = 55µA). The default REG5 voltage is 1.8V. REG5 delivers up to 200mA. See the *I²C Interface* section for details on how to adjust the output voltage.

The power input for the REG5 linear regulator is IN5. The IN5 input voltage range extends down to 2.35V. Note that in the Intel XScale specification, *VCC_MVT* is enabled by *SYS_EN* (along with V1 and V2), but must not rise after V1 (*VCC_I/O*) or V2 (*VCC_MEM*). This requirement dictates that IN5 be connected to IN and not V1 or V2.

EN5 is a dedicated enable input for REG5. Drive EN5 high to enable REG5. Drive EN5 low to disable REG5. EN5 has hysteresis so that an RC may be used to implement manual sequencing with respect to other inputs. In systems with Intel XScale processors, EN1, EN2, and EN5 are typically connected to *SYS_EN* (Table 2).

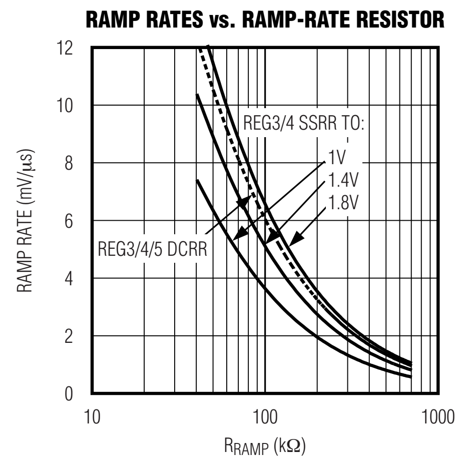
REG6/REG7 (VCC_CARD1, VCC_CARD2)

The REG6/REG7 linear regulators supply up to 500mA each (REG6 or REG 7 + REG8 I_Q = 85µA). The output voltages, V6 and V7, are programmable through the serial interface from 1.8V to 3.3V in 0.1V steps (Table 13). See the *I²C Interface* section for details on changing the V6 or V7 voltage. On the MAX8660, the combined power input for the REG6 and REG7 linear regulators is IN67. On the MAX8661, IN6 is the power input for REG6 (REG7 is not available on the MAX8661).

REG6 and REG7 are disabled by default and must be enabled using the I²C serial interface. REG6 and REG7 have independent enable bits in the OVER2 register: EN6 and EN7 (Table 9). To enable the regulators, set the corresponding enable bit.

REG8 (VCC_BBATT) Always-On Regulator

The output of REG8 (V8) is always active when the input voltage (V_{IN}) is above the undervoltage-lockout threshold of 2.55V (max) and below the overvoltage-lockout threshold of 6.0V (min). The REG8 linear regulator is supplied from IN and its output regulates to 3.3V and supplies up to 30mA. The internal REG8 pass element is 12Ω in dropout, providing a 180mV dropout voltage with a 15mA output current. Connect V8 to *VCC_BBATT* for applications that use Intel XScale processors. The $\overline{RSO}$ output goes low if V8 is less than 2.2V (falling typ).



REG3/REG4 SOFT – START RAMP RATE (SSRR):

$$SSRR\left[\frac{mV}{\mu s}\right] = \frac{1.4 \times V_{OUT}[V]}{0.0014848 \times (2.2 \times (R_{AMP}[k\Omega] + 13.5) + 9)}$$

REG/REG4/REG5 DYNAMIC – CHANGE RAMP RATE (DCRR):

$$DCRR\left[\frac{mV}{\mu s}\right] = \frac{12500}{8 \times (2.2 \times (R_{RAMP}[k\Omega] + 13.5) + 9)}$$

Figure 4. Soft-Start and Voltage-Change Ramp Rates

Ramp-Rate Control (RAMP)

REG1 and REG2 have a fixed soft-start ramp that eliminates input current spikes when they are enabled; 200µs after being enabled, REG1 and REG2 linearly ramp from 0V to the set output voltage in 450µs. When these regulators are disabled, the output voltage decays at a rate determined by the output capacitance, internal 650Ω discharge resistance, and the external load.

The REG3 and REG4 output voltage have a variable linear ramp rate that is set by a resistor connected from RAMP to AGND (R_{RAMP}). This resistor controls the output-voltage ramp rate during soft-start and a positive voltage change (i.e., 1.0V to 1.4V). The negative voltage change (i.e., 1.4V to 1.0V) is controlled in forced-PWM mode, and when the ARD bit is set in normal mode (Table 9). Figure 4 shows the relationship between R_{RAMP} and the output-voltage ramp rates. A 56kΩ R_{RAMP} satisfies the typical requirements of Intel XScale processors; 200µs after being enabled, REG3 and REG4 linearly ramp from 0V to the set output voltage at the rate set by R_{RAMP}. When REG3 and REG4 are disabled, the output voltage decays at a rate determined by the output capacitance, internal 550Ω discharge resistance, and the external load.

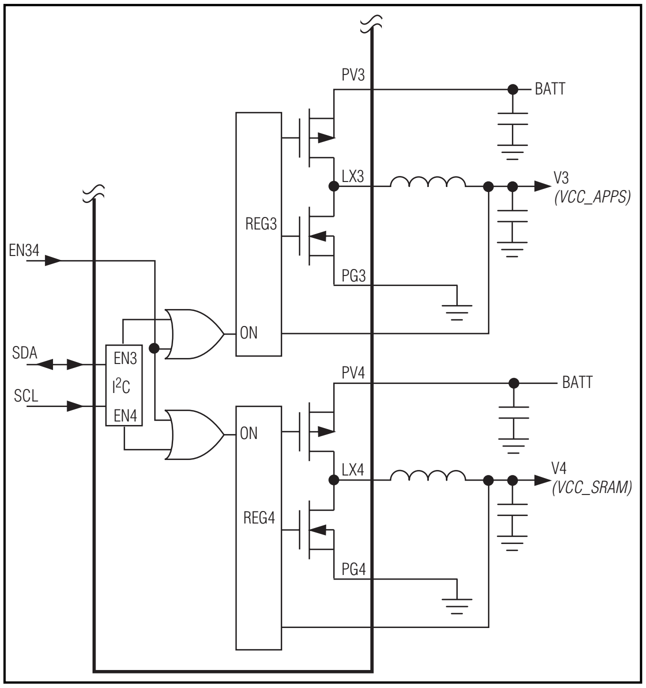


Figure 5. V3/V4 Enable Logic

Active ramp-down functionality is inherent in forced-PWM operation. In normal-mode operation, active ramp down is enabled by setting ARD3 and ARD4 (Table 9). With "active ramp-down" enabled, the regulator output voltage ramps down at the rate set by R_{RAMP}. With small loads, the regulator must sink current from the output capacitor to actively ramp down the output voltage. In normal mode, with "active ramp-down" disabled, the regulator output voltage ramps down at the rate determined by the output capacitance and the external load; small loads result in an output-voltage decay that is slower than that specified by R_{RAMP}, large loads (> C_{OUT} x RAMPRATE) result in an output-voltage decay that is no faster than that specified by R_{RAMP}.

80µs after being enabled, REG5 linearly ramps from 0V to the set output voltage in 225µs. The ramp rate during a positive voltage change (i.e., 1.8V to 1.9V) is set with R_{RAMP}. During a negative voltage change (i.e., 1.9V to 1.8V), the REG5 output voltage decays at a rate determined by the output capacitance and the external load; however, ramp-down is no faster than the rate specified by R_{RAMP}. When REG5 is disabled, the output voltage decays at a rate determined by the output capacitance, internal 2kΩ discharge resistance, and the external load.

60µs after being enabled by I^2C, REG6 and REG7 linearly ramp from 0V to the set output voltage in 450µs. REG6 and REG7 do not have positive voltage-change (i.e., 1.8V to 2.5V) ramp-rate control. During a positive voltage change, the output-voltage dV/dt is as fast as possible. To avoid this fast output dV/dt, disable REG6 or REG7 before changing the output. With this method, the soft-start ramp rate limits the output dV/dt, and therefore, the input current is controlled. During a negative voltage change (i.e., 2.5V to 1.8V), the REG6 or REG7 output voltage decays at a rate determined by the output capacitance and the external load. When REG6 or REG7 is disabled, the output voltage decays at a rate determined by the output capacitance, internal 350Ω discharge resistance, and the external load.

Power Sequencing

Enable Signals (EN_, PWR_EN, SYS_EN, I^2C)

As shown in Table 5, the MAX8660/MAX8661 feature numerous enable signals for flexibility in many applications. In a typical application with the Intel XScale processor, many of these enable signals are connected together. EN1, EN2, and EN5 typically connect to Intel's SYS_EN output. With this connection, REG5 is the first

POWER DOMAIN	MAXIM ENABLE SIGNAL		INTEL ENABLE SIGNAL
	HARDWARE	SOFTWARE	
V1 (*VCC_IO*) (MAX8660/MAX8660A only)	EN1	—	*SYS_EN*
V2 (*VCC_MEM*)	EN2	—	
V5 (*VCC_MVT*)	EN5	—	
V3 (*VCC_APPS*)	EN34	EN3 (OVER1)	*PWR_EN & PWR_I²C*
V4 (*VCC_SRAM*)		EN4 (OVER1)	
V6 (*VCC_CARD1*)	—	EN6 (OVER2)	*Standard I²C*
V7 (*VCC_CARD2*) (MAX8660/MAX8660A only)	—	EN7 (OVER2)	
V8 (*VCC_BBATT*)	Always on		—

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supply to rise (if IN5 is connected to IN). EN34 typically connects to Intel's PWR_EN output. Alternatively, REG3 and REG4 can be activated by the I²C interface (see the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information). REG6 and REG7 are activated by the serial interface. REG8 has no enable input and always remains on as long the MAX8660/MAX8661 are powered between the UVLO and OVLO range. All regulators are forced off during UVLO and OVLO. See the *Undervoltage and Overvoltage Lockout* section for more information.

Note: The logic that controls the Intel XScale processor *SYS_EN* and *PWR_EN* signals is powered from the *VCC_BBATT* power domain.

REG3/REG4 Enable (EN34, EN3, EN4)

REG3 and REG4 have independent I²C enable bits (EN3, EN4) and a shared hardware-enable input (EN34). As shown in Figure 5, the EN34 hardware-enable input is logically ORed with the I²C enable bits. Table 6 is the truth table for the V3/V4 enable logic. Note that to achieve a pure I²C enable/disable, connect EN34 to ground. Similarly, to achieve a pure hardware enable/disable, leave the I²C enable bits at their default value (EN3 = EN4 = 0 = off); V3 and V4 cannot be independently enabled/disabled using only hardware.

Table 6. Truth Table for V3/V4 Enable Logic

HARDWARE INPUT	I²C BITS		V3	V4
EN34	EN3	EN4		
0	0 (default)	0 (default)	OFF	OFF
0	0	1	OFF	ON
0	1	0	ON	OFF
X	1	1	ON	ON
1	X	X	ON	ON

X = Don't care.

Note: A low $\overline{MR}$ drives $\overline{RSO}$ low and returns the I²C registers to their default values: EN3 = 0 and EN4 = 0.

Power Modes

The MAX8660/MAX8661 provide numerous enable signals (Table 5) and support any combination for enabling and disabling their supplies with these signals. Table 7 shows several power modes defined for Intel XScale processors along with their corresponding MAX8660/MAX8661 quiescent operating currents.

Table 7. Power Modes and Corresponding Quiescent Operating Currents

POWER MODE	POWER DOMAIN STATE	DIGITAL CONTROL STATE	MAX8660 QUIESCENT OPERATING CURRENT (FIGURE 3)	
			NORMAL OPERATING MODE	FORCED-PWM MODE
ALL ON	V1, V2, V3, V4, V5, V6, V7, and V8 are on	EN1/EN2/EN5 (*SYS_EN*) and EN34 (*PWR_EN*) are asserted. V6, V7 are enabled by I²C	250µA	23mA
RUN, IDLE, and STANDBY	V1, V2, V3, V4, V5, and V8 are on	EN1/EN2/EN5 (*SYS_EN*) and EN34 (*PWR_EN*) are asserted	140µA	22.9mA
	V6 and V7 are off	V6 and V7 are disabled by I²C (default)		
SLEEP	V1, V2, V5, and V8 are on	EN1/EN2/EN5 (*SYS_EN*) are asserted	90µA	10mA
	V3, V4, V6, and V7 are off	EN34 (*PWR_EN*) is deasserted; V6 and V7 are disabled by I²C (default)		
DEEP SLEEP	All supplies off except V8	EN1/EN2/EN5 (*SYS_EN*) and EN34 (*PWR_EN*) are deasserted; V6, V7 are disabled by I²C	20µA	

Note: *Forced-PWM currents are measured on the MAX8660 EV kit. Currents vary with step-down inductor and output capacitor tolerance.*

Power-Up and Power-Down Timing

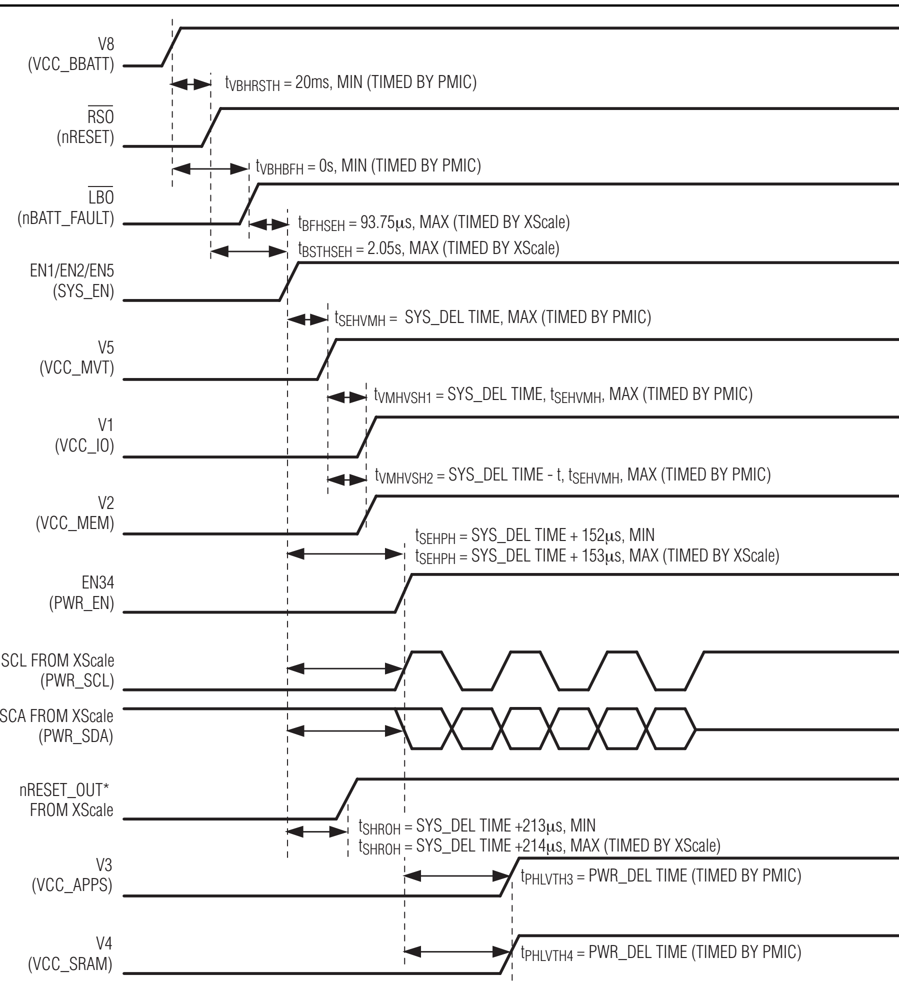
Figure 6 shows the power-up sequence for the Intel XScale family of processors. In general, the supplies should power up in the following order:

1) POWER-UP: V8 ➔ V5 ➔ V1 and V2 ➔ V3 and V4
2) REG6 and REG7 typically power external card slots and can be powered up and down based on application requirements.

Note that the Intel XScale processor controls EN1/EN2/EN5 with the same *SYS_EN* signal, yet Intel's timing diagrams show that V5 is supposed to power up before V1 and V2. Because of the Intel XScale family's timing parameters, most systems connect EN1/EN2/EN5 together and drive them with *SYS_EN*. When powering up, this connection ensures that V5 powers up before V1 and V2 (only when V5 is powered from IN).

Intel XScale Power Configuration Register (PCFR)

The MAX8660/MAX8661 comply with the Intel XScale power I²C register specifications. This allows the PMIC to be used along with the Intel XScale processor with little-to-no software development. As shown in Table 9, there are many I²C registers, but since the Intel XScale processor automatically updates the PMIC through its power I²C interface, only the REG6 and REG7 enable bits need be programmed to fully utilize the PMIC.



*THE MAX8660/MAX8661 DO NOT DIRECTLY USE THE INTEL XScale PROCESSOR'S nRESET_OUT LOGIC OUTPUT.

Figure 6. Power-Up Timing

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The Intel XScale processor contains a power management unit general configuration register (PCFR). The default values of this register are compliant with the MAX8660/MAX8661. However, wake-up performance can be optimized using this register:

- The PCFR register contains timers for the SYS_DEL and PWR_DEL timing parameters as shown in Figure 6. Each timer defaults to 125ms. When using the MAX8660/MAX8661, these timers may be shortened to 2ms to speed up the overall system wake-up delay.
- Enabling the "shorten wake-up delay" function (SWDD bit) bypasses the SYS_DEL and PWR_DEL timers and uses voltage detectors on the Intel XScale processor to optimize the overall system wake-up delay.

Voltage Monitors, Reset, and Undervoltage-Lockout Functions

Undervoltage and Overvoltage Lockout

When the V_{IN} is below V_{UVLO} (typically 2.35V), the MAX8660/MAX8661 enter its undervoltage-lockout mode (UVLO). UVLO forces the device to a dormant state. In UVLO, the input current is very low (1.5µA) and all regulators are off. $\overline{\text{RSO}}$ and $\overline{\text{LBO}}$ are forced low when the input voltage is between 1V (typ) and V_{UVLO}. The I²C does not function in UVLO, and the I²C register contents are reset in UVLO.

When the input voltage is above V_{OVLO} (typically 6.35V) the MAX8660/MAX8661 enter overvoltage-lockout mode (OVLO). OVLO mode protects the MAX8660/MAX8661 from high-voltage stress. In OVLO, the input current is 25µA and all regulators are off. $\overline{\text{RSO}}$ is held low, the I²C does not function, and register contents are reset in OVLO. $\overline{\text{LBO}}$ continues to function in OVLO; however, since $\overline{\text{LBO}}$ is typically pulled up to V8 (*VCC_BBATT*), $\overline{\text{LBO}}$ appears to go low in OVLO because V8 is disabled. Alternatively, $\overline{\text{LBO}}$ may be pulled up to IN.

Reset Output ($\overline{\text{RSO}}$) and $\overline{\text{MR}}$ Input

$\overline{\text{RSO}}$ is an open-drain reset output. As shown in Figure 1, $\overline{\text{RSO}}$ typically connects to the *nRESET* input of the Intel XScale processor and is pulled up to V8 (*VCC_BBATT*). A low on *nRESET* causes the processor to enter its reset state.

$\overline{\text{RSO}}$ is forced low when one or more of the following conditions occur:

- $\overline{\text{MR}}$ is low.
- V8 is below V_{RSOTH} (2.2V falling typ).
- V_{IN} is below V_{UVLO} (2.35V typ).
- V_{IN} is above V_{OVLO} (6.35V typ).

$\overline{\text{RSO}}$ is high impedance when all of the following conditions are satisfied:

- $\overline{\text{MR}}$ is high.
- V8 is above V_{RSOTH} (2.35V rising typ).
- $V_{UVLO} < V_{IN} < V_{OVLO}$.
- The $\overline{\text{RSO}}$ deassert delay ($t_{VBHRSTH}$ = 24ms typ) has expired.

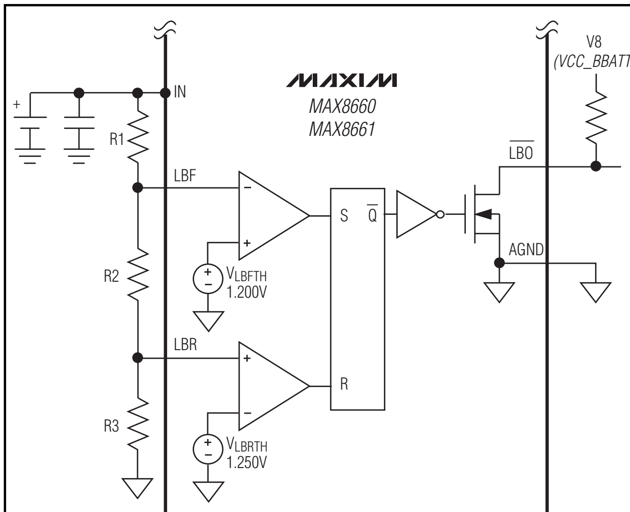
When $\overline{\text{RSO}}$ goes low, the MAX8660/MAX8661 I²C registers are reset to their default values.

If the $\overline{\text{MR}}$ feature is not required, connect $\overline{\text{MR}}$ high. If the $\overline{\text{RSO}}$ feature is not required, connect $\overline{\text{RSO}}$ low.

Low-Battery Detector ($\overline{\text{LBO}}$, LBF, LBR)

$\overline{\text{LBO}}$ is an open-drain output that typically connects to the *nBATT_FAULT* input of the Intel XScale processor to indicate that the battery has been removed or discharged (Figure 1). $\overline{\text{LBO}}$ is typically pulled up to V8 (*VCC_BBATT*).

LBR and LBF monitor the input voltage (usually a battery) and trigger the $\overline{\text{LBO}}$ output (Figure 7). The truth table in Figure 7 shows that $\overline{\text{LBO}}$ is high impedance when the voltage from LBR to AGND (V_{LBR}) exceeds the low-battery rising threshold (V_{LBRTH} = 1.25V (typ). $\overline{\text{LBO}}$ is low when the voltage from LBF to AGND (V_{LBF}) falls below the low-battery falling threshold (V_{LBFTH} = 1.20V typ). On power-up, the LBR threshold must be exceeded before $\overline{\text{LBO}}$ deasserts.



TRUTH TABLE		
LBF	LBR	$\overline{\text{LBO}}$
$V_{LBF} < V_{LBFTH}$	$V_{LBR} < V_{LBRTH}$	0
$V_{LBF} < V_{LBFTH}$	$V_{LBR} > V_{LBRTH}$	0
$V_{LBF} > V_{LBFTH}$	$V_{LBR} < V_{LBRTH}$	HOLD
$V_{LBF} > V_{LBFTH}$	$V_{LBR} > V_{LBRTH}$	1

Figure 7. Low-Battery Detector Functional Diagram

Connecting LBF to LBR and to a two-resistor voltage-divider sets a 50mV hysteresis referred to LBF (hysteresis at the battery voltage is scaled up by the resistor value), connecting LBF and LBR separately to a three-resistor voltage-divider (Figure 7) allows the falling threshold and rising threshold to be set separately (achieving larger hysteresis). The Figure 7 resistor values are selected as a function of the desired falling (V_{LBOF}) and rising (V_{LBOR}) thresholds as follows:

First, select R3 in the 100kΩ to 1MΩ range:

$$R1 = R3 \times \frac{V_{LBOR}}{V_{LBRTH}} \times \left(1 - \frac{V_{LBFTH}}{V_{LBOF}}\right)$$

$$R2 = R3 \times \left(\frac{V_{LBFTH} \times V_{LBOR}}{V_{LBRTH} \times V_{LBOF}} - 1\right)$$

where V_{LBOR} is the rising voltage at the top of R1 (typically V_{IN}) when $\overline{LBO}$ goes high, and V_{LBOF} is the falling voltage at the top of R1 when $\overline{LBO}$ goes low.

For example, to set V_{LBOR} to 3.6V and V_{LBOF} to 3.2V, choose R3 to be 1MΩ. Then, R1 = 1.8MΩ and R2 = 80kΩ.

If the low-battery-detector feature is not required, connect $\overline{LBO}$ to ground and connect LBF and LBR to IN.

Internal Off-Discharge Resistors

Each regulator on the MAX8660/MAX8661 has an internal resistor that discharges the output capacitor when the regulator is off (Table 8). The internal discharge resistors pull their respective output to ground when the regulator is off, ensuring that load circuitry always powers down completely. The internal off-discharge resistors are active when a regulator is disabled, when the device is in OVLO, and when the device is in UVLO with V_{IN} greater than 1.0V. With V_{IN} less than 1.0V, the internal off-discharge resistors may not activate.

Table 8. Internal Off-Discharge Resistor

REGULATOR	INTERNAL OFF-DISCHARGE RESISTOR VALUE
REG1	650Ω ±30%
REG2	650Ω ±30%
REG3	550Ω ±30%
REG4	550Ω ±30%
REG5	2kΩ ±30%
REG6	350Ω ±30%
REG7	350Ω ±30%
REG8	1.5kΩ ±30%

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8660/MAX8661. When internal thermal sensors detect a die temperature in excess of +160°C, the corresponding regulator(s) are shut down, allowing the IC to cool. The regulators turn on again after the junction cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

A thermal overload on any of REG1 through REG5 only shuts down the overloaded regulator. An overload on REG6 or REG7 shuts down both regulators together. During thermal overload, REG8 is not turned off, and the I^2C interface and voltage monitors remain active.

I^2C Interface

An I^2C-compatible, 2-wire serial interface controls a variety of MAX8660/MAX8661 functions:

- The output voltages of V3–V7 are set by the serial interface.
- Each of the four step-down DC-DC converters (REG1/REG4) can be put into forced-PWM operation.
- REG3 and REG4 can be enabled by the serial interface or by a hardware-enable pin (EN34). See the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information.
- REG6 and REG7 are activated only by the serial interface.

The serial interface operates whenever V_{IN} is between V_{UVLO} (typically 2.40V) and V_{OVLO} (typically 6.35V). When V_{IN} is outside the I^2C operation range, the I^2C registers are reset to their default values.

The serial interface consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The MAX8660/MAX8661 are slave-only devices, relying upon a master to generate a clock signal. The master (typically the Intel XScale processor) initiates data transfer on the bus and generates SCL to permit data transfer.

I^2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize cross-talk and undershoot on bus signals.

The Intel XScale specification contains an extensive list of registers for various functions, not all of which are provided on the MAX8660/MAX8661. The list in Table 9 is a subset of the Intel list as it relates to functions included in the PMIC. Even though the MAX8660/MAX8661 use a subset of the Intel XScale-specified registers, they acknowledge writes to the entire register space (0x00 to 0xFF).

In Intel XScale applications, the pullups are typically to VCC_IOx.

Table 9. I²C Registers

REGISTER ADDRESS	REGISTER NAME	R/W	FUNCTION		DATA BIT 7	6	5	4	3	2	1	0
0x10	OVER1*	W	Output-Voltage Enable Register 1. Enables/disables V3 and V4. See the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information.		R	R	R	R	R	**EN4 (S_EN)**	R	**EN3 (A_EN)**
				Default	0	0	0	0	0	0	0	0
0x12	OVER2	W	Output-Voltage Enable Register 2. Enables/disables V6 and V7. See the *REG6/REG7 (VCC_CARD1, VCC_CARD2)* section for more information.		R	—	—	—	—	**EN7****	**EN6**	—
				Default	0	0	0	0	0	0	0	0
0x20	VCC1*	W	Voltage-Change Control Register. Independently specifies that the V3, V4, and V5 output voltage must follow either target register 1 or 2. See Table 10.		**MVS**	**MGO**	**SVS**	**SGO**	R	R	**AVS**	**AGO**
				Default	0	0	0	0	0	0	0	0
0x23	ADTV1*	W	VCC_APPS (V3) DVM Target Voltage 1 Register. Sets target 1 voltage for V3.		R	R	R	**V3 (VCC_APPS) Target 1**—See Table 11				
				Default	0	0	0	1	1	0	1	1
0x24	ADTV2*	W	VCC_APPS (V3) DVM Target Voltage 2 Register. Sets target 2 voltage for V3.		R	R	R	**V3 (VCC_APPS) Target 2**—See Table 11				
				Default	0	0	0	1	1	0	1	1
0x29	SDTV1*	W	VCC_SRAM (V4) DVM Target Voltage 1 Register. Sets target 1 voltage for V4.		R	R	R	**V4 (VCC_SRAM) Target 1**—See Table 11				
				Default	0	0	0	1	1	0	1	1
0x2A	SDTV2*	W	VCC_SRAM (V4) DVM Target Voltage 2 Register. Sets target 2 voltage for V4.		R	R	R	**V4 (VCC_SRAM) Target 2**—See Table 11				
				Default	0	0	0	1	1	0	1	1
0x32	MDTV1	W	VCC_MVT (V5) Target Voltage 1 Register. Sets target 1 voltage for V5.		R	R	R	**V5 (VCC_MVT) Target 1**—See Table 12				
				Default	0	0	0	0	0	1	0	0
0x33	MDTV2	W	VCC_MVT (V5) DVM Target Voltage 2 Register. Sets target 2 voltage for V5.		R	R	R	**V5 (VCC_MVT) Target 2**—See Table 12				
				Default	0	0	0	0	0	1	0	0
0x39	L12VCR	W	LDO1 and LDO2 Voltage-Control Register (V6 and V7 on MAX8660). Specifies the V6 and V7 output voltage. V6 and V7 are enabled/disabled with OVER2.		**V7 Voltage**—See Table 13				**V6 Voltage**—See Table 13			
				Default	0	0	0	0	0	0	0	0
0x80	FPWM	W	Forced-PWM Register. The FPWM_ bits allow V1, V2, V3, and V4 to independently operate in either skip mode or forced-PWM mode. See the *REG1–REG4 Step-Down DC-DC Converter Operating Modes* section for more information. The ARD_ bits allow the output voltage to be actively ramped down during negative voltage transitions See the *Ramp-Rate Control (RAMP)* section for more information. Note that this is a Maxim custom register that is not required by the Intel XScale processor.		**ARD4**	**ARD3**	—	—	**FPWM4**	**FPWM3**	**FPWM2**	**FPWM1****
				Default	0	0	0	0	0	0	0	0

R means these data locations are designated reserved in the Intel specification.

Note: *The MAX8660/MAX8661 acknowledge attempts to write to the entire address space from 0x00 to 0xFF, even though only a subset of those addresses actually exist in the IC.*

** These registers are accessed by the power I²C bus of the Intel XScale processor.*

*** Maintain these bits at their default 0 value for the MAX8661.*

Table 10. DVM Voltage-Change Register (VCC1, 0x20)

REGISTER ADDRESS	REGISTER NAME	BIT	NAME	FUNCTION
0x20	VCC1	7	MVS	V5 (*VCC_MVT*) voltage select: 0—Ramp V5 to voltage selected by MDTV1 (default) 1—Ramp V5 to voltage selected by MDTV2
		6	MGO	Start V5 (*VCC_MVT*) voltage change: 0—Hold V5 at current level (default) 1—Ramp V5 as selected by MVS
		5	SVS	V4 (*VCC_SRAM*) voltage select: 0—Ramp V4 to voltage selected by SDTV1 (default) 1—Ramp V4 to voltage selected by SDTV2
		4	SGO	Start V4 (*VCC_SRAM*) voltage change: 0—Hold V4 at current level (default) 1—Ramp V4 as selected by SVS
		3	R	Reserved
		2	R	Reserved
		1	AVS	V3 (*VCC_APPS*) voltage select: 0—Ramp V3 to voltage selected by ADTV1 (default) 1—Ramp V3 to voltage selected by ADTV2
		0	AGO	Start V3 (*VCC_APPS*) voltage change: 0—Hold V3 at current level (default) 1—Ramp V3 as selected by AVS

Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section for more information).

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long; 8 bits of data followed by the acknowledge bit. The MAX8660/MAX8661 suport data transfer rates with SCL frequencies up to 400kHz.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high (Figure 7).

A START condition from the master signals the beginning of a transmission to the MAX8660/MAX8661. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *Acknowledge Bit* section for more information). The STOP condition frees the bus. To issue a series of commands to the slave, the master may issue repeated start (Sr) commands instead of a stop command in order to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

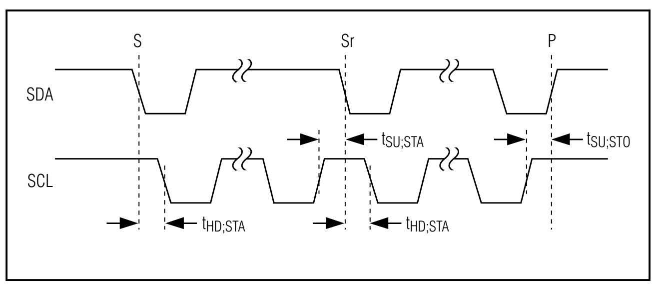


Figure 8. START and STOP Conditions

When a STOP condition or incorrect address is detected, the MAX8660/MAX8661 internally disconnect SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

Table 11. Serial Codes for V3 (*VCC_APPS)* and V4 (*VCC_SRAM*) Output Voltages

REGISTER ADDRESS	REGISTER NAME	DATA BYTE	OUTPUT VOLTAGE (V)
0x23 0x24 0x29 0x2A	ADTV1 ADTV2 SDTV1 SDTV2	0x00	0.725
		0x01	0.750
		0x02	0.775
		0x03	0.800
		0x04	0.825
		0x05	0.850
		0x06	0.875
		0x07	0.900
		0x08	0.925
		0x09	0.950
		0x0A	0.975
		0x0B	1.000
		0x0C	1.025
		0x0D	1.050
		0x0E	1.075
		0x0F	1.100
		0x10	1.125
		0x11	1.150
		0x12	1.175
		0x13	1.200
		0x14	1.225
		0x15	1.250
		0x16	1.275
		0x17	1.300
		0x18	1.325
		0x19	1.350
		0x1A	1.375
		0x1B	**1.400 (default)***
		0x1C	1.425
		0x1D	1.450
		0x1E	1.475
		0x1F	1.500
		0x20	1.525
		0x21	1.550
		0x22	1.575
		0x23	1.600
		0x24	1.625
		0x25	1.650
		0x26	1.675
		0x27	1.700
		0x28	1.725
		0x29	1.750
		0x2A	1.775
		0x2B	1.800

**Contact factory for other default voltages.*

Table 12. Serial Codes for V5 Output Voltage

REGISTER ADDRESS	REGISTER NAME	DATA BYTE	OUTPUT VOLTAGE (V)
0x32 0x33	MDTV1 MDTV2	0x00	1.700
		0x01	1.725
		0x02	1.750
		0x03	1.775
		0x04	**1.800 (default)**
		0x05	1.825
		0x06	1.850
		0x07	1.875
		0x08	1.900
		0x09	1.925
		0x0A	1.950
		0x0B	1.975
		0x0C	2.000

Table 13. Serial Codes for V6 and V7 Output Voltages

REGISTER ADDRESS	REGISTER NAME	DATA NIBBLE	OUTPUT VOLTAGE (V)
0x39	L12VCR	**0x0**	**1.8 (default)**
		0x1	1.9
		0x2	2.0
		0x3	2.1
		0x4	2.2
		0x5	2.3
		0x6	2.4
		0x7	2.5
		0x8	2.6
		0x9	2.7
		0xA	2.8
		0xB	2.9
		0xC	3.0
		0xD	3.1
		0xE	3.2
		0xF	3.3

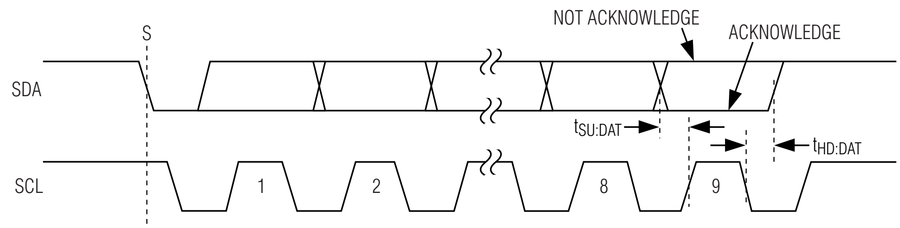


Figure 9. Acknowledge Bits

SRAD	SLAVE ADDRESS (WRITE)	
	BINARY	HEXADECIMAL
0 (GND)	0b 0110 1000	0x68
1 (IN)	0b 0110 1010	0x6A

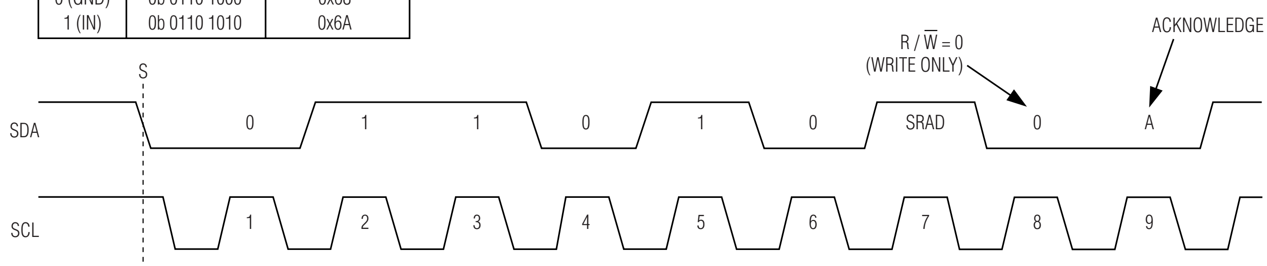


Figure 10. Slave Address Byte

Acknowledge Bit

Both the master and the MAX8660/MAX8661 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 9). To generate a not acknowledge ($\overline{A}$), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

A bus master initiates communication with a slave device (MAX8660/MAX8661) by issuing a START condition followed by the slave address. As shown in Figure 10, the slave address byte consists of 7 address bits and a read/write bit (R/$\overline{W}$). After receiving the proper address, the MAX8660/MAX8661 issue an acknowledge by pulling SDA low during the ninth clock cycle. Note that the R/$\overline{W}$ bit is always zero since the MAX8660/MAX8661 are write only.

The Intel XScale processor supports 0x68 (SRAD = GND) as the I^{2}C slave address.

I^{2}C Write Operation

The MAX8660MAX8661 are write-only devices and recognize the “write byte” protocol as defined in the SMBus specification and shown in section A of Figure 11. The “write byte” protocol allows the I^{2}C master device to send 1 byte of data to the slave device. The “write byte” protocol requires a register pointer address for the subsequent write. The MAX8660/MAX8661 acknowledge any register pointer even though only a subset of those registers actually exists in the device. The “write byte” protocol is as follows:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.

8) The slave acknowledges the data byte.
9) The master sends a STOP condition.

In addition to the write-byte protocol, the MAX8660/MAX8661 recognize the multiple byte register-data pair protocol as shown in section B of Figure 11. This protocol allows the I²C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a STOP condition.

The multiple-byte register-data pair protocol is as follows:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 5 to 7 are repeated as many times as the master requires. Registers may be accessed in random order.
10) The master sends a STOP condition.

Design Procedure

Setting the Output Voltages

The REG1 and REG2 regulators each have three preset voltages that are programmed with the SET1 and SET2 inputs. See the *REG1 (VCC_IO) Step-Down DC-DC Converter* and *REG2 (VCC_IO, VCC_MEM) Step-Down DC-DC Converters* sections for more information. V8 is fixed at 3.3V and cannot be changed.

V3–V7 are set by the I²C interface. See the *I²C Interface* section for more information. Note that while operating in forced-PWM mode with an input voltage greater than 4.3V, the minimum output voltage of REG3 and REG4 is limited by the minimum duty cycle. In forced-PWM mode, the minimum output voltage for REG3 or REG4 is:

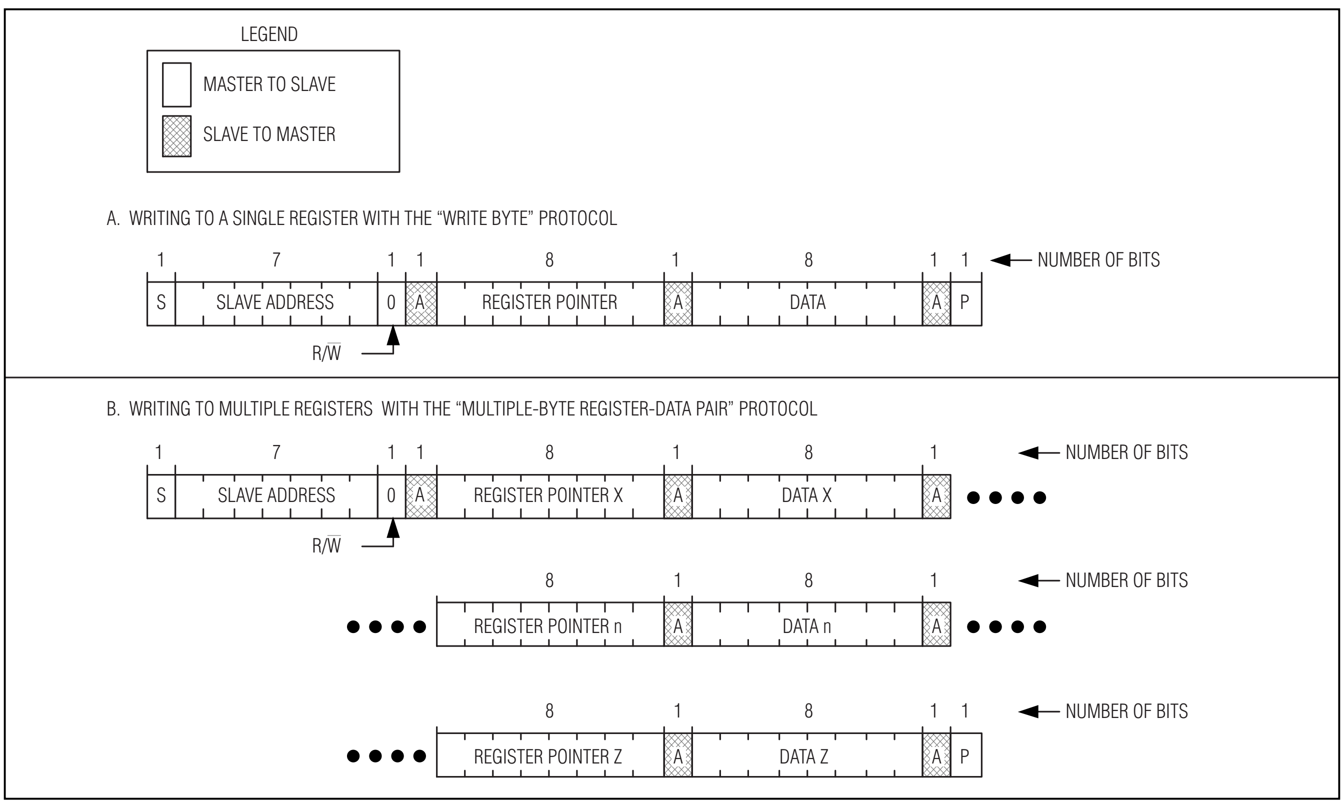


Figure 11. Writing to the MAX8660/MAX8661

$$V3_{MIN} = 0.167 \times V_{PV3}$$
$$V4_{MIN} = 0.167 \times V_{PV4}$$

Note that the above minimum voltage limitation does not apply to normal-mode operation.

Inductor Selection

Calculate the inductor value (L_{IDEAL}) for each of REG1 through REG4 as follows:

$$L_{IDEAL} = \frac{4 \times V_{IN} \times D \times (1 - D)}{I_{OUT(MAX)} \times f_{OSC}}$$

This sets the peak-to-peak inductor current ripple to 1/4 the maximum output current. The oscillator frequency, f_{OSC}, is 2MHz, and the duty cycle, D, is:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Given L_{IDEAL}, the peak-to-peak inductor ripple current is 0.25 x $I_{OUT(MAX)}$. The peak inductor current is 1.125 x $I_{OUT(MAX)}$. Make sure that the saturation current of the inductor exceeds the peak inductor current, and the rated maximum DC inductor current exceeds the maximum output current ($I_{OUT(MAX)}$). Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, peak inductor current rises and a larger output capacitance may be required to suppress output ripple. Larger inductance values than L_{IDEAL} can be used to obtain higher output current, but typically require physically larger inductor size. Refer to the MAX8660 EV kit data sheet for specific inductor recommendations.

Input Capacitor Selection

The input capacitor in a step-down DC-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents do not pass through the input source.

The input capacitor must meet the input-ripple-current requirement imposed by the step-down converter. Ceramic capacitors are preferred due to their resilience to power-up surge currents. Choose the input capacitor so that the temperature rise due to input ripple current does not exceed approximately 10°C. For a step-down DC-DC converter, the maximum input ripple current is 1/2 of the output. This maximum input ripple current occurs when the step-down converter operates at 50% duty factor ($V_{IN} = 2 \times V_{OUT}$).

Refer to the MAX8660 EV kit data sheet for specific input capacitor recommendations.

Output Capacitor Selection

The step-down DC-DC converter output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and lowest high-frequency impedance.

Output ripple due to capacitance (neglecting ESR) is approximately:

$$V_{RIPPLE} = \frac{I_{L(PEAK)}}{2\pi \times f_{OSC} \times C_{OUT}}$$

Additional ripple due to capacitor ESR is:

$$V_{RIPPLE(ESR)} = I_{L(PEAK)} \times ESR$$

Refer to the MAX8660 EV kit data sheet for specific output capacitor recommendations.

Applications Information

Power Dissipation

The MAX8660/MAX8661 have a thermal-shutdown feature that protects the IC from damage when the die temperature exceeds +160°C (see the *Thermal-Overload Protection* section for more information). To prevent thermal overload and allow the maximum load current on each regulator, it is important to ensure that the heat generated by the MAX8660/MAX8661 can be dissipated into the PC board. The exposed pad must be soldered to the PC board, with multiple vias under the exposed pad (EP) conducting heat to a ground plane.

The junction-to-case thermal resistance (θ_{JC}) of the MAX8660/MAX8661 is 2.7°C/W. When properly mounted on a multilayer PC board, the junction-to-ambient thermal resistance (θ_{JA}) is typically 28°C/W.

PC Board Layout and Routing

Good printed circuit board (PC board) layout is necessary to achieve optimal performance. Conductors carrying discontinuous currents and any high-current path must be made as short and wide as possible.

Refer to the MAX8660 EV kit data sheet for an example of a good PC board layout. Place the bypass capacitors for each power input pair (IN to AGND, PV1 to PG1, PV2 to PG2, PV3, to PG3, and PV4 to PG4) as close as possible to the IC.

The exposed pad (EP) is the main path for heat to exit the IC. Connect EP to the ground plane with multiple vias to allow heat to dissipate from the device.

High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications

Package Marking

TOP VIEW

MAXIM 8660E TLyww + aaaa	MAXIM 8660AE TLyww + aaaa	MAXIM 8661E TLyww + aaaa

"yww" is a date code.
"aaaa" is an assembly code.
+ Denotes lead-free packaging and marks pin 1 location.

Chip Information

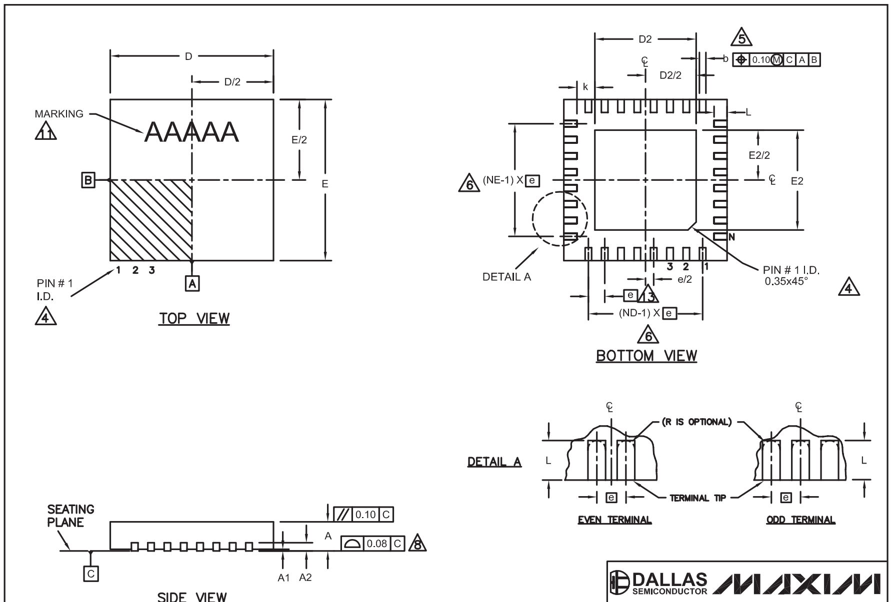
PROCESS: BiCMOS

High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. J | 1/2

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

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DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

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