

Dual P-Channel 60-V (D-S) 175° MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- · Level 3 MOS

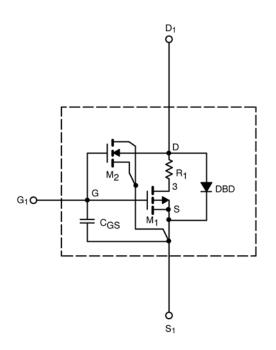
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

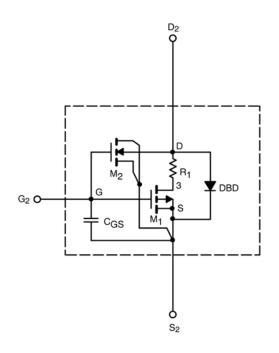
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|------------------------|---|-------------------|------------------|------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V_{DS} = V_{GS} , I_D = -250 μ A | 2.1 | | V |
| On-State Drain Current ^a | I _{D(on)} | V_{DS} = -5 V, V_{GS} = -10 V | 50 | | А |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V_{GS} = -10 V, I _D = -3.1 A | 0.100 | 0.100 | Ω |
| | | V_{GS} = -4.5 V, I _D = -2 A | 0.120 | 0.126 | |
| Forward Transconductance ^a | g _{fs} | V_{DS} = -15 V, I _D = -3.1 A | 7 | 8.5 | S |
| Diode Forward Voltage ^a | V _{SD} | $I_{\rm S}$ = -2 A, $V_{\rm GS}$ = 0 V | -0.81 | -0.80 | V |
| Dynamic ^b | ! | | - | | |
| Total Gate Charge | Qg | V_{DS} = -30 V, V_{GS} = -10 V, I_D = -3.1 A | 13 | 14.5 | nC |
| Gate-Source Charge | Q _{gs} | | 2.2 | 2.2 | |
| Gate-Drain Charge | Q _{gd} | | 3.7 | 3.7 | |
| Turn-On Delay Time | t _{d(on)} | $\label{eq:V_DD} \begin{array}{l} V_{\text{DD}} = -30 \ \text{V}, \ \text{R}_{\text{L}} = 30 \ \Omega \\ \text{I}_{\text{D}} \cong -1 \ \text{A}, \ \text{V}_{\text{GEN}} = -10 \ \text{V}, \ \text{R}_{\text{G}} = 6 \ \Omega \end{array}$ | 10 | 10 | ns |
| Rise Time | tr | | 14 | 15 | |
| Turn-Off Delay Time | t _{d(off)} | | 40 | 50 | |
| Fall Time | t _f | | 22 | 35 | |

Notes

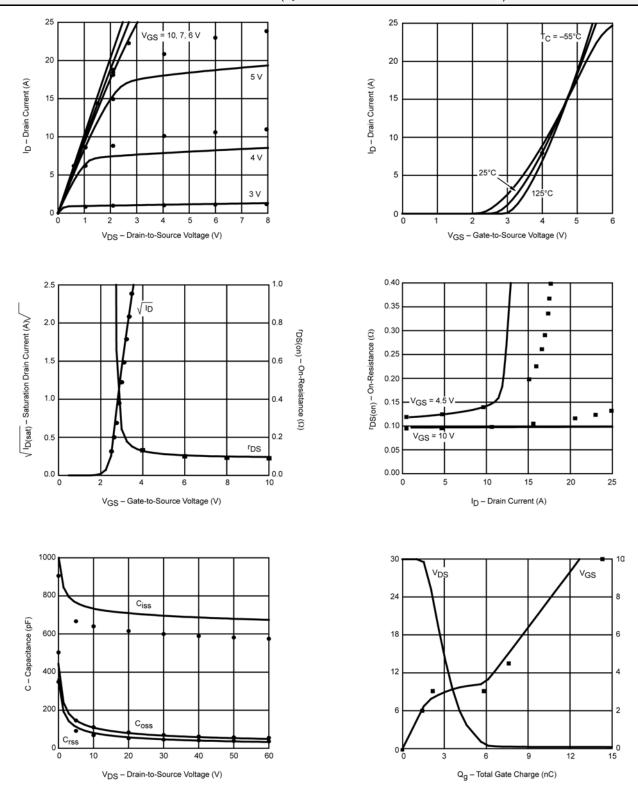
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si4948BEY

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Vishay

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