AND8029/D

Ramp Compensation for the NCP1200

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APPLICATION NOTE

INTRODUCTION

As any current–mode controllers, the NCP1200 can be subject to subharmonic oscillations. Oscillations take place when the Switch–Mode Power Supply (SMPS) operates in Continuous Conduction Mode (CCM) together with a duty–cycle near or greater than 50%. For Discontinuous Conduction Mode (DCM) designs, this normally does not happen. However, at the lowest line levels and when the SMPS is pushed to its upper output power capability, CCM can engender these oscillations within the current loop. This application note details how to properly cure this problem by injecting the correct amount of ramp compensation.

Origin of the Problem

A current–mode power supply is a two–loop system: one loop controls the inductor peak current while the other monitors the output voltage. The current loop is actually embedded into the voltage loop which fixes the final current setpoint. In CCM operation, the action of the current loop can be compared to a sample and hold device. This sampling action creates a pair of RHP zeroes in the current loop which are responsible for the boost in gain at $F_{switching}/2$ but also stress the phase lag at this point. If the gain margin is too low at this frequency, any perturbation in the current will make the system unstable since, as we said, both voltage and current loops are embedded. You can fight the problem by providing the converter with an external compensation ramp. This ramp will oppose the duty cycle action by lowering the current–loop DC gain, correspondingly increasing the phase margin at $F_{switching}/2$, finally damping the high Q poles in the $V_{out}/V_{control}$ transfer function. As other benefits of ramp compensation, Ray Ridley [1] confirmed that an external ramp whose slope is equal to 50% ($m_c = 1.5$) of the inductor downslope could nullify the audio susceptibility in a BUCK converter, as already calculated by Holland [2]. As more external ramp is added, the low frequency pole ω_p moves to higher frequencies while the double poles will be split into two distinct poles. The first one will move towards lower frequencies until it joins and combines with the first low frequency pole at ω_p. At this point, the converter behaves as if it is operating in voltage mode.

Lowering the Peaking

A current mode controlled SMPS exhibits one low frequency pole, ω_p, and two poles which are located at $F_{switching}/2$. These poles move in relation to the duty cycle and the external compensation ramp, when present. The two high frequency poles present a Q that depends on the compensating ramp and the duty–cycle. Ridley demonstrated that the Q becomes infinite at D = 0.5 with no external ramp (mc = 1), confirming the inherent instability of a CCM current–mode SMPS operating at a duty cycle greater than 0.5. Below stands the definition of this quality coefficient:

$Q = \frac{1}{\pi \cdot (mc \cdot D' - 0.5)}$ where $m_c = 1 + S_e/S_n$. S_e is the external ramp slope, S_n is the inductor on–time slope and $D' = 1 - D$.

For designers, once the system's Q has been determined, they should look for the amount of ramp compensation that will make this number equal to 1: $mc = \left[\frac{1}{\pi} + 0.5\right] \cdot \frac{1}{D'}$.

How to Create a Ramp?

On the NCP1200, you do not have access to any oscillator sawtooth. However, you can easily charge a capacitor when the gate drive is high, and immediately discharge it when the MOSFET switches off. Figure 1a shows how to simply generate a sawtooth from the gate drive:

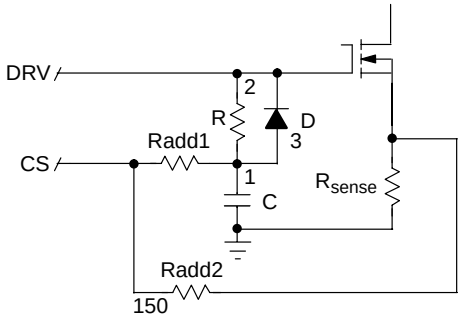

Figure 1a

A very simple way to generate a ramp from a square wave signal.

Calculating the RC component values is a rather easy task. By drawing the smallest current from the drive to avoid increasing the standby power, R shall be of high value. If this is the case, you can consider this system as a current generator. By applying $Vc \cdot C = i \cdot t$, you calculate R and C. Suppose we want to create a ramp that goes up to 5.0 V when a 60 kHz NCP1200 is operating at 50% duty–cycle. The ON time is therefore $\frac{1}{2 \cdot 60\,k} = 8.3\,\mu s$. In order to not bothering the NCP1200 operation, let's select a charging current of 250 μA. With a gate plateau of 11 V, this leads to a resistor of ≈11 V/250 μA = 44 kΩ. With a charging current of 250 μA, what capacitor do we need to generate a ramp that reaches 5.0 V in 8.33 μs? Well, $C = \frac{250\,\mu \cdot 8.33\,\mu}{5} = 416\,pF$. However, because the charging current varies during the ramping (we actually obtain an exponential), we will to reduce both elements to their next lower normalized values, e.g., 39 kΩ and 390 pF. If we feed our SPICE simulator with these values, Figure 1b and 1c confirms the calculations:

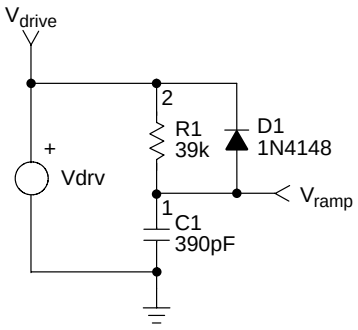

Figure 1b

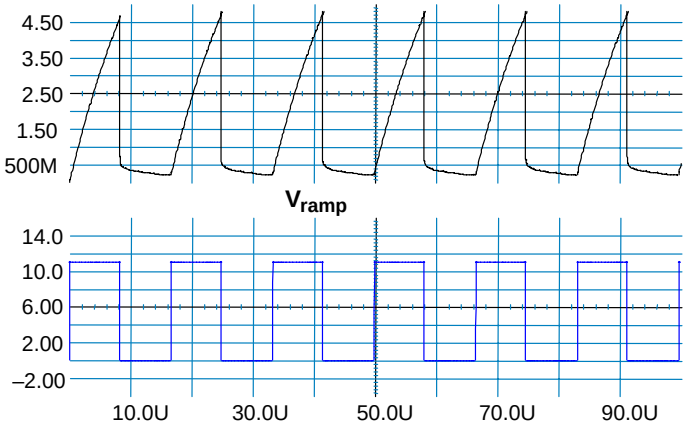

Figure 1c

A simple simulation schematic confirms the calculations: the capacitor voltage ramps up from a few hundred of mV up to nearly 5.0 V.

By ramping from 0.6 V to 4.5 V in 8.3 μs, we have created a signal exhibiting a slope of 468 mV/μs.

"What compensation level shall I inject?"

Let's suppose the following specs for our FLYBACK converter:

VHV_{DC} = 110 V
Fsw = 60 kHz
Lp = 1.8 mH
η = 80%
N = Np:Ns = 0.1
$Pout_{max}$ = 15 W

To calculate the operating duty–cycle D, we need to compute the peak current authorizing a 15 W output power flow from the 1.8 mH primary inductance: $Pin = \frac{1}{2} \cdot Lp \cdot Ip? \cdot Fsw$. From our specs, we know that Pin = 15/08 = 18.8 W. At the boundary between DCM and CCM, the peak current is evaluated to: $Ip = \sqrt{\frac{2 \cdot Pin}{Lp \cdot Fsw}} = 590\,mA$. To reach this value, we need to apply VHV_{DC} over Lp during: $Ip \cdot \frac{Lp}{VHV_{DC}} = 9.6\,\mu s$. Compared to a 60 kHz switching frequency, it corresponds to a 58% duty–cycle or D = 0.58.

The external ramp injection will keep Q below 1. To adhere to this requirement, we must inject a compensating ramp mc equal to $\left[\frac{1}{\pi} + 0.5\right]$. $\frac{1}{D'} = 1.9$. By applying mc definition, we can deduct the final amount of external ramp we must inject: $mc = 1 + \frac{Se}{Sn}$ or $Se = (mc - 1) \cdot Sn$. In a FLYBACK, the ON slope Sn is given by the rectified DC rail applied over the primary inductance Lp: $Sn = \frac{VHV_{DC}}{Lp}$. With Lp = 1.8 mH, Rsense = 1.5 Ω and the lowest main equals 110 V, then Sn = 91.5 mV/μs once reflected in volts over Rsense. To get the final level of ramp compensation, let's compute Se by: $Se = (mc - 1) \cdot Sn$ or 82 mV/μs. To obtain this ramp from our ramping generator, we must create a division ratio of 0.082/468 or 175 m. If we select a 10 kΩ resistor to convey the current sense information, then the ramp resistor is calculated using: $\frac{10\,k - 0.175 \cdot 10\,k}{0.175}$ or 47 kΩ in this example.

Simulation of the Converter

To check our calculation, we can use the NCP1200 SPICE model. Figure 2a portrays the application schematic for this converter with INTUSOFT's IsSpice4 model version:

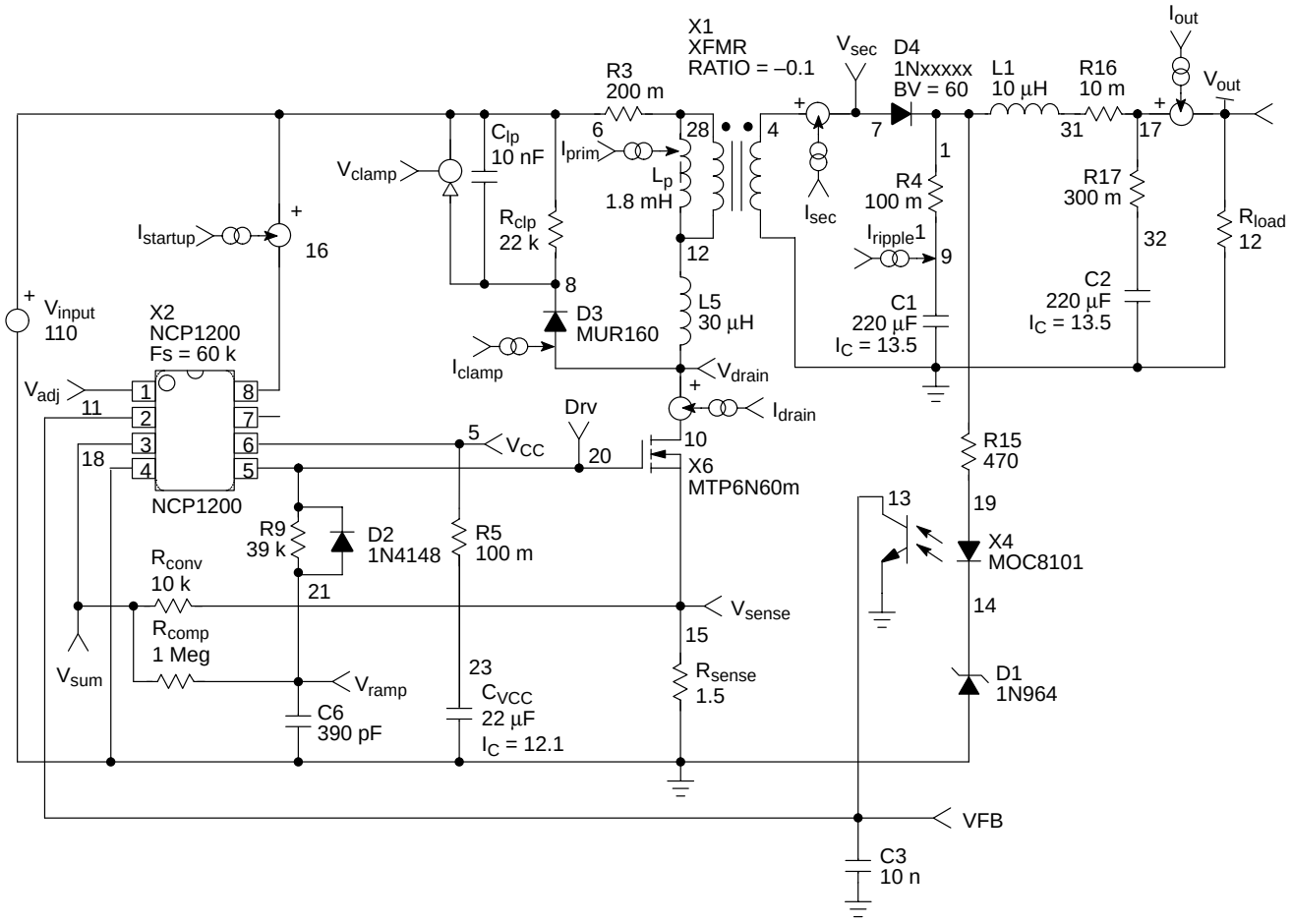

Figure 2a

The current–mode SMPS built with the NCP1200 SPICE model.

The system enters CCM for a load of 12 Ω and subharmonic oscillations take place, as shown by Figure 2b. Measurements on the board confirm the presence of these unwanted oscillations (Figure 2c). Rcomp was kept to a high value to suppress any compensating action.

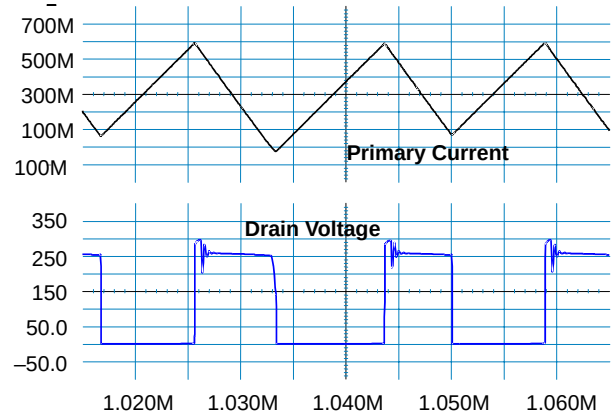

Figure 2b

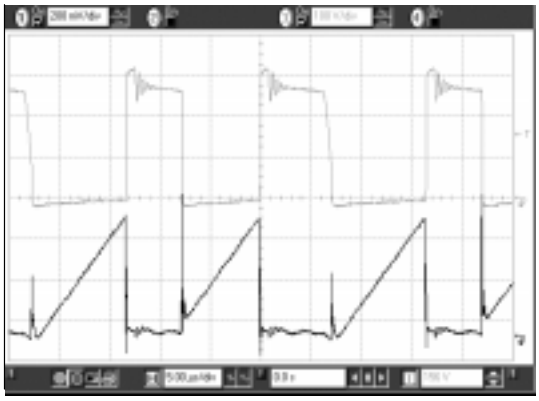

Figure 2c

Oscillations take place when entering CCM with a duty–cycle greater than 50% as confirmed by both models and measurements.

Let's now diminish Rcomp to 47 kΩ as previously calculated and run a new simulation. Results are depicted by Figure 2d and confirmed by Figure 2e:

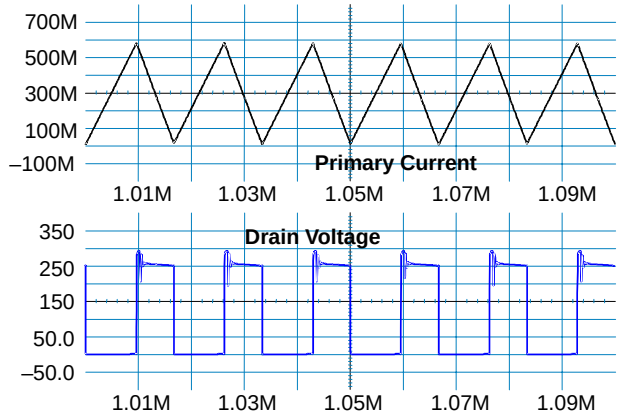

Figure 2d

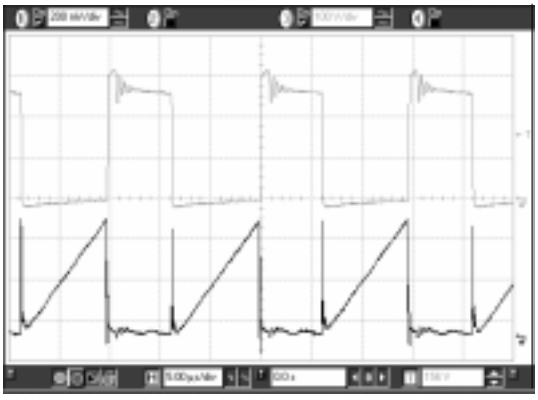

Figure 2e

The right amount of ramp compensation stabilizes the converter (2d simulated, 2c measured).

The previous default has disappeared and the converter is stabilized. However, the designer shall keep in mind that injecting a compensation ramp diminishes the current loop gain. This has the same effect as raising Rsense on the small–signal point of view. As a result, the controller grows its operating feedback voltage V_{FB} (that sets Ip) to impose the same peak current. If before compensation V_{FB} was already close to the maximum limit, the ramp injection will make it raise and the possibility exists that the NCP1200 goes into short–circuit protection ($V_{FB} \approx 4.1$ V).

We deliberately selected a rather high value for the ramp generator resistor in order to not load the NCP1200 (otherwise the standby power can be degraded). As a consequence, the summing resistor Rcomp cannot be too low to prevent from disturbing the ramp generator. In a noisy environment, the electrical paths conveying these signals to the NCP1200 pins shall be kept as short as possible to avoid undesirable peaking. In case of troubles, the solutions consists in lowering the ramp generator's output impedance and re–iterating the other elements.

References

1. R. B. RIDLEY, "A new small–signal model for current–mode control'', PhD. dissertation, Virginia Polytechnic Institute and State University, 1990 (e–mail : RRIDLEY@AOL.COM). This document can also be ordered from Ray Ridley's homepage: http://www.ridleyengineering.com/index.html
2. HOLLAND, "Modelling, Analysis and Compensation of the Current Mode Converter", Powercon 11, 1984 Record, Paper H–2.

Notes

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