Portable Power Management 300mA Dual LDO Regulator

General Description

The RT9054 is a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The range of output voltage is from 1.2V to 3.6V by operating from 2.5V to 5.5V input.

The RT9054 offers 3% accuracy, extremely low dropout voltage (240mV @ 300mA), and extremely low ground current, only 27μA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature and output short circuit protection.

The RT9054 is short circuit thermal folded back protected. The IC lowers its OTP trip point from 165°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) providing maximum safety to end users.

The RT9054 can operate stably with very small ceramic output capacitors, reducing required board space and component cost. The RT9054 is available in fixed output voltages in the WDFN-6L 1.6x1.6 packages.

Ordering Information

RT9054-□□□□

- Package Type
  QW : WDFN-6L 1.6x1.6 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Output Voltage : VOUT1/VOUT2
  VOUT2 > VOUT1 is Recommended

Note :

Richtek products are :

- RoHS compliant and compatible with the current require-
  ments of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Wide Operating Voltage Ranges : 2.5V to 5.5V**
- **Low-Noise for RF Application**
- **No Noise Bypass Capacitor Required**
- **Fast Response in Line/Load Transient**
- **TTL-Logic-Controlled Shutdown Input**
- **Low Temperature Coefficient**
- **Dual LDO Outputs (300mA/300mA)**
- **Ultra-low Quiescent Current 27μA/LDO**
- **High Output Accuracy 3%**
- **Short Circuit Protection**
- **Thermal Shutdown Protection**
- **Current Limit Protection**
- **Short Circuit Thermal Folded Back Protection**
- **Tiny 6-Lead WDFN Packages**
- **RoHS Compliant and Halogen Free**

Applications

- CDMA/GSM Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

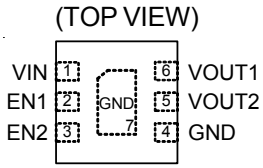
Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Available Voltage Version

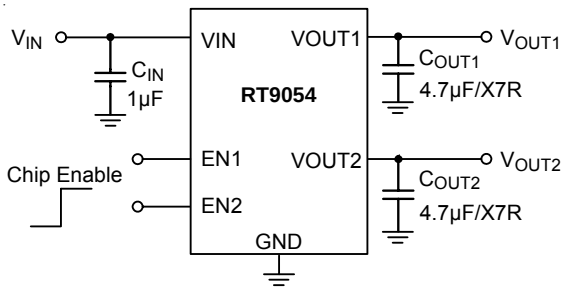
Code	Voltage	Code	Voltage	Code	Voltage
A	3.5	B	1.3	C	1.2
D	1.85	E	2.1	F	1.5
G	1.8	H	2	J	2.5
K	2.6	L	2.7	M	2.8
N	2.85	P	3	Q	3.1
R	3.2	S	3.3	T	2.65
V	2.9	W	1.6	X	3.15
Y	1.9	U	1.4		

Pin Configurations



WDFN-6L 1.6x1.6

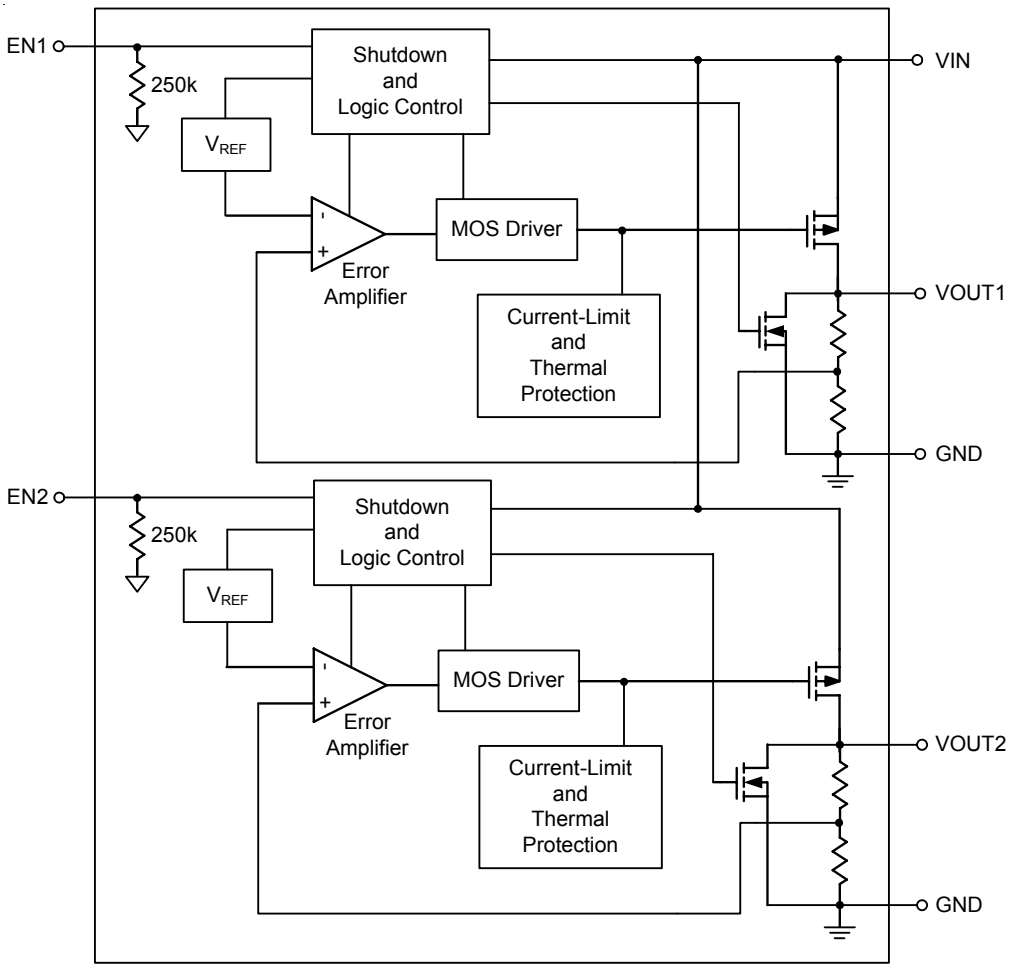
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Supply Input.
2	EN1	Chip Enable1.
3	EN2	Chip Enable2.
4, 7 (Exposed Pad)	GND	Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	VOUT2	Channel 2 Output Voltage.
6	VOUT1	Channel 1 Output Voltage.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 7V
- Other I/O Pin Voltages ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 1.6x1.6 ---------- 0.571W
- Package Thermal Resistance (Note 2) ----------
  WDFN-6L 1.6x1.6, θ_{JA} ---------- 175°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Enable Input Voltage ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUTx} + 1V, V_{ENx} = V_{IN}, C_{IN} = 1μF, C_{OUT} = 4.7μF, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Dropout Voltage (Note 5)		V_{DROP}	I_{OUTx} = 300mA	--	240	330	mV
Output Voltage Range		V_{OUTx}		1.2	--	3.6	V
V_{OUT} Accuracy		ΔV_{OUTx}	I_{OUTx} = 1mA to 300mA	–3	--	+3	%
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUTx} + 0.3V) to 5.5V or V_{IN} > 2.5V, whichever is larger	--	--	0.2	%/V
Load Regulation		ΔV_{LOAD}	1mA < I_{OUTx} < 300mA	--	--	0.6	%
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	330	450	700	mA
Quiescent Current		I_Q	V_{ENx} > 1.5V	--	58	80	μA
Shutdown Current		I_{Q_SD}	V_{ENx} < 0.4V	--	--	1	μA
Output Voltage TC				--	100	--	ppm/°C
EN Input Threshold Voltage	Logic High	V_{IH}	V_{IN} = 2.5V to 5.5V, Power On	1.5	--	--	V
	Logic Low	V_{IL}	V_{IN} = 2.5V to 5.5V, Shutdown	--	--	0.4	
EN Input Pull-Low Resistor				150	250	330	kΩ
V_{OUT} Discharge Resistance in Shutdown (Note 6)			V_{IN} = 5V, EN1 = EN2 = GND	--	3	--	kΩ
Thermal Shutdown		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	40	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PSRR V_{IN} = V_{OUT} + 1V, C_{OUT} = 4.7μF I_{LOAD} = 50mA	PSRR	f = 100Hz	--	70	--	dB
		f = 1kHz	--	70	--	
		f = 10kHz	--	70	--	
PSRR V_{IN} = V_{OUT} + 1V, C_{OUT} = 4.7μF I_{LOAD} = 50mA		f = 100kHz	--	54	--	dB
		f = 200kHz	--	45	--	
		f = 300kHz	--	38	--	
Output Voltage Noise		C_{OUT1} = C_{OUT2} = 10μF, 10Hz to 100kHz, I_{OUT1} = I_{OUT2} = 1mA	--	100	--	μV_{RMS}

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

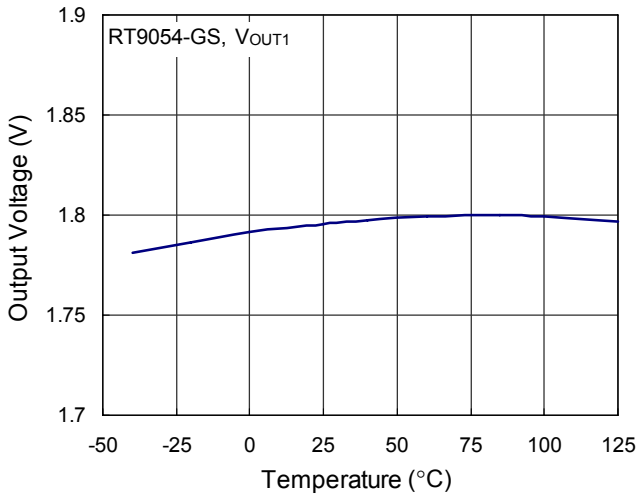
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ – 100mV.

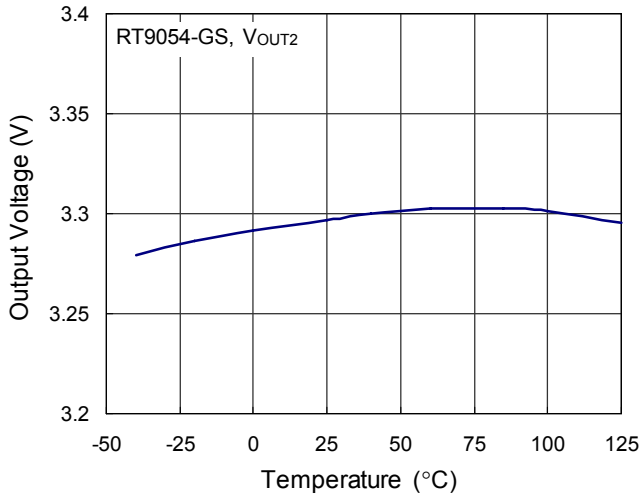
Note 6. It is guaranteed by design.

Typical Operating Characteristics

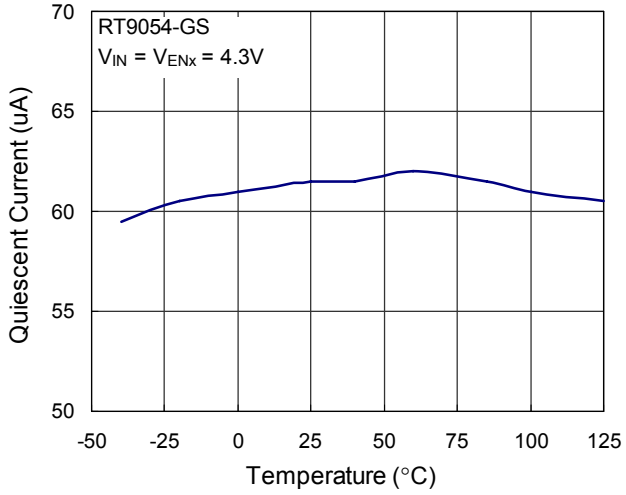
Output Voltage vs. Temperature



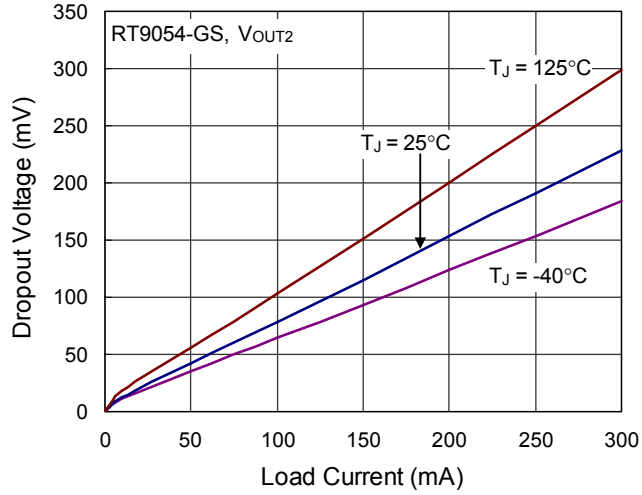
Output Voltage vs. Temperature



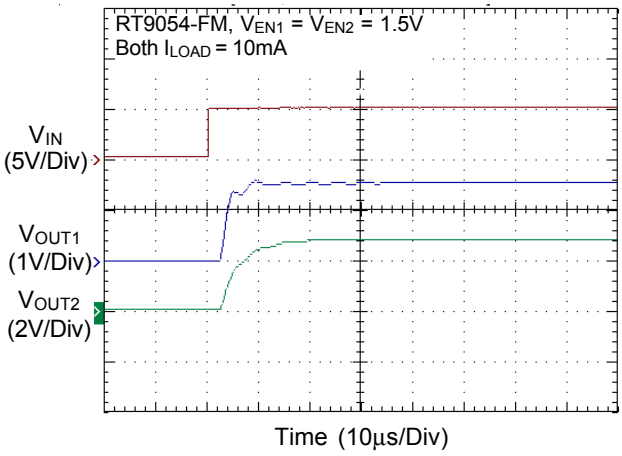
Quiescent Current vs. Temperature



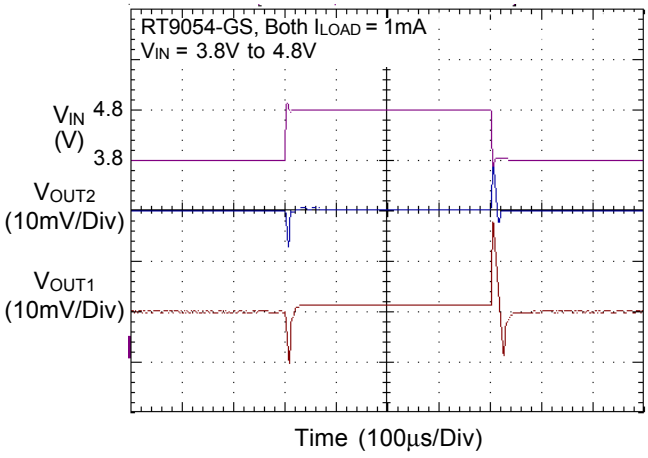
Dropout Voltage vs. Load Current



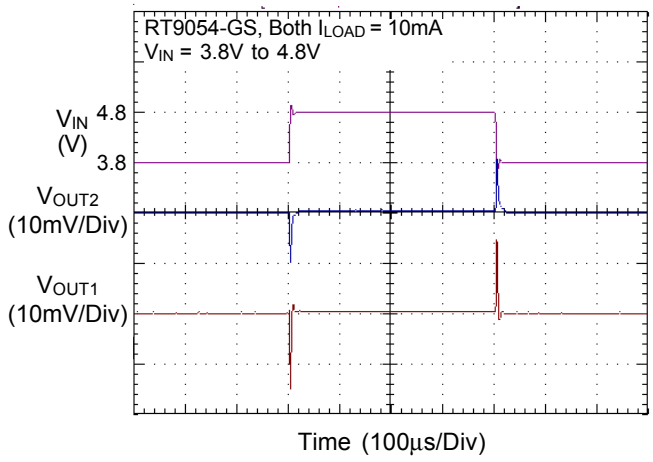
Power On from V_{IN}



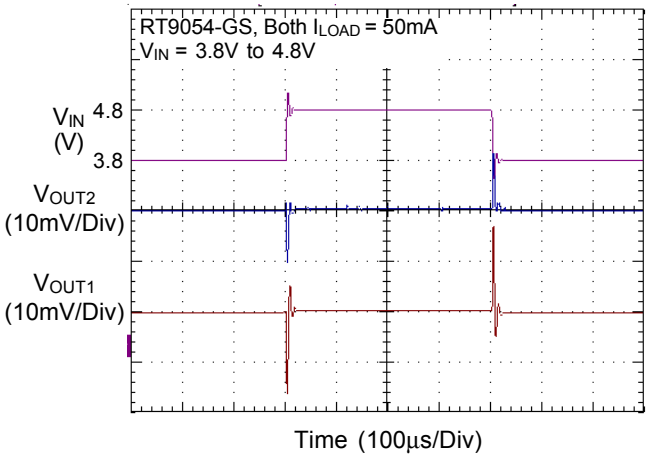
Line Transient Response



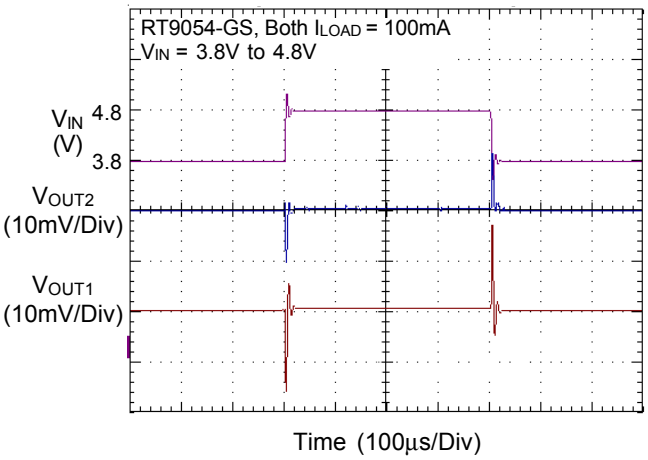
Line Transient Response



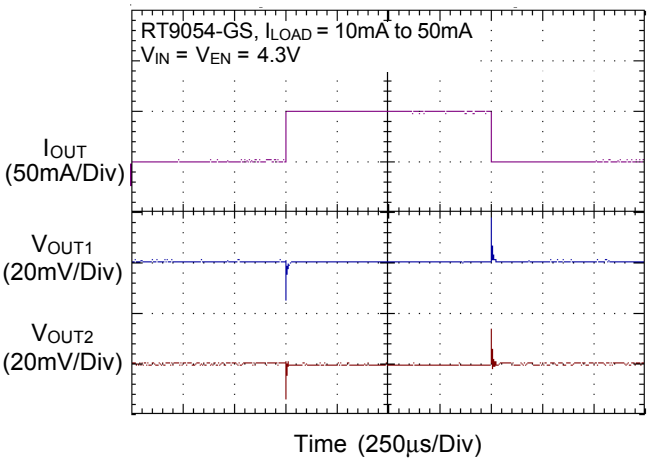
Line Transient Response



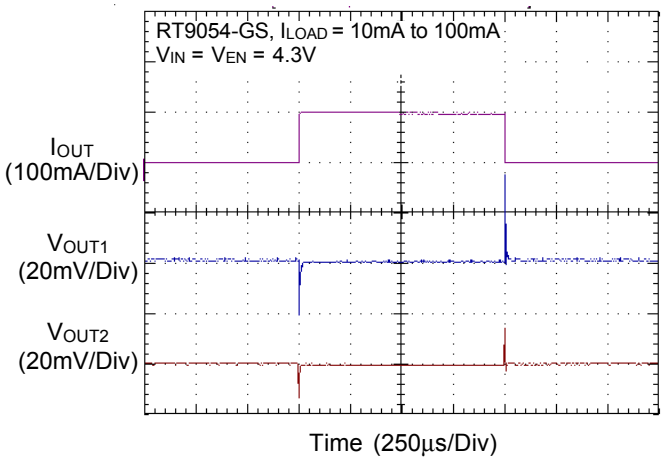
Line Transient Response



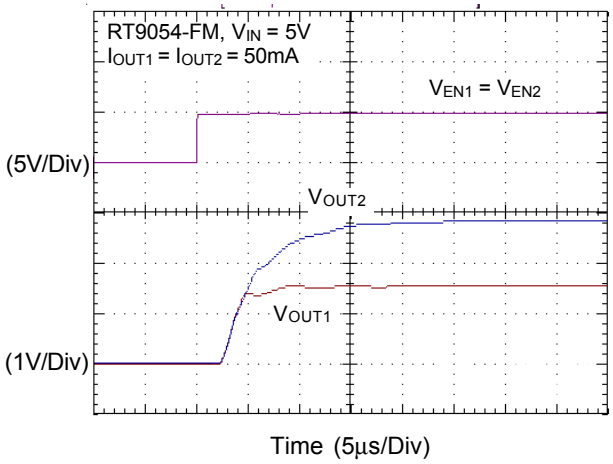
Load Transient Response



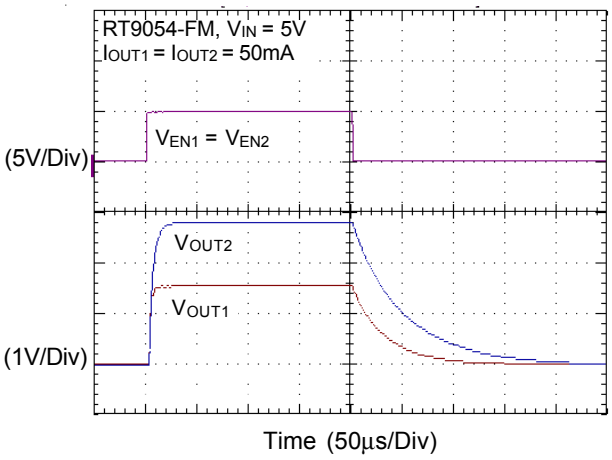
Load Transient Response



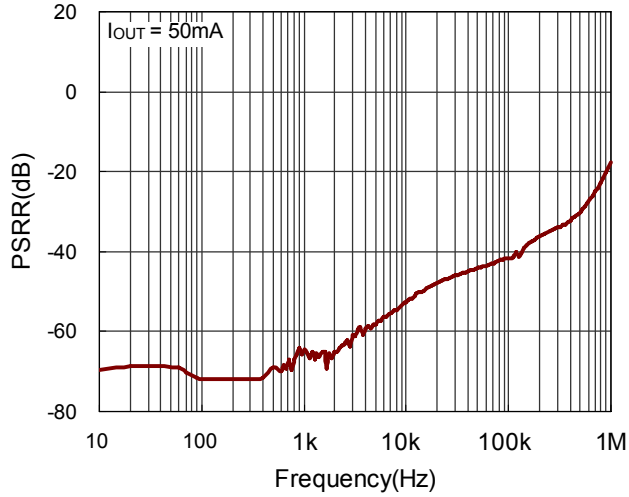
Power On from EN



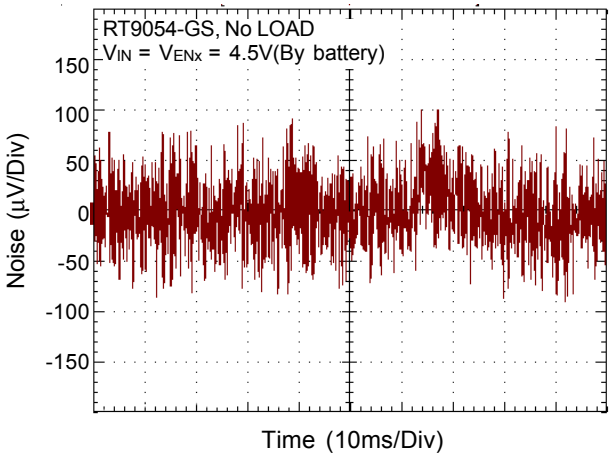
EN Pin Shutdown Response



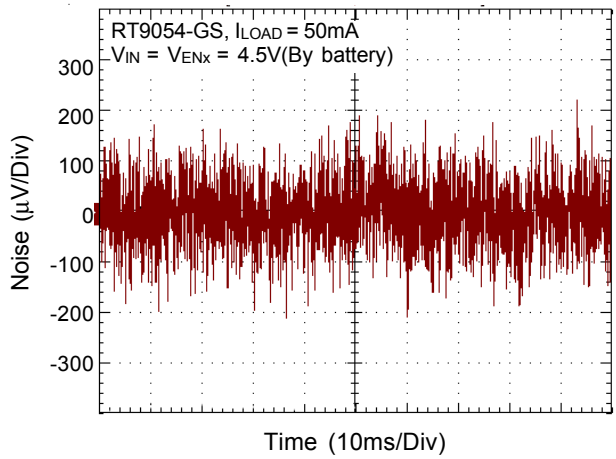
PSRR



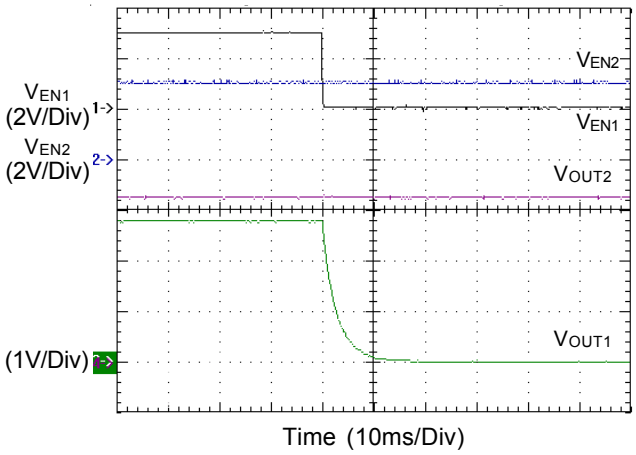
Noise



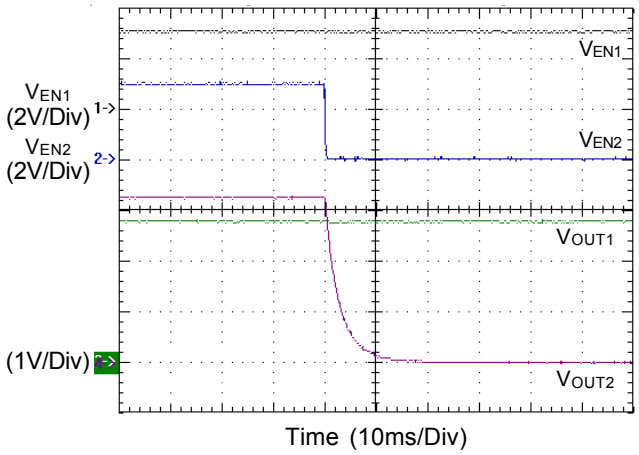
Noise



EN1 Pin Shutdown Response



EN2 Pin Shutdown Response



Application Information

Like any low-dropout regulator, the external capacitors used with the RT9054 must be carefully selected for regulator stability and performance. Using a capacitor value is >1μF on the RT9054 input, and the amount of capacitance can be increased without limit. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDO applications. The RT9054 is designed specifically to work with low ESR ceramic output capacitor under space-saving and performance consideration. Using a ceramic capacitor with value at least 4.7μF and ESR is > 20mΩ on the RT9054 output ensures stability. The RT9054 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9054 and returned to a clean analog ground.

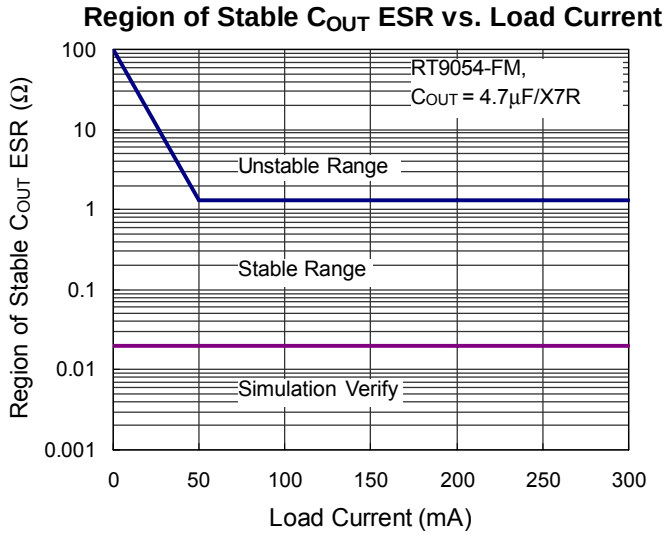


Figure 1. Stable Cout ESR Range

Thermal Considerations

Thermal protection limits power dissipation in RT9054. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools by 40°C. The RT9054 lowers its OTP trip level from 170°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) as shown in Figure 2. It limits the IC case temperature to under 100°C and provides maximum safety to customer while output short circuit occurs.

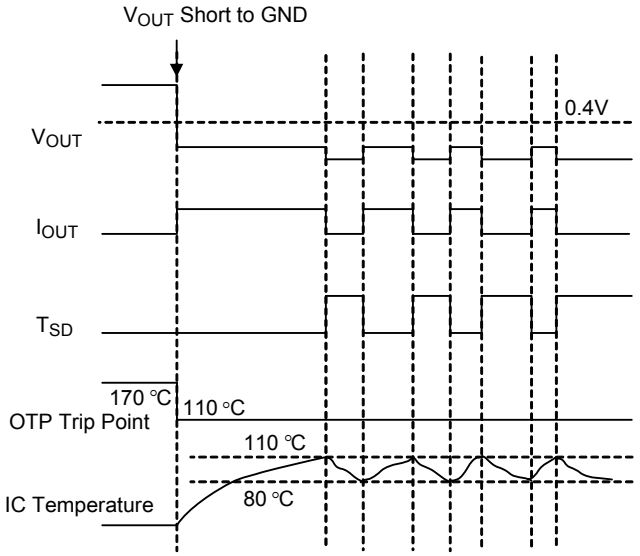


Figure 2. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the IC, the maximum junction temperature is 125°C. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for WDFN-8L 1.6x1.6 is 175°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (175°C/W) = 0.571W for WDFN-6L 1.6x1.6 packages

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For the IC packages, the Figure 3 of de-rating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

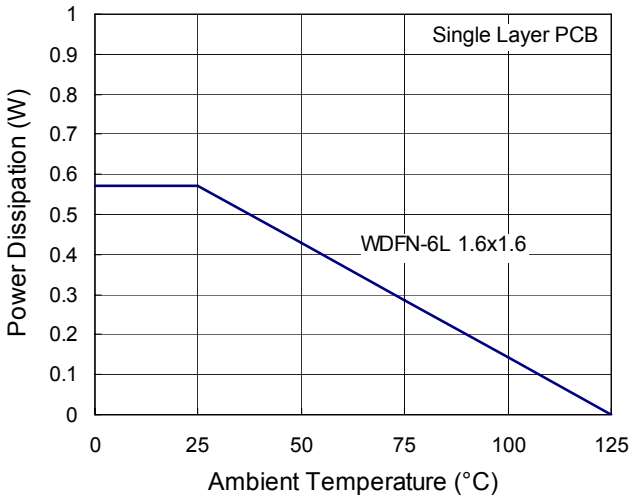
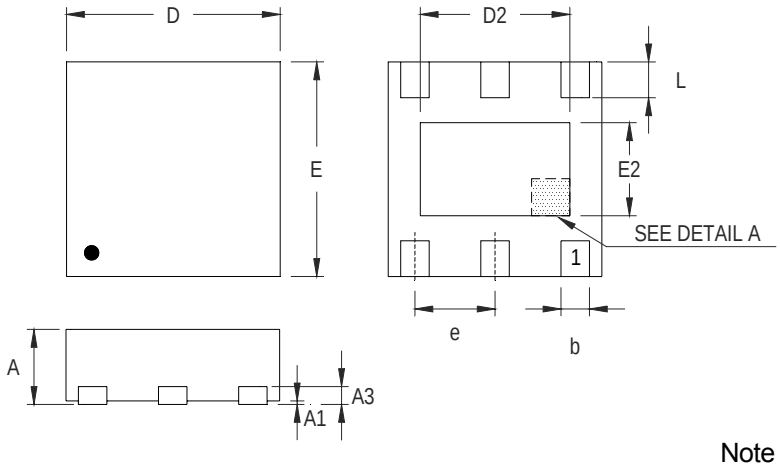
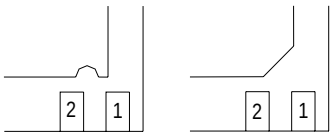


Figure 3. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.550	1.650	0.061	0.065
D2	0.950	1.050	0.037	0.041
E	1.550	1.650	0.061	0.065
E2	0.550	0.650	0.022	0.026
e	0.500		0.020	
L	0.190	0.290	0.007	0.011

W-Type 6L DFN 1.6x1.6 Package

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