Freescale Semiconductor
Data Sheet: Advance Information
An Energy Efficient Solution by Freescale

Document Number: MMA955xL
Rev. 1, 10/2011

Intelligent Motion-Sensing Platform

MMA955xL

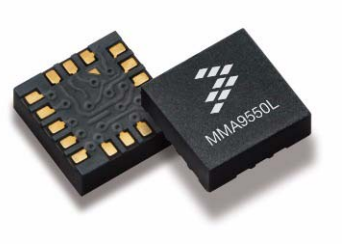
The MMA955xL device is a member of Freescale's Xtrinsic family of intelligent sensor platforms. This device incorporates dedicated accelerometer MEMS transducers, signal conditioning, data conversion, and a 32-bit programmable microcontroller.

This unique blend transforms Freescale's MMA955xL into an intelligent, high-precision, motion-sensing platform able to manage multiple sensor inputs. This device can make system-level decisions required for sophisticated applications such as gesture recognition, pedometer functionality, tilt compensation and calibration, and activity monitoring.

The MMA955xL device is programmed and configured with the CodeWarrior Development Studio for Microcontrollers software, version 10.1 or later. This standard integrated design environment enables customers to quickly implement custom algorithms and features to exactly match their application needs.

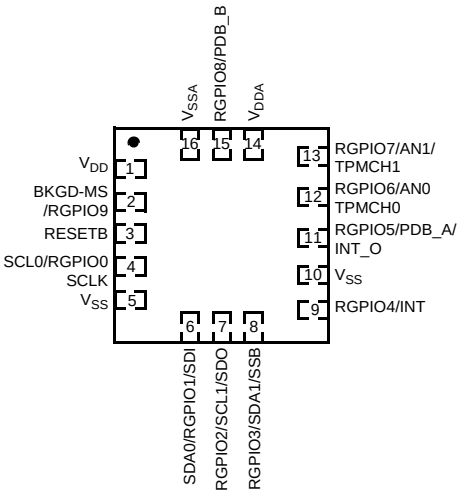
Using the master I^2C port, the MMA955xL device can manage secondary sensors, such as pressure sensors, magnetometers, or gyroscopes. This allows sensor initialization, calibration, data compensation, and computation functions to be off-loaded from the system application processor. The MMA955xL device also acts as an intelligent sensing hub and a highly configurable decision engine. Total system power consumption is significantly reduced because the application processor stays powered down until absolutely needed.

Top and bottom view



16-pin LGA
3 mm x 3 mm x 1 mm
Case 2094-01

Top view



Pin connections

Hardware Features

- Three accelerometer operating ranges:
  - ±2g suits most hand gestures (orientation detection and tit control) and freefall. For tap detection, ±4g and ±8g are supported.
  - ±4g covers most regular human dynamics (walking and jogging)
  - ±8g detects most abrupt activities (gaming)
- Integrated temperature sensor
- One slave SPI or I^2C interface operating at up to 2 Mbps, dedicated to communication with host processor. Default value of the I^2C, 7-bit address is 0x4C. (This can be customized by firmware.)
- One master I^2C interface operating at up to 400 kbps that can be used to communicate with external sensors
- Eight selectable output data rates (ODR), from 488 Hz to 3.8 Hz
- 10, 12, 14, and 16-bit trimmed ADC data formats available
- 1.8V supply voltage
- 32-bit ColdFire V1 CPU with MAC unit
- Extensive set of power-management features and low-power modes
- Integrated ADC can be used to convert external analog signals
- Single-Wire, Background-Debug Mode (BDM) pin interface
- 16-KB flash memory
- 2-KB Random Access Memory
- ROM-based flash controller and slave-port, command-line interpreter
- Two-channel timer with input capture, output capture, or edge-aligned PWM
- Programmable delay block for scheduling events relative to start of frame
- A 16-bit, modulo timer for scheduling periodic events
- Minimal external component requirements
- RoHS compliant (-40 to +85ºC), 16-pin, 3 x 3 x 1-mm LGA package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Software Features

This device can be programmed to provide any of the following:

- Orientation detection (portrait/landscape)
- High-g/Low-g threshold detection
- Pulse detection (single, double and directional tap)
- Tilt detection
- Auto wake/sleep
- Embedded, smart FIFO
- Power management
- Pedometer

A selection of the software features are included in the factory-programmed firmware for some devices. Users may add their own features with user firmware.The power and flexibility of the embedded ColdFire V1 MCU core has new and unprecedented capabilities.

Table 1. Ordering information

Part number	Firmware	Temperature range	Package description	Shipping
MMA9550LT	Motion	-40°C to +85°C	LGA-16	Tray
MMA9550LR1	Motion	-40°C to +85°C	LGA-16	Tape and reel
MMA9551LT	Gesture	-40°C to +85°C	LGA-16	Tray
MMA9551LR1	Gesture	-40°C to +85°C	LGA-16	Tape and reel
MMA9553LR1	Pedometer	-40°C to +85°C	LGA-16	Tape and reel
MMA 9559LR1	Foundation	-40°C to +85°C	LGA-16	Tape and reel

Contents

Related Documentation

The MMA955xL device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA955xL.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Variations of MMA955xL Device

Freescale offers a variety of firmware versions for the MMA955xL devices. The different versions of the device are identified by the fourth digit in the part number (for example MMA955**9**). Information and specifications provided in this data sheet are independent of the Freescale firmware versions.

The following table lists some of the variations among the MMA955xL-platform devices.

Table 2. Features of product-line devices

Feature - Device	MMA9550L	MMA9551L	MMA9553	MMA9559L
Key elements	Motion sensing	Gesture sensing	Pedometer	High flexibility
User flash available	6.5 KB	4.5 KB	1.5K	14 KB
User RAM available	576 bytes	452 bytes	200 bytes	1664 bytes
Digital resolution (bits)	10,12,14,16 bits	10,12,14,16 bits	10,12,14,16 bits	10,12,14,16 bits
G measurement ranges	2g, 4g, 8g	2g, 4g, 8g	2g, 4g, 8g	2g, 4g, 8g
Real-time and preemptive scheduling	Yes	Yes	Yes	No
Event management	No	No	No	Yes
Slave Port Command Interpreter				
• Normal mode	Yes	Yes	Yes	No
• Legacy mode	Yes	Yes	Yes	No
• Streaming mode	Yes	Yes	Yes	No
Front-end processing				
• 100-Hz BW anti-aliasing	Yes	Yes	Yes	No
• 50-Hz BW anti-aliasing	Yes	Yes	Yes	No
• g-mode-dependent resolution	Yes	Yes	Yes	Yes
• Absolute value	Yes	Yes	Yes	No
• Low-pass filter	Yes	Yes	Yes	No
• High-pass filter	Yes	Yes	Yes	No
• Data-ready interrupt	Yes	Yes	Yes	Yes
Gesture applications				
• High g/Low g	No	Yes	No	No
• Tilt	No	Yes	No	No
• Portrait/Landscape	No	Yes	No	No
• Programmable orientation	No	Yes	No	No
• Tap/Double-tap	No	Yes	No	No
• Freefall	No	Yes	No	No
• Motion	No	Yes	No	No

Table 2. Features of product-line devices (Continued)

Feature - Device	MMA9550L	MMA9551L	MMA9553	MMA9559L
Data-storage modules				
• Data FIFO	Yes	Yes	Yes	No
• Event queue	Yes	Yes	Yes	No
• Inter-process FIFO	No	No	No	Yes
Power-control module				
• Run and Stop on idle	Yes	Yes	Yes	Yes
• Run and No stop	Yes	Yes	Yes	Yes
• Stop NC	Yes	Yes	Yes	Yes
• Auto-Wake / Auto-Sleep / Doze	Yes	Yes	Yes	No
Data-management daemons	Yes	Yes		Yes
Pedometer applications				
• Step count	No	No	Yes	No
• Distance	No	No	Yes	No
• Adaptive distance	No	No	Yes	No
• Activity monitor	No	No	Yes	No

The only difference between the various device configurations is the firmware content that is loaded into the flash memory at the factory. The user still can add custom software using the remaining portion of flash memory.

The MMA9550, MMA95501, and MMA95503 devices can function immediately as they are. They have an internal command interpreter and applications scheduler and can interact directly with the users' host system.

The MMA9559 device provides the most flexibility and is for users who need to design their own control loop and system. The device needs to be programmed with custom user code.

2 Typical Applications

This low-power, intelligent sensor platform is optimized for use in portable and mobile consumer products such as:

- Mobile phones/PMP/PDA/digital cameras
  - Orientation detection (portrait/landscape)
  - Image stability
  - Tilt control enabled with higher resolution
  - Gesture recognition
  - Tap to control
  - Auto wake/sleep for low power consumption
- Smartbooks/ereaders/netbooks/laptops
  - Anti-theft
  - Freefall detection for hard-disk drives
  - Orientation detection
  - Tap detection
- Pedometers
- Gaming and toys
- Activity monitoring in medical applications
- Security
  - Anti-theft
  - Shock detection
  - Tilt
- Fleet monitoring, tracking
  - Dead reckoning
  - System auto-wake on movement
  - Detection
  - Shock recording
  - Anti-theft
- Power tools and small appliances
  - Tilt
  - Safety shut-off

3 General Description

3.1 Functional Overview

The MMA955xL device consists of a 3-axis, MEMS accelerometer and a mixed-signal ASIC with an integrated, 32-bit CPU. The mixed-signal ASIC can be utilized to measure and condition the outputs of the MEMS accelerometer, internal temperature sensor, or a differential analog signal from an external device.

These measured values can be read via the slave I^2C or SPI port or utilized internally within the MMA955xL platform.

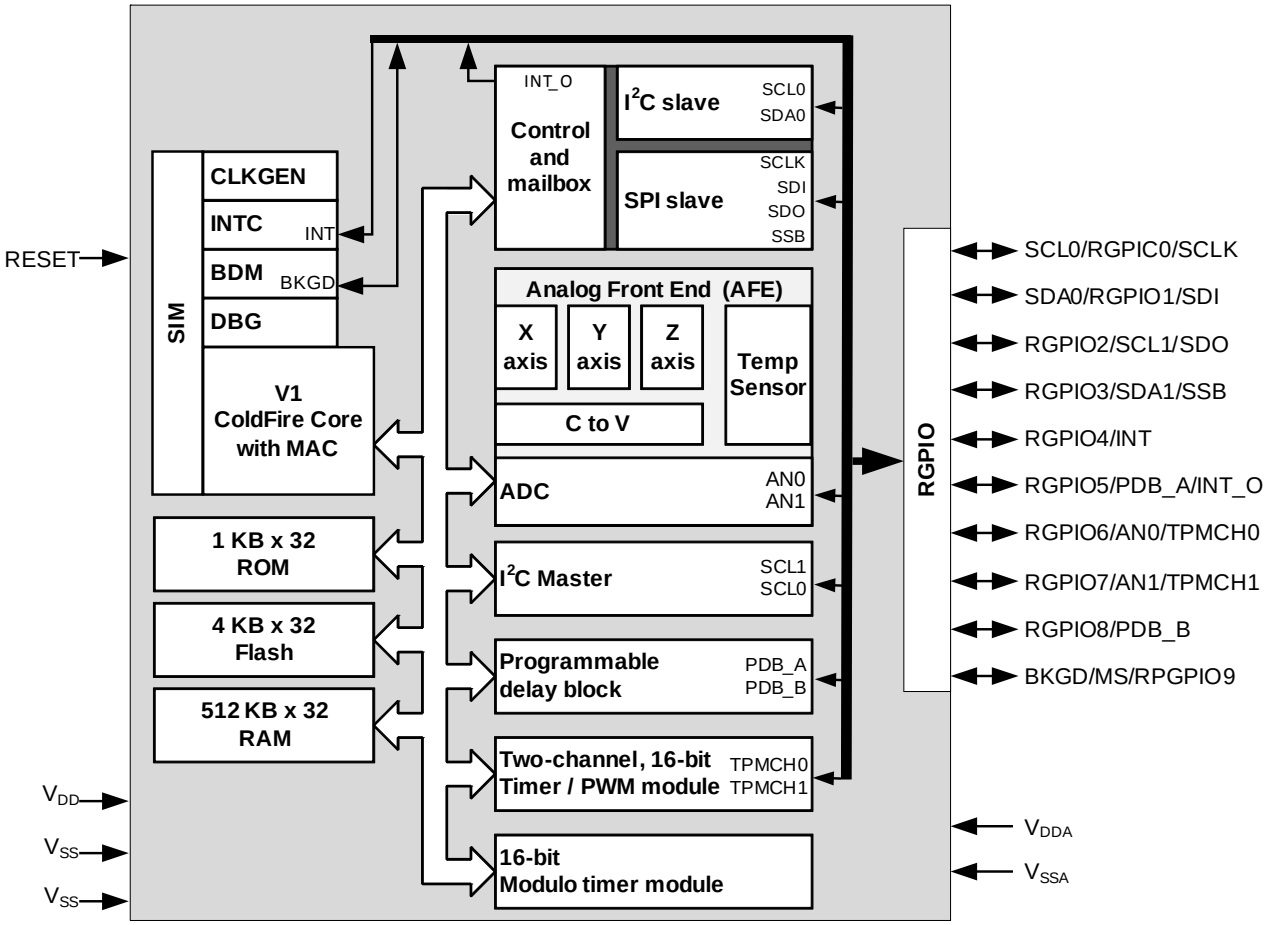


Figure 1. Platform block diagram(1)

1. Preliminary data for memory sizes.

A block level view of is shown in the preceding figure and can be summarized at a high level as an analog/mixed-mode subsystem associated with a digital engine:

- The analog sub-system is composed of:
  - A 3-axis transducer that is an entirely passive block including the MEMS structures.
  - An Analog Front End (AFE) with the following:
    - A capacitance-to-voltage converter (C to V)
    - An analog-to-digital converter
    - A temperature sensor
- The digital sub-system is composed of:
  - The 32-bit, ColdFire V1 CPU with a Background-Debug Module (BDM)
  - Memory: RAM, ROM, and flash
  - Rapid GPIO (RGPIO) port-control logic
  - Timer functions include:
    - Modulo timer module (MTIM16)
    - Programmable Delay Timer (PDB)

- General-Purpose Timer/PWM Module (TPM)

– I^2C master interface
– I^2C or SPI slave interface
– System Integration Module (SIM)
– Clock-Generation Module

The slave interfaces (either SPI or I^2C) operate independently of the CPU subsystem. They can be accessed at any time, including while the device is in low-power, deep-sleep mode.

3.2 Packaging Information

The package pinout definition for this device is designed as a super set of functions found typically on Freescale's ColdFire V1 CPU offering, as well as other competitive devices. All pins on the device are utilized and many are multiplexed.

The following sections describe the pinout. Users can select from multiple pin functions via the SIM pin, mux-control registers.

3.2.1 Package diagrams

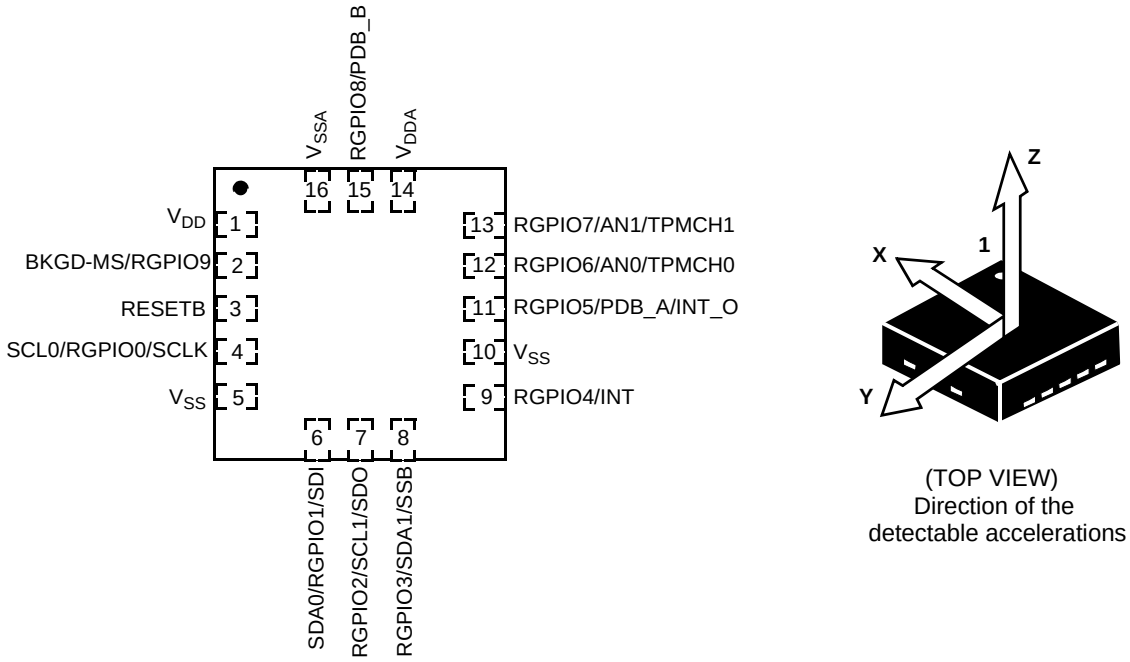


Figure 2. Device pinout (top view) and package frame convention

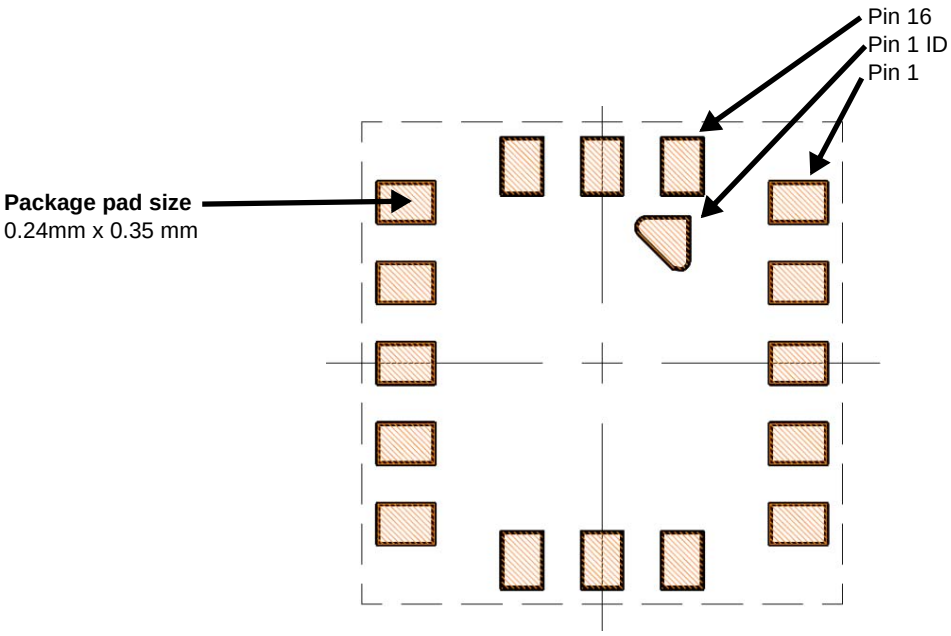


Figure 3. Package bottom view

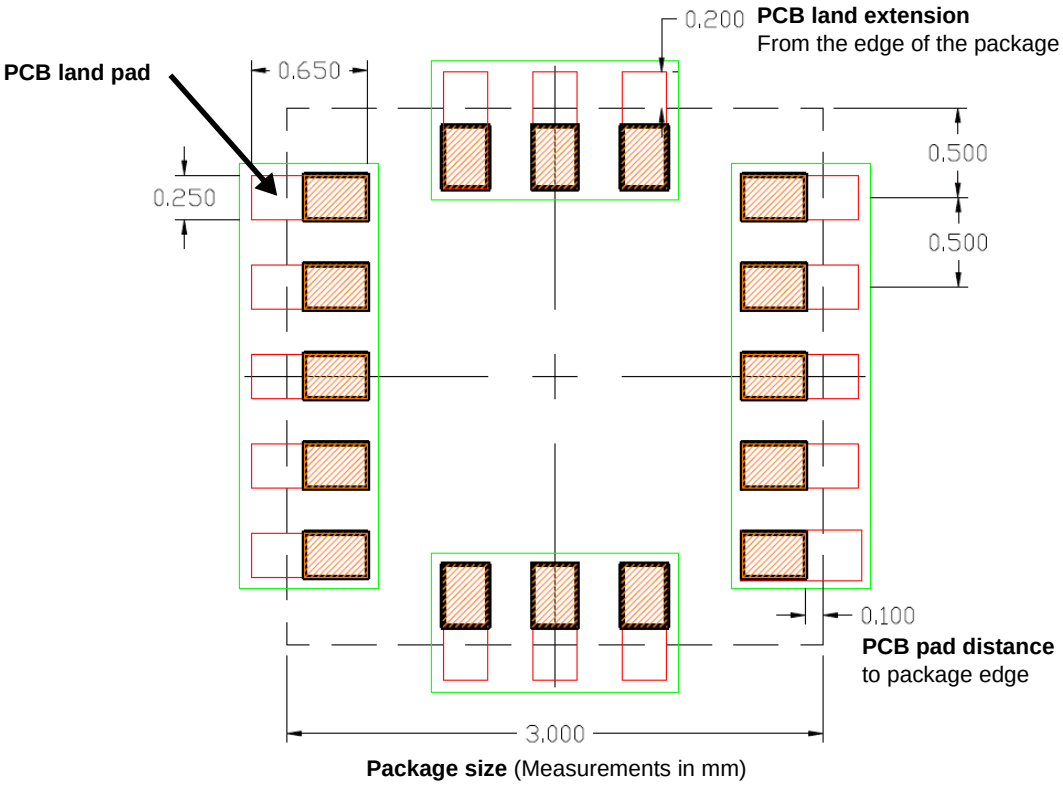


Figure 4. Package overlaid on PCB footprint diagram (top view)

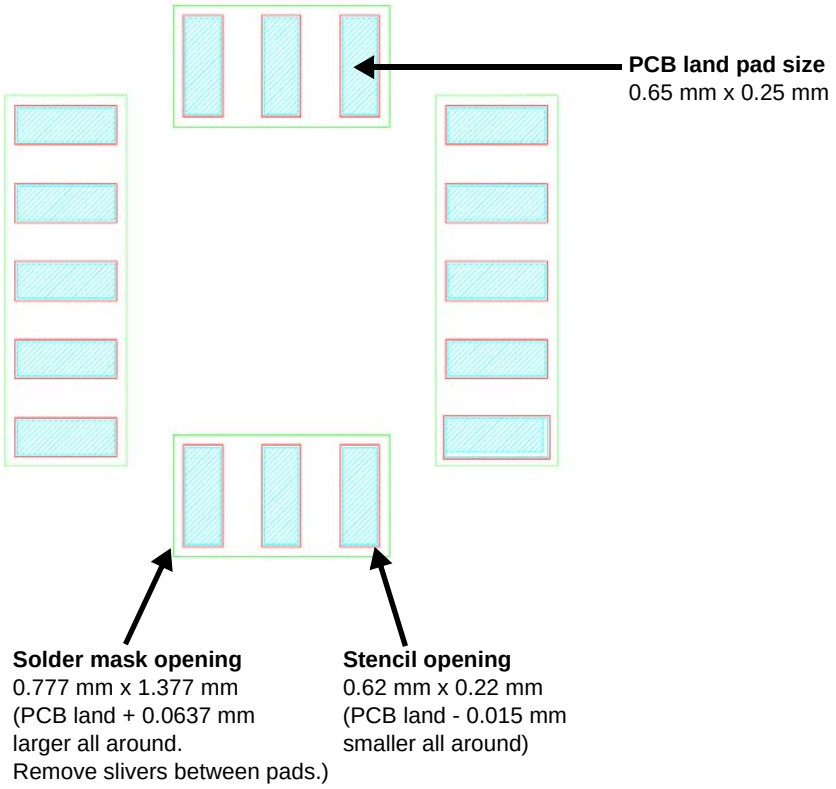


Figure 5. Recommended PCB footprint

3.2.2 Sensing Direction and Output Response

The following figure shows the device's default sensing direction when measuring gravity in a static manner. Also included are the standard abbreviations or names for the six different orientation modes: portrait up/down, landscape left/right and back/front.

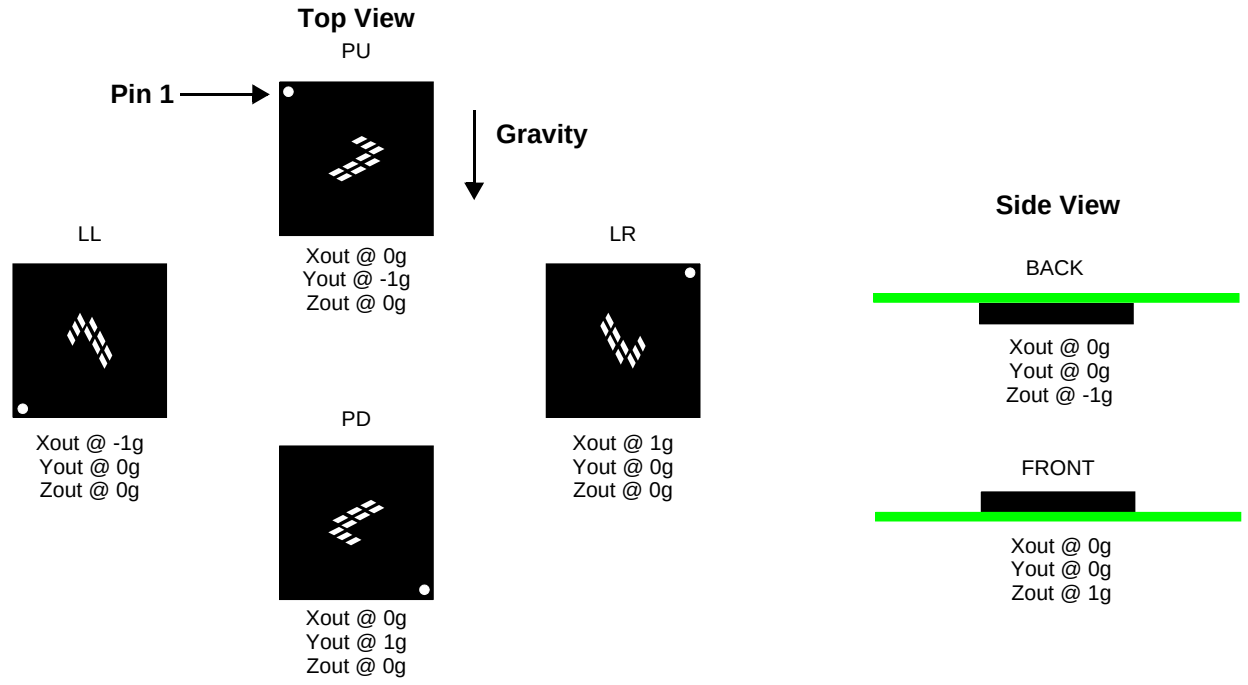


Figure 6. Sensing direction and output response

3.2.3 Pin Functions

The following table summarizes functional options for each pin on this device.

Table 3. Pin functions

Pin #	Pin Function #1[1]	Pin Function #2	Pin Function #3	Description
1	V_{DD}			Digital power supply
2	BKGD/MS	RGPIO9		Background-debug / Mode select / RGPIO9
3	RESETB[2]			Active-low reset
4	SCL0	RGPIO0	SCLK	Serial clock for slave I^2C / RGPIO0 / Serial clock for slave SPI
5	V_{SS}			Digital ground
6	SDA0	RGPIO1	SDI	Serial data for slave I^2C / RGPIO1 / SPI serial data input
7	RGPIO2	SCL1	SDO	RGPIO2 / Serial clock for master I^2C / SPI serial data output
8[3]	RGPIO3	SDA1	SSB	RGPIO3 / Serial data for master I^2C / SPI slave select
9	RGPIO4	INT		RGPIO4 / Interrupt input
10	RESERVED (Connect to V_{SS})			(Must be grounded externally.)
11	RGPIO5	PDB_A	INT_O	RGPIO5 / PDB_A / INT_O slave-port interrupt output
12	RGPIO6	AN0	TPMCH0	RGPIO6 / ADC Input 0 / TPM Channel 0
13	RGPIO7	AN1	TPMCH1	RGPIO7 / ADC Input 1 / TPM Channel 1
14	V_{DDA}			Analog power
15	RGPIO8	PDB_B		RGPIO8 / PDB_B
16	V_{SSA}			Analog ground

1. Pin function #1 represents the reset state of the hardware. Pin functions can be changed via the SIM pin, mux-control registers in Freescale or user firmware.
2. RESETB is an open-drain, bidirectional pin. Reset must be pulled high at startup. After startup, Reset may be asserted to reset the device.
3. RGPIO3/SDA1/SSB = Low at startup selects SPI. High at startup selects I^2C. This is a function of the application boot code, not of the hardware.

3.3 Pin Function Descriptions

This section provides a brief description of the various pin functions available on the MMA955xL platform. Ten of the device pins are multiplexed with Rapid GPIO (RGPIO) functions. The “Pin Function #1” column in Table 3 on page 11 lists which function is active when the hardware exits the reset state. Freescale or user firmware can use the pin mux-control registers in the System Integration Module (SIM) to change pin assignments for each pin after reset. For detailed information about these registers, see the *MMA955xL Three-Axis Accelerometer Reference Manual* (MMA955xLRM).

V_{DD} and V_{SS}: Digital power and ground. V_{DD} is nominally 1.8V.

V_{DDA} and V_{SSA}: Analog power and ground. V_{DDA} is nominally 1.8V. To optimize performance, the V_{DDA} line can be filtered to remove any digital noise that can be present on the 1.8V supply. (See Figure 5 and Figure 6 on page 17.)

RESETB: The RESETB pin is an open-drain, bidirectional pin with an internal, weak, pullup resistor. At start up, it is configured as an input pin, but also can be programmed to become bidirectional. Using this feature, the MMA955xL device can reset external devices for any purpose other than power-on reset. Reset must be pulled high at startup. After startup, Reset may be asserted to reset the device. The total external capacitance to ground has to be limited when using RESETB-pin, output-drive capability. For more details, see the “System Integration Module” chapter of the *MMA955xL Three-Axis Accelerometer Reference Manual* (MMA955xLRM).

Slave I^2C port: SDA0 and SCL0: These are the slave-I^2C data and clock signals, respectively. The MMA955xL device can be controlled via the serial port or via the slave SPI interface.

Master I^2C: SDA1 and SCL1: These are the master-I^2C clock and data signals, respectively.

Analog-to-Digital Conversion: AN0, AN1: The on-chip ADC can be used to perform a differential, analog-to-digital conversion based on the voltage present across pins AN0(-) and AN1(+). Conversions for these pins are at the same Output Data Rate (ODR) as the MEMS transducer signals. Input levels are limited to 1.8V differential.

Rapid General Purpose I/O: RGPIO[9:0]: The ColdFire V1 CPU has a feature called Rapid GPIO (RGPIO). This is a 16-bit, input/output port with single-cycle write, set, clear, and toggle functions available to the CPU. The MMA955xL device brings out the lower 10 bits of that port as pins of the device.

Interrupts: INT: This input pin can be used to wake the CPU from a deep-sleep mode. It can be programmed to trigger on either rising or falling edge, or high or low level. This pin operates as a Level-7 (high-priority) interrupt.

Debug/Mode Control: BKGD/MS: At start up, this pin operates as mode select. If this pin is pulled high during start up, the CPU will boot normally and run code. If this pin is pulled low during start up, the CPU will boot into active Background-Debug Mode (BDM). In BDM, this pin operates as a bidirectional, single-wire, background-debug port. It can be used by development tools for downloading code into on-chip RAM and flash and to debug that code.

Timer: PDB_A and PDB_B: These are the two outputs of the programmable delay block.

Slave SPI Interface: SCLK, SDI, SDO and SSB: These pins control the slave SPI clock, data in, data out, and slave-select signals, respectively. The MMA955xL platform can be controlled via this serial port or via the slave-I^2C interface. SBB has a special function at startup that selects the Slave interface mode. Low at startup selects SPI and high selects I^2C.

INT_O: The slave-port output interrupt pin. This pin can be used to flag the host when a response to a command is available to read on the slave port.

TPMCH0 and TPMCH1: The I/O pin associated with 16-bit, TPM channel 0 and 1.

3.4 System Connections

3.4.1 Power Sequencing

An internal circuit powered by V_{DDA} provides the device with a power-on-reset signal. In order for this signal to be properly recognized, it is important that V_{DD} is powered up before or simultaneously with V_{DDA}. The voltage potential between V_{DD} and V_{DDA} must not be allowed to exceed the value specified in Table 7 on page 17.

3.4.2 Layout Recommendations

- Provide a low-impedance path from the board power supply to each power pin (V_{DD} and V_{DDA}) on the device and from the board ground to each ground pin (V_{SS} and V_{SSA}).
- Place 0.01 to 0.1-µF capacitors as close as possible to the package supply pins to meet he minimum bypass requirement. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs. V_{DDA}/V_{SSA}. ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed-circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the power and ground with a capacitor of approximately 1 µF and a number of 0.1-µF ceramic capacitors.

- Minimize PCB trace lengths for high-frequency signals. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{DDA} and V_{SSA} pins.
- Use separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA}. Connect the separate analog and digital power and ground planes as close as possible to power supply outputs. If both analog circuit and digital circuits are powered by the same power supply, it is advisable to connect a small inductor or ferrite bead in series with both the V_{DDA} and V_{SSA} traces.
- Physically separate the analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. It is also desirable to place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Provide an interface to the BKGD/MS pin if in-circuit debug capability is desired.
- Ensure that resistors R_{P1} and R_{P2}, in the following figure, match the requirements stated in the I^2C standard. For the shown configuration, the value of 4.7 kΩ would be appropriate.

3.4.3 MMA955xL Platform as an Intelligent Slave

I^2C pullup resistors, a ferrite bead, and a few bypass capacitors are all that are required to attach this device to a host platform. The basic configurations are shown in the following two figures. In addition, the RGPIO pins can be programmed to generate interrupts to a host platform in response to the occurrence of real-time application events. In this case, the pins should be routed to the external interrupt pins of the CPU.

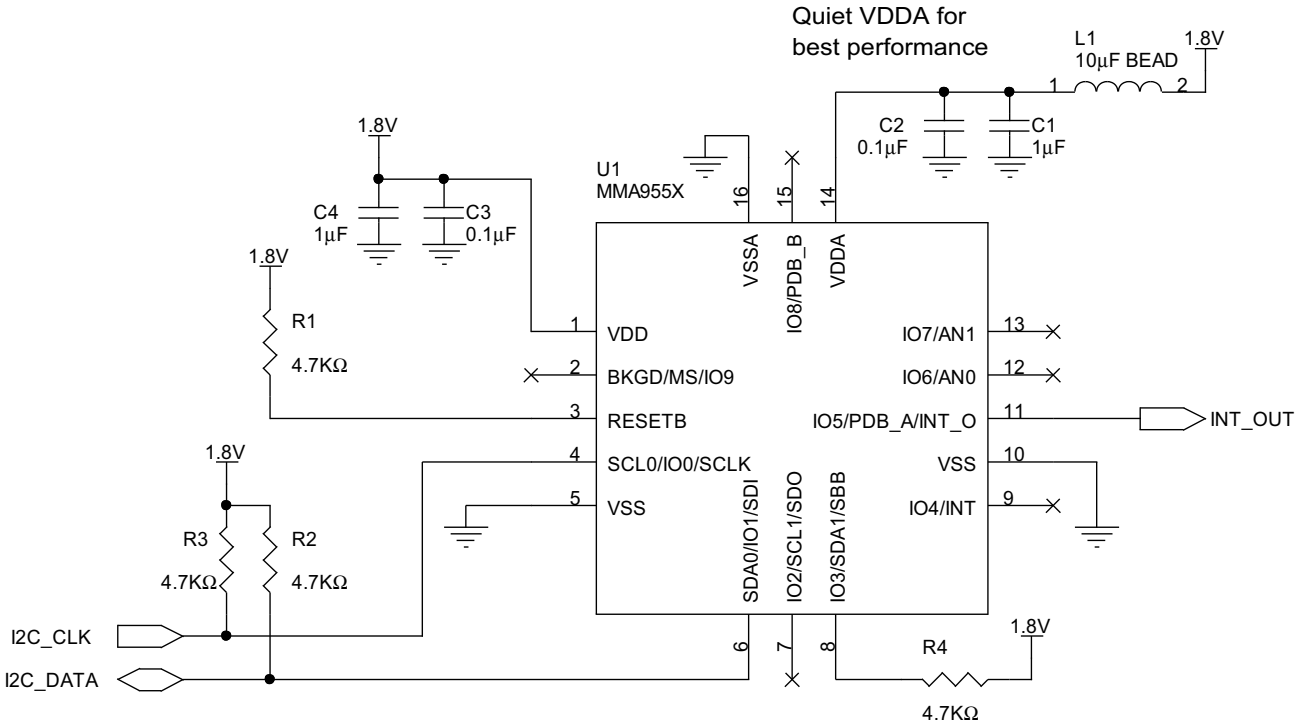


Figure 7. Platform as an I^2C slave

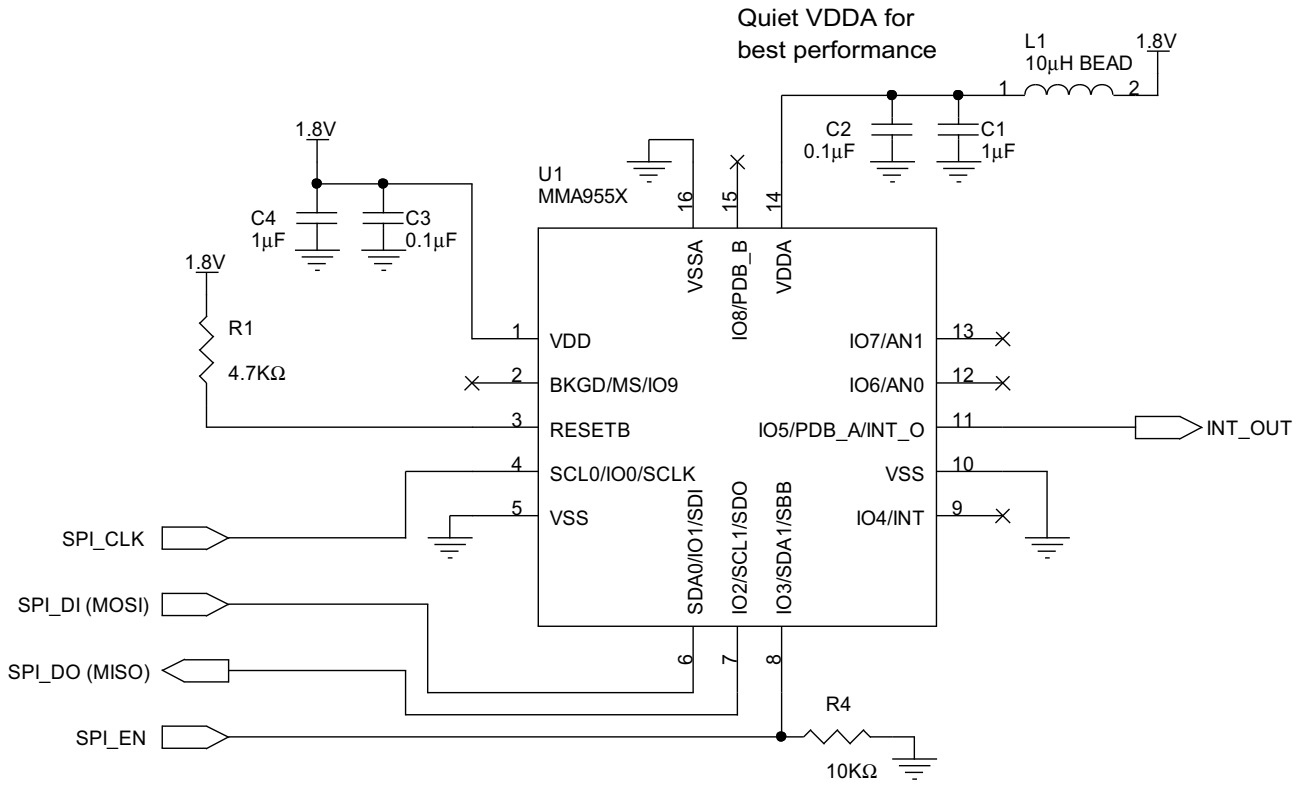


Figure 8. Platform as an SPI slave

3.4.4 MMA955xL Platform as a Sensor Hub

The MMA955xL device includes a powerful, 32-bit ColdFire V1 CPU; a second, I^2C bus; and one, external analog input. These features can all be monitored using the on-chip ADC.

The combination of low power consumption and powerful features mean that the MMA955xL platform can effectively operate as a power controller for handheld units such as cell phones, PDAs, and games. The host platform can put itself to sleep with confidence that the MMA955xL device will issue a wake request should any external event require its attention.

The following figure illustrates the MMA955xL device being used in this configuration. Observe how all that is required is a few bypass capacitors, a ferrite bead, and some pullup resistors for the I^2C buses.

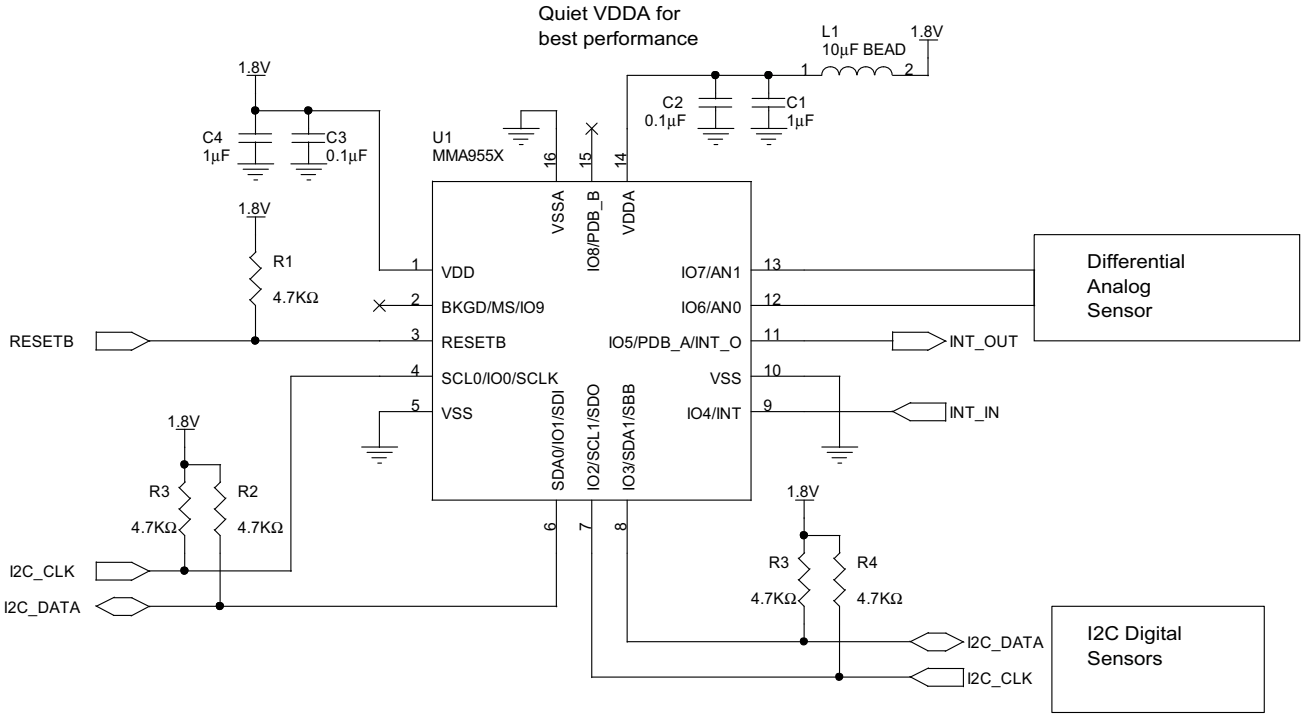


Figure 9. Platform as sensor hub

4 Mechanical and Electrical Specifications

This section contains electrical specification tables and reference timing diagrams for the MMA955xL device, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

4.1 Definitions

Cross-axis sensitivity	The proportionality constant that relates a variation of accelerometer output to cross acceleration. This sensitivity varies with the direction of cross acceleration and is primarily due to misalignment.
Full range	The algebraic difference between the upper and lower values of the input range. Refer to the input/output characteristics.
Hardware compensated	Sensor modules on this device include hardware-correction factors for gain and offset errors that are calibrated during factory test using a least-squares fit of the raw sensor data.
Linearity error	The deviation of the sensor output from a least-squares linear fit of the input/output data.
Nonlinearity	The systematic deviation from the straight line that defines the nominal input/output relationship.
Pin group	the clustering of device pins into a number of logical pin groupings to simplify and standardize electrical data sheet parameters. Pin groups are defined in Section 4.2, “Pin Groups”.
Software compensated	Freescale’s advanced non-linear calibration functions that—with the first-order hardware gain and offset calibration features—improve sensor performance.
Warm-up time	The time from the initial application of power for a sensor to reach its specified performance under the documented operating conditions.

4.2 Pin Groups

The following pin groups are used throughout the remainder of this section.

Group 1	RESETB
Group 2	RESERVED
Group 3	RGPIO[9:0]

4.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only and operation at these maximums is not guaranteed. Stress beyond the limits specified can affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 4. Absolute maximum ratings

Rating	Symbol	Minimum	Maximum	Unit
Digital supply voltage	V_{DD}	-0.3	2.0	V
Analog supply voltage	V_{DDA}	-0.3	2.0	V
Voltage difference, V_{DD} to V_{DDA}	V_{DD} - V_{DDA}	-0.1	0.1	V
Voltage difference, V_{SS} to V_{SSA}	V_{SS} - V_{SSA}	-0.1	0.1	V
Input voltage	V_{In}	-0.3	V_{DD} + 0.3	V
Input/Output pin-clamp current	I_C	-20	20	mA
Output voltage range (Open-Drain Mode)	V_{OUTOD}	-0.3	V_{DD} + 0.3	V
Storage temperature	T_{stg}	-40	125	°C
Mechanical shock	SH		5k	g

4.4 Operating Conditions

Table 5. Nominal operating conditions

Rating	Symbol	Condition(s)	Min	Typ	Max	Unit
Digital supply voltage	V_{DD}		1.71	1.8	1.89	V
Analog supply voltage	V_{DDA}		1.71	1.8	1.89	V
Voltage difference, V_{DD} to V_{DDA}	V_{DD} - V_{DDA}		-0.1		0.1	V
Voltage difference, V_{SS} to V_{SSA}	V_{SS} - V_{SSA}		-0.1		0.1	V
Input voltage high	V_{IH}		0.7*V_{DD}		V_{DD}+0.1	V
Input voltage low	V_{IL}		V_{SS} - 0.3		0.3*V_{DD}	V
Operating temperature	T_A		-40	25	85	°C

4.5 Electrostatic Discharge (ESD) and Latch-up Protection Characteristics

Table 6. ESD and latch-up protection characteristics

Rating	Symbol	Min	Max	Unit
Human Body Model (HBM)	V_{HBM}	±2000	—	V
Machine Model (MM)	V_{MM}	±200	—	V
Charge Device Model (CDM)	V_{CDM}	±500	—	V
Latch-up current at 85°C	I_{LAT}	±100	—	mA

4.6 General DC Characteristics

Table 7. DC characteristics(1)

Characteristic	Symbol	Condition(s)(2)	Min	Typ	Max	Unit
Output voltage high • Low-drive strength • High-drive strength	V_{OH}	Pin Groups 1 and 3 I_{LOAD} = -2 mA I_{LOAD} = -3 mA	VDD - 0.5	—	—	V
Output voltage low • Low-drive strength • High-drive strength	V_{OL}	Pin Groups 1 and 3 I_{LOAD} = 2 mA I_{LOAD} = 3 mA	—	—	0.5	V
Output-low current Max total I_{OL} for all ports	I_{OLT}				24	mA
Output-high current Max total I_{OH} for all ports	I_{OHT}				24	mA
Input-leakage current	$\|I_{IN}\|$	Pin Group 2 V_{in} = V_{DD} or V_{SS}	—	0.1	1	µA
Hi-Z (off-state) leakage current	$\|I_{OZ}\|$	Pin Group 3 input resistors disabled V_{in} = V_{DD} or V_{SS}	—	0.1	1	µA
Pullup resistor	R_{PU}	when enabled	17.5		52.5	KΩ
Power-on-reset voltage	V_{POR}			1.50		V
Power-on-reset hysteresis	$V_{POR-hys}$			100		mV
Input-pin capacitance	C_{IN}			7		pF
Output-pin capacitance	C_{OUT}			7		pF

1.All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8V.
2.Pin groups are defined in “Pin Groups” on page 16.

4.7 Supply Current Characteristics

Table 8. Supply current characteristics(1)

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Supply current in $STOP_{NC}$ mode	I_{DD-SNC}	Internal clocks disabled		2		µA
Supply current in $STOP_{SC}$ mode	I_{DD-SSC}	Internal clock in slow-speed mode		15		µA
Supply current in RUN mode(2)	I_{DD-R}	Internal clock in fast mode		3.1		mA

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8V$.
2. Total current with the analog section active, 16 bits ADC resolution selected, MAC unit used and all peripheral clocks enabled.

4.8 Accelerometer Transducer Mechanical Characteristics

Table 9. Accelerometer characteristics

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Full range	A_{FR}	2g	±1.8	±2	±2.2	g
		4g	±3.6	±4	±4.4	
		8g	±7.2	±8	±8.8	
Sensitivity/resolution	A_{SENS}	2g		0.061		mg/LSB
		4g		0.122		
		8g		0.244		
Zero-g level offset accuracy (Pre-board mount)	OFF_{PBM}	2g	-100		+100	mg
		4g				
		8g				
Non-linearity Best fit straight line	A_{NL}	2g		±0.25		% A_{FR}
		4g		±0.5		
		8g		±1		
Sensitivity change vs.temperature	TC_{SA}	2g		±0.17		%/°C
Zero-g level change vs. temperature(1)	TC_{Off}			±1.9		mg/°C
Zero-g Level offset accuracy (Post-board mount)	OFF_{BM}	2g	-100		+100	mg
		4g				
		8g				
Output data bandwidth	BW			ODR/2		Hz
Output noise	Noise	2g, ODR = 488 Hz		100		µg/sqrt(Hz)
		8g, ODR = 488 Hz		120		µg/sqrt(Hz)
Cross-axis sensitivity			-5		5	%

1. Relative to 25°C.

4.9 Temperature Sensor Characteristics

Table 10. Temperature sensor characteristics(1)

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Full range	T_{FR}		-40		85	°C
Sensitivity	T_{SENS}			0.00252		°C/LSB
Non-linearity	T_{NL}			±1		°C

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8V$.

4.10 ADC Characteristics

Table 11. ADC characteristics(1)

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Input voltage	V_{AI}	Voltage at AN0 or AN1	0.2		1.1	V
Differential input voltage	V_{ADI}	AN1 - AN0	-0.9		0.9	V
Full-scale range	V_{FS}			1.8		V
Programmable resolution	R_{ES}		10	14	16	Bits
Conversion time @ 14-bits resolution (Three-sample frame)	t_c			207		µs
Integral non-linearity	INL	Full Scale		±15		LSB
Differential non-linearity	DNL			±2		LSB
Input leakage	I_{IA}				±2	µA
Effective number of bits	ENOB			13.5		Bits

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8V$ and $R_{ES} = 14$, unless otherwise noted.

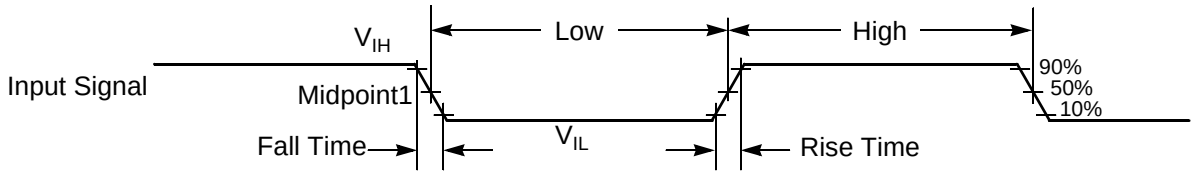
4.11 ADC Sample Rates

The MMA955xL platform supports the following sample rates:

- 488.28 frames per second (fps)
- 244.17 fps
- 122.07 fps
- 61.04 fps
- 30.52 fps
- 15.26 fps
- 7.63 fps
- 3.81 fps

4.12 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 5 on page 17. Unless otherwise specified, propagation delays are measured from the 50-percent to 50-percent point. Rise and fall times are measured between the 10-percent and 90-percent points, as shown in the following figure.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 10. Input signal measurement references

The subsequent figure shows the definitions of the following signal states:

- Active state, when a bus or signal is driven and enters a low-impedance state
- Three-stated, when a bus or signal is placed in a high-impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

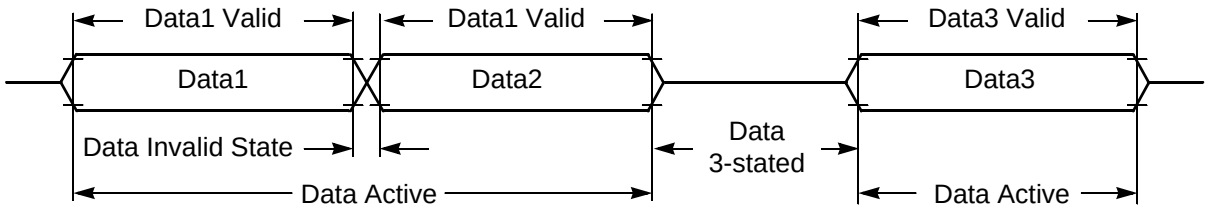


Figure 11. Signal states

4.13 General Timing Control

Table 12. General timing characteristics(1)

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
V_{DD} rise time	T_{rvdd}	10% to 90%			1	ms
POR release delay(2)	T_{POR}	Power-up	0.35		1.5	ms
Warm-up time	T_{WU}	From $STOP_{NC}$		7		sample periods
Frequency of operation	F_{OPH}	Full Speed Clock		8		MHz
	F_{OPL}	Slow Clock		62.5		KHz
System clock period	t_{CYCH}	Full Speed Clock		125		ns
	t_{CYCL}	Slow Clock		16		µs
Full/Slow clock ratio				128		
Oscillator frequency absolute accuracy @ 25°C		Full Speed Clock	-5		+5	%
Oscillator frequency variation over temperature (-40°C to 85°C vs. ambient)		Slow Clock	-6		+6	%
Minimum RESET assertion duration	t_{RA}		4T(3)			

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8$ V
2. This is the time measured from $V_{DD} = V_{POR}$ until the internal reset signal is released.
3. In the formulas, T = 1 system clock cycle. In full speed mode, T is nominally 125 ns. In slow speed mode, T is nominally 16 µs.

4.14 I²C Timing

This device includes a slave I²C module that can be used to control the sensor and can be active 100 percent of the time. It also includes a master/slave I²C module that should be used only during CPU run mode (Φ_D).

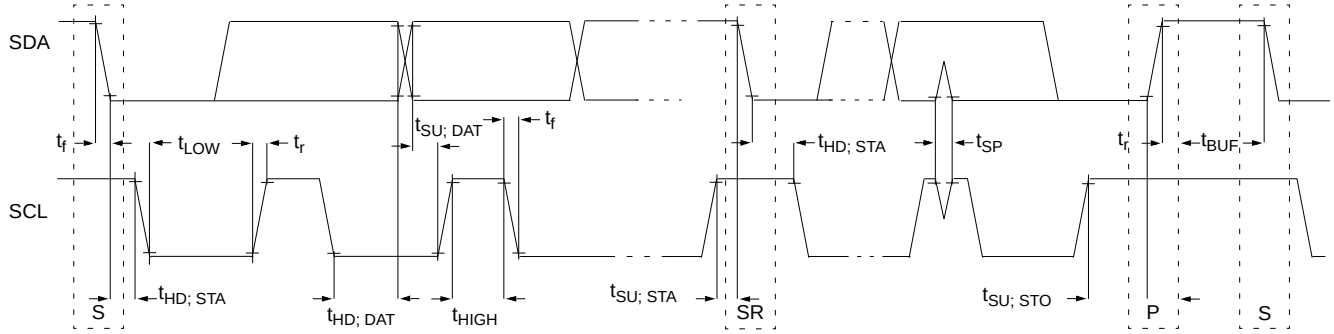


Figure 12. I²C standard and fast-mode timing

4.14.1 Slave I²C

Table 13. I²C Speed Ranges

Mode	Max Baud Rate (f_{SCL})	Minimum Bit Time	Minimum SCL Low (t_{LOW})	Minimum SCL High (t_{HIGH})	Min Data setup Time ($t_{SU;\ DAT}$)	Min/Max Data Hold Time ($t_{HD;\ DAT}$)
Standard	100 KHz	10 µs	4.7 µs	4 µs	250 ns	0 µs/3.45 µs(1)
Fast	400 KHz	2.5 µs	1.3 µs	0.6 µs	100 ns	0 µs/0.9 µs(1)
Fast +	1 MHz	1 µs	500 ns	260 ns	50 ns	0 µs/0.45 µs(1)
High-speed supported	2.0 MHz	0.5 µs	200 ns	200 ns	10 ns(2)	0 ns/70 ns (100 pf)(2)

1. The maximum $t_{HD;\ DAT}$ must be at least a transmission time less than $t_{VD;DAT}$ or $t_{VD;ACK}$. For details, see the I²C standard.
2. Timing met with IFE = 0, DS = 1, and SE = 1. See the "Port Controls" chapter in the *MMA955xL Three-Axis Accelerometer Reference Manual* (MMA955xLRM).

4.14.2 Master I²C Timing

The master I²C module should only be used when the system clock is running at full rate. Do not attempt to use the master I²C module across frames in which a portion of the time is spent in low-speed mode.

Table 14. Master I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	0.6	—	µs
Data hold time for I²C-bus devices	$t_{HD;\ DAT}$	0(1)	3.45(2)	0(1)	0.9(2)	µs
Data setup time	$t_{SU;\ DAT}$	250(3)	—	100(3) (4)	—	ns
Setup time for STOP condition	$t_{SU;\ STO}$	4.0	—	0.6	—	µs
Bus-free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

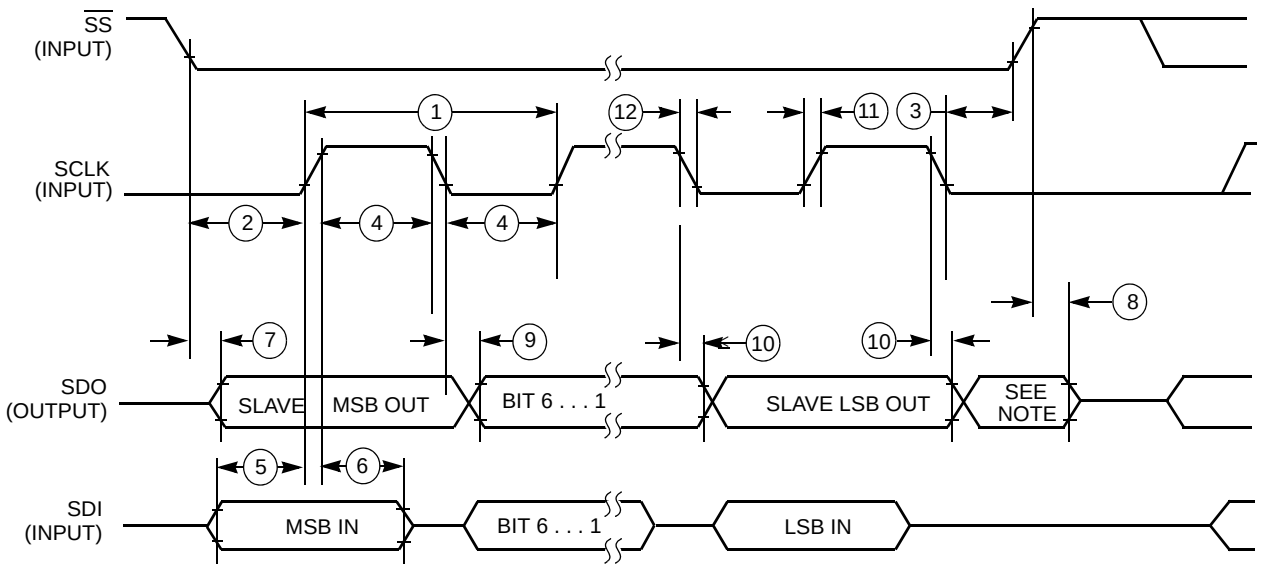
1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Setup time in slave-transmitter mode is one IPBus clock period, if the TX FIFO is empty.
4. A fast-mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $tr_{max} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C bus specification) before the SCL line is released.

4.15 Slave SPI Timing

The following table describes the timing requirements for the SPI system. The "#" column refers to the numbered time period in Figure 13.

Table 15. Slave SPI timing

#	Function	Symbol	Min	Max	Unit
—	Operating frequency	f_{op}	0	$F_{OPH}/4$	Hz
1	SCLK period	t_{SCLK}	4	—	t_{CYCH}
2	Enable lead time	t_{Lead}	0.5	—	t_{CYCH}
3	Enable lag time	t_{Lag}	0.5	—	t_{CYCH}
4	Clock (SCLK) high or low time	t_{WSCLK}	200	—	ns
5	Data setup time (inputs)	t_{SU}	15	—	ns
6	Data-hold time (inputs)	t_{HI}	25	—	ns
7	Access time	t_a	—	25	ns
8	SDO-disable time	t_{dis}	—	25	ns
9	Data valid (after SCLK edge)	t_v	—	25	ns
10	Data-hold time (outputs)	t_{HO}	0	—	ns
11	Rise time Input Output	 t_{RI} t_{RO}	 — —	 25 25	 ns ns
12	Fall time Input Output	 t_{FI} t_{FO}	 — —	 25 25	 ns ns



NOTE:

1. Not defined but normally MSB of character just received.

Figure 13. SPI slave timing

4.16 Flash Parameters

The MMA955xL platform has 16 KB of internal flash memory. There are ROM functions that allow erase and programming of that memory. Chip supply voltage of 1.8V is sufficient for the flash programming voltage.

The size of the available flash memory varies between the different devices in the MMA955xL product family, as shown in the following figure.

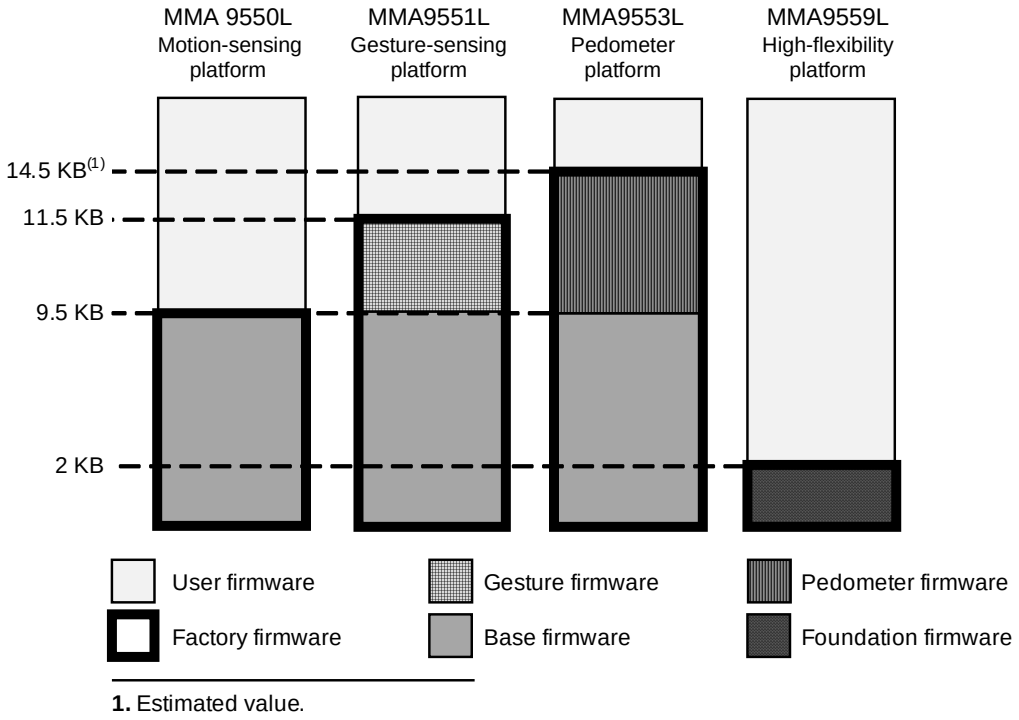


Figure 14. Flash memory map for devices

The smallest block of memory that can be written is 4 bytes and those 4 bytes must be aligned on a 4-byte boundary. The largest block of memory that can be programmed is 128 bytes and the block must start at a 128-byte boundary.

Flash programming blocks must start on a 4-byte boundary and cannot cross a 128-byte page boundary.

Table 16. Flash parameters

Parameter	Value
Word depth	4096
Row size	128 bytes
Page erase size (Erase block size)	4 rows = 512 bytes
Maximum page programming size	1 row = 128 bytes
Minimum word programming size	4 bytes
Memory organization	4096 x 32 bits = 16 KB total
Endurance	20,000 cycles minimum
Data retention	> 100 years, at room temperature

5 Package Information

The MMA955xL platform uses a 16-lead LGA package, case number 2094. Use the following link for the latest diagram of the package:

http://www.freescale.com/files/shared/doc/package_info/98ASA00287D.pdf

6 Revision History

Revision number	Revision date	Description of changes
0	06/2011	Initial release of document.
1	10/2011	• Removed MMA9552L device from product family and added the MMA9559L device. • Added a features table and a package land diagram figure. • Modified block diagram • Inserted flash memory map figure

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