100-MHz Differential Buffer for PCI Express and SATA

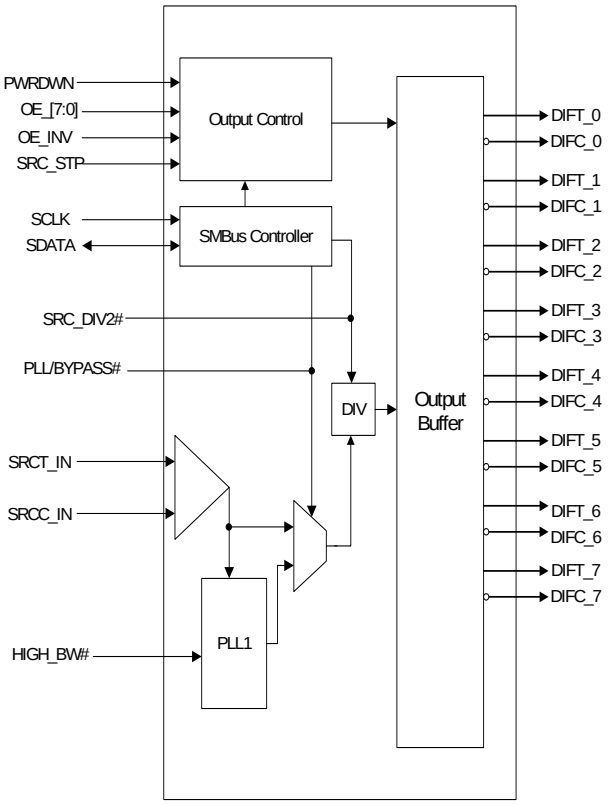
Features

- **CK409 and CK410 companion buffer**
- **Eight differential 0.7V clock output pairs**
- **OE_INV input for inverting OE, PWRDWN, and SRC_STP active levels**
- **Individual OE controls**
- **Low CTC jitter (< 50 ps)**
- **Programmable bandwidth**
- **SRC_STP power management control**
- **SMBus Block/Byte/Word Read and Write support**
- **3.3V operation**
- **PLL Bypass-configurable**
- **Divide by 2 programmable**
- **48-pin SSOP package**

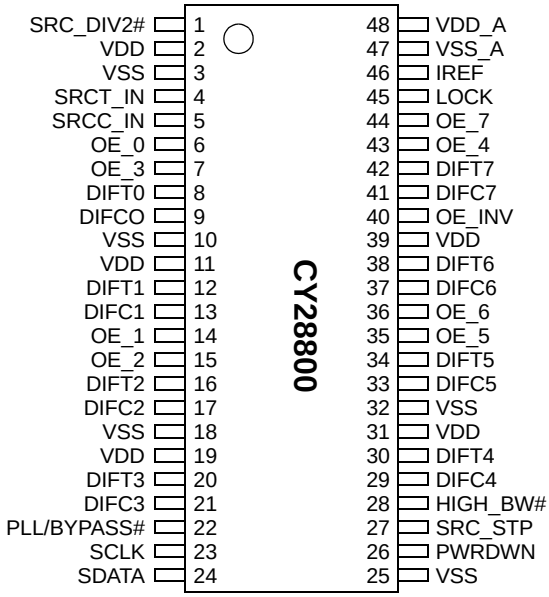
Functional Description

The CY28800 is a differential buffer and serves as a companion device to the CK409 or CK410 clock generator. The device is capable of distributing the Serial Reference Clock (SRC) in PCI Express and SATA implementations.

Block Diagram



Pin Configuration



48 SSOP

Pin Description

Pin	Name	Type	Description
4,5	SRCT_IN, SRCC_IN	I,DIF	**0.7V Differential inputs**
8,9;12,13;16,17;20,21; 30,29; 34,33;38,37;42,41	DIF[T/C][7:0]	O,DIF	**0.7V Differential Clock Outputs**
6,7,14,15,35,36,43,44	OE_[7:0]	I,SE	**3.3V LVTTL input for enabling differential outputs** Active High if OE_INV = 0 Active Low if OE_INV = 1
28	HIGH_BW#	I,SE	**3.3V LVTTL input for selecting PLL bandwidth** 0 = High BW, 1 = Low BW
45	LOCK	O,SE	**3.3V LVTTL output, transitions high when PL lock is achieved (latched output)**
26	PWRDWN	I,SE	**3.3V LVTTL input for Power Down** Active Low if OE_INV = 0 Active High if OE_INV = 1
1	SRC_DIV2#	I,SE	**3.3V LVTTL input for selecting input frequency divided by two, active low**
27	SRC_STP	I,SE	**3.3V LVTTL input for SRC_STP.** Disables stoppable outputs. Active Low if OE_INV = 0 Active High if OE_INV = 1
23	SCLK	I,SE	**SMBus Slave Clock Input**
24	SDATA	I/O,OC	**Open collector SMBus data**
46	IREF	I	**A precision resistor is attached to this pin to set the differential output current**
22	PLL/BYPASS#	I	**3.3V LVTTL input for selecting fan-out or PLL operation**
48	VDD_A	PWR	**3.3V Power Supply for PLL**
47	VSS_A	GND	**Ground for PLL**
3,10,18,25,32	VSS	GND	**Ground for outputs**
2,11,19,31,39	VDD	PWR	**3.3V power supply for outputs**
40	OE_INV	I, SE	**Input strap for setting polarity of OE_[7:0], SRC_STP, and PWRDWN**

Serial Data Interface

To enhance the flexibility and function of the clock buffer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11011100 (DCh).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 from master – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 from master – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge from host
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge from host
....	Acknowledge from slave	48:55	Data byte 1 from slave – 8 bits
....	Stop	56	Acknowledge from host
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Acknowledge from host
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Acknowledge from master
		39	Stop

Byte 0: Control Register 0

Bit	@pup	Name	Description
7	0	PWRDWN Drive Mode	Power Down drive mode 0 = Driven when stopped, 1 = Tri-state
6	0	SRC_STP Drive Mode	SRC Stop drive mode 0 = Driven when stopped, 1 = Tri-state
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	1	HIGH_BW#	HIGH_BW# 0 = High Bandwidth, 1 = Low bandwidth
1	1	PLL/BYPASS#	PLL/BYPASS# 0 = Fanout buffer, 1 = PLL mode
0	1	SRC_DIV2#	SRC_DIV2# configures output frequency at half the input frequency 0 = Divided by 2 mode (output = input/2),1 = Normal (output = input)

Byte 1: Control Register 1

Bit	@pup	Name	Description
7	1	OE_7	DIF[T/C]7 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
6	1	OE_6	DIF[T/C]6 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
5	1	OE_5	DIF[T/C]5 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
4	1	OE_4	DIF[T/C]4 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
3	1	OE_3	DIF[T/C]3 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
2	1	OE_2	DIF[T/C]2 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
1	1	OE_1	DIF[T/C]1 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
0	1	OE_0	DIF[T/C]0 Output Enable 0 = Disabled (Tri-state) 1 = Enabled

Byte 2: Control Register 2

Bit	@pup	Name	Description
7	0	SRC_STP_DIF[T/C]7	Allow Control DIF[T/C]7 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
6	0	SRC_STP_DIF[T/C]6	Allow Control DIF[T/C]6 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
5	0	SRC_STP_DIF[T/C]5	Allow Control DIF[T/C]5 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP

Byte 2: Control Register 2 (continued)

Bit	@pup	Name	Description
4	0	SRC_STP_DIF[T/C]4	Allow Control DIF[T/C]4 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
3	0	SRC_STP_DIF[T/C]3	Allow Control DIF[T/C]3 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
2	0	SRC_STP_DIF[T/C]2	Allow Control DIF[T/C]2 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
1	0	SRC_STP_DIF[T/C]1	Allow Control DIF[T/C]1 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
0	0	SRC_STP_DIF[T/C]0	Allow Control DIF[T/C]0 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP

Byte 3: Control Register 3

Bit	@pup	Name	Description
7	0		Reserved
6	0		Reserved
5	0		Reserved
4	0		Reserved
3	0		Reserved
2	0		Reserved
1	0		Reserved
0	0		Reserved

Byte 4: Vendor ID Register

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0		Reserved
6	0		Reserved
5	0		Reserved
4	0		Reserved
3	0		Reserved
2	0		Reserved
1	0		Reserved
0	0		Reserved

OE_INV Clarification

The OE_INV pin is an input strap sampled at power-on. The functionality of this input is to set the active level polarities for OE_[7:0], PWRDWN, and SRC_STP input pins. ‘Active High’ indicates the functionality of the input is asserted when the input voltage level at the pin is high and deasserted when the voltage level at the input is low. ‘Active Low’ indicates that the functionality of the input is asserted when the voltage level at the input is low and deasserted when the voltage level at the input pin is high. See V_{IH} and V_{IL} in the DC Electrical Specifications for input voltage high and low ranges.

OE_INV	PWRDWN	SRC	OE_[7:0]
0	Active Low	Active Low	Active High
1	Active High	Active High	Active Low

PWRDWN Clarification

The PWRDWN pin is an asynchronous input used to shut off all clocks cleanly and instruct the device to evoke power savings mode. It may be active high or active low depending on the strapped value of the OE_INV input. The PWRDWN pin should be asserted prior to shutting off the input clock or power to ensure all clocks shut down in a glitch-free manner. This signal is synchronized internal to the device prior to powering down the clock buffer. PWRDWN is an asynchronous input for powering up the system. When the PWRDWN pin is asserted, all clocks will be held high or tri-stated (depending on the state of the control register drive mode and OE bits) prior to turning off the VCO. All clocks will start and stop without any abnormal behavior and meet all AC and DC parameters. This means no glitches, frequency shifting or amplitude abnormalities among others.

OE_INV	PWRDWN	Mode
0	0	Power Down
0	1	Normal
1	0	Normal
1	1	Power Down

PWRDWN Assertion

When the power down pin is sampled as being asserted by two consecutive rising edges of DIFC, all DIFT outputs will be held high or Tri-stated (depending on the state of the control register drive mode and OE bits) on the next DIFC high to low transition. When the SMBus PWRDWN Drive Mode bit is programmed to ‘0’, all clock outputs will be held with the DIFT pin driven high at 2 x Iref and DIFC tri-stated. However, if the control register PWRDWN Drive Mode bit is programmed to ‘1’, then both DIFT and the DIFC are Tri-stated.

PWRDWN Deassertion

The power-up latency is less than 1 ms. This is the time from the deassertion of the PWRDWN pin or the ramping of the power supply or the time from valid SRC_IN input clocks until the time that stable clocks are output from the buffer chip (PLL locked). IF the control register PWRDWN Drive Mode bit is programmed to ‘1’, all differential outputs must be driven high in less than 300 µs of the power down pin deassertion to a voltage greater than 200 mV.

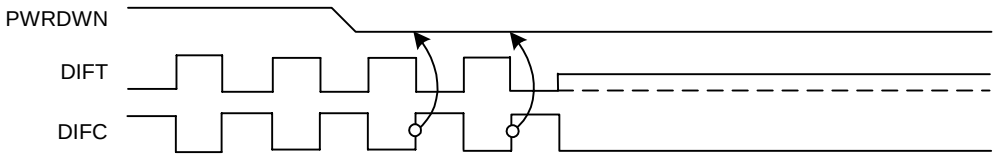


Figure 1. PWRDWN Assertion Diagram, OE_INV = 0

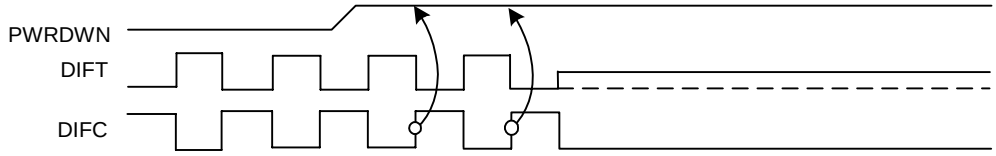


Figure 2. PWRDWN Assertion Diagram, OE_INV = 1

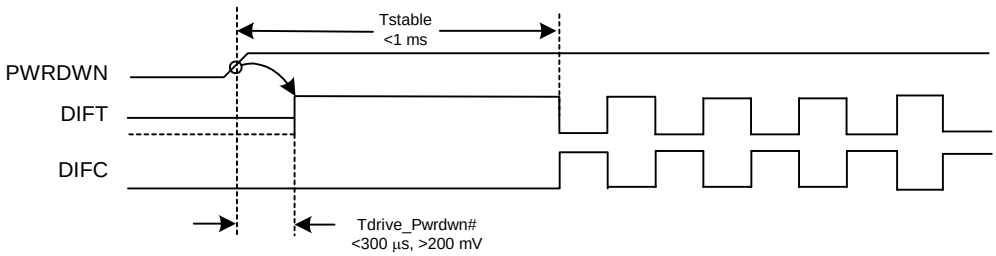


Figure 3. PWRDWN Deassertion Diagram, OE_INV = 0

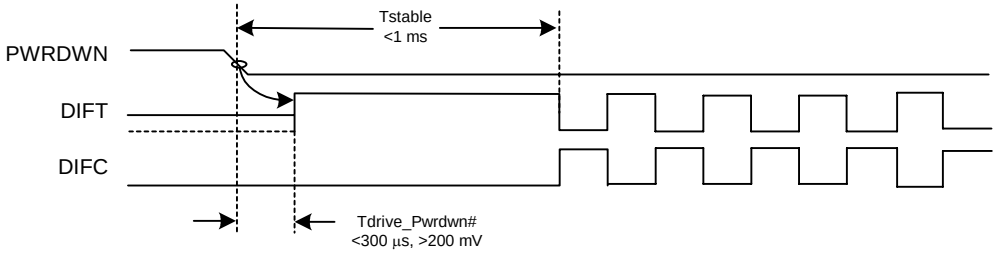


Figure 4. PWRDWN Deassertion Diagram, OE_INV = 1

Table 4. Buffer Power-up State Machine

State	Description
0	3.3V Buffer power off
1	After 3.3V supply is detected to rise above 1.8V–2.0V, the buffer enters state 1 and initiates a 0.2-ms–0.3-ms delay
2[5]	Buffer waits for PWRDWN deassertion **(and a valid clock on the SRC_IN input if in PLL mode)**
3[2, 3, 4]	Outputs enabled for normal operation (PLL lock to the SRC_IN input is assured in PLL mode)

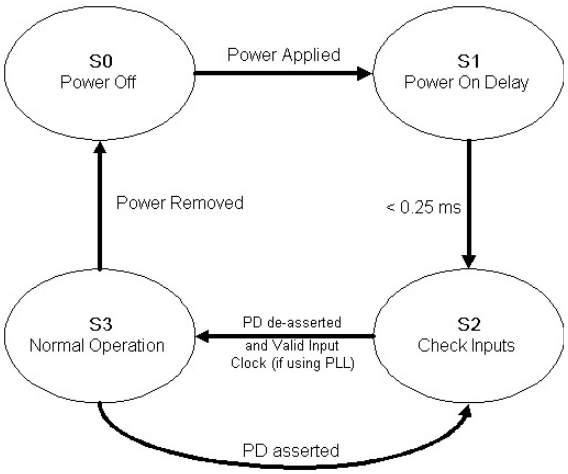


Figure 5. Buffer Power-up State Diagram[1]

SRC_STP Clarification

The SRC_STP signal is an asynchronous input used for clean stopping and starting the DIFT/C outputs. This input can be Active High or Active Low based on the strapped value of the OE_INV input. The SRC_STP signal is a debounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.) In the case where the output is disabled via OE control, the output will always be tri-stated regardless of the SRC_STP Drive Mode register bit state.

Table 5. SRC_STP Functionality[6]

OE_INV	SRC_STP	DIFT	DIFC
0	1	Normal	Normal
0	0	Iref * 6 or Float	Low
1	1	Iref * 6 or Float	Low
1	0	Normal	Normal

Notes:
1. Disabling of the SRCT_IN input clock prior to assertion of PWRDWN is an undefined mode and not recommended. Operation in this mode may result in glitches excessive frequency shifting.
2. The total power-up latency from power on to all outputs active is less than 1 ms (assuming a valid clock is present on SRC_IN input).
3. LOCK output is a latched signal that is reset with the assertion of PWRDWN or when VDD<1.8V.
4. Special care must be taken to ensure that no abnormal clock behavior occurs after the assertion PLL LOCK (i.e., overshoot/undershoot is allowed).
5. In PLL mode, if power is valid and PWRDWN is deasserted but no input clocks are present on the SRC_IN input, DIF clocks will remain disabled. Only after valid input clocks are detected, valid power, PWRDWN deasserted with the PLL locked and stable, are the DIF outputs enabled.
6. In the case where OE is asserted low, the output will always be three-stated regardless of SRC_STP drive mode register bit state.

SRC_STP Assertion

The impact of asserting the SRC_STP pin is that all DIF outputs that are set in the control registers to stoppable via assertion of SRC_STP are stopped after their next transition. When the control register SRC_STP three-state bit is programmed to '0', the final state of all stopped DIFT/C signals is DIFT clock = High and DIFC = Low. There will be no change to the output drive current values, DIFT will be driven high with a current value equal 6 x Iref, and DIFC will not be driven. When the control register SRC_STP three-state bit is programmed to '1', the final state of all stopped DIF signals is low, both DIFT clock and DIFC clock outputs will not be driven.

SRC_STP Deassertion

All differential outputs that were stopped will resume normal operation in a glitch-free manner. The maximum latency from the deassertion to active outputs is between 2-6 DIFT/C clock periods (2 clocks are shown) with all DIFT/C outputs resuming simultaneously. If the control register tri-state bit is programmed to '1' (tri-state), then all stopped DIFT outputs will be driven high within 15 ns of SRC_STP deassertion to a voltage greater than 200 mV.

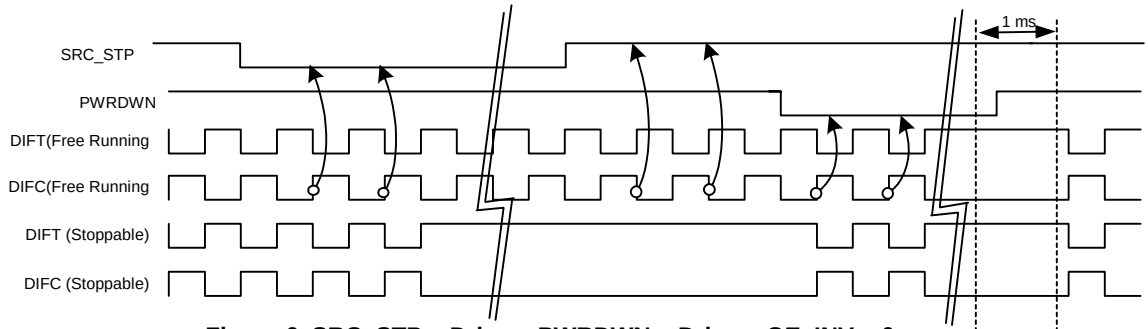


Figure 6. SRC_STP = Driven, PWRDWN = Driven, OE_INV = 0

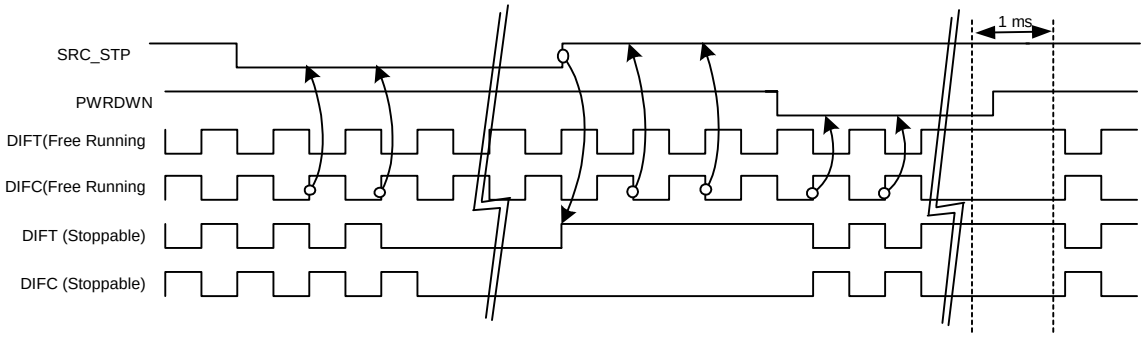


Figure 7. SRC_STP = Tri-state, PWRDWN = Driven, OE_INV = 0

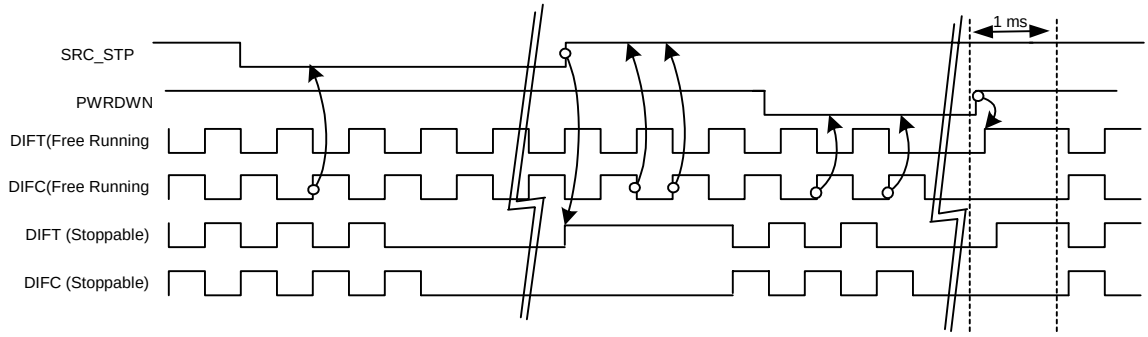


Figure 8. SRC_STP = Tri-state, PWRDWN = Tri-state, OE_INV = 0

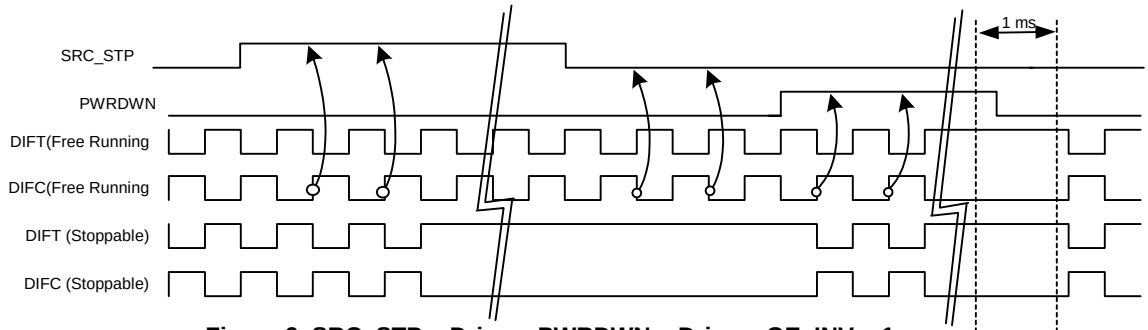


Figure 9. SRC_STP = Driven, PWRDWN = Driven, OE_INV = 1

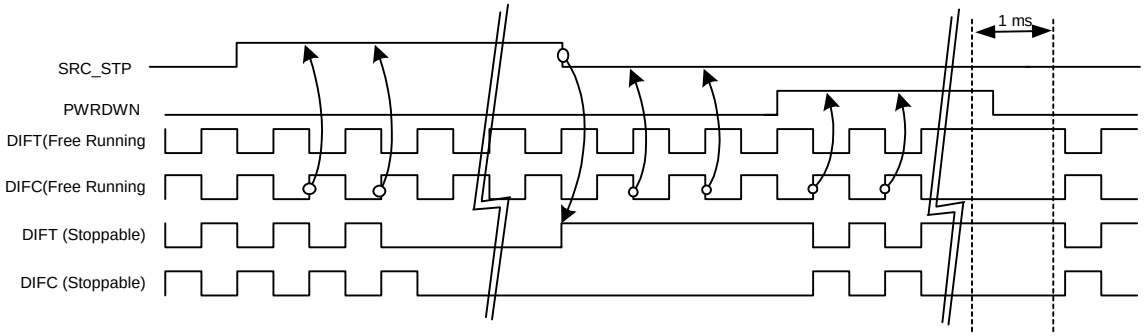


Figure 10. SRC_STP = Tri-state, PWRDWN = Driven, OE_INV = 1

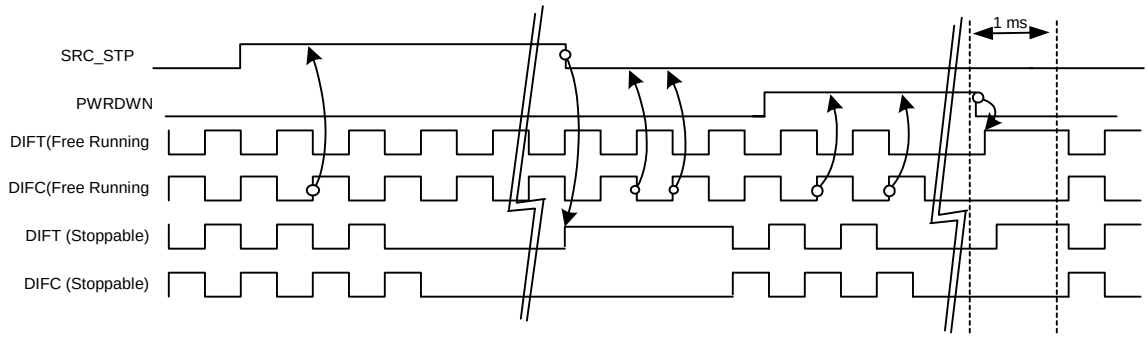


Figure 11. SRC_STP = Tri-state, PWRDWN = Tri-state, OE_INV = 1

Output Enable Clarification

OE functionality allows for enabling and disabling individual outputs. OE_[7:0] are Active High or Active Low inputs depending on the strapped value of the OE_INV input. Disabling the outputs may be implemented in two ways, via writing a '0' to SMBus register bit corresponding to output of interest or by deasserting the OE input pin. In both methods, if SMBus registered bit has been written low or the OE pin is deasserted or both, the output of interest will be tri-stated. (The assertion and deassertion of this signal is absolutely asynchronous.)

Table 6. OE Functionality

OE_INV	OE (Pin)	OE (SMBus Bit)	DIF[T/C]
0	0	0	Tri-State
0	0	1	Tri-State
0	1	0	Tri-State
0	1	1	Enabled
1	0	0	Tri-State
1	0	1	Enabled
1	1	0	Tri-State
1	1	1	Tri-State

OE Assertion

All differential outputs that were tri-stated will resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2–6 DIF clock periods. In addition, DIFT clocks will be driven high within 15 ns of OE assertion to a voltage greater than 200 mV.

OE Deassertion

The impact of deasserting OE is that each corresponding output will transition from normal operation to tri-state in a glitch-free manner. The maximum latency from the deassertion to tri-stated outputs is between two–six DIF clock periods.

LOCK Signal Clarification

The LOCK output signal is intended to provide designers a signal indicating that PLL lock has been achieved and valid clock are available. This can be helpful when cascading multiple buffers which each contribute a 1-ms start-up delay in addition to the start-up time of the clock source. Upon receiving a valid clock on the SRC_IN input (PWRDWN deasserted), the buffer will begin ramping the internal PLL until lock is achieved and stable, the clock buffer will assert the LOCK pin high and enable DIF output clocks. In other words, if power is valid and PWRDWN is deasserted but no input clocks are present on the SRC_IN input, all DIF clocks remain disabled. Only after valid input clocks are detected, valid power, PWRDWN deasserted with the PLL locked and stable are LOCK to be asserted and the DIF outputs enabled. The maximum start-up latency from valid clocks on SRC_IN input to the assertion of LOCK (output clocks are valid) is to be less than 1 ms. Once LOCK has been asserted high, it will remain high (regardless of the actual PLL status) until power is removed or the PWRDWN pin has been asserted.

SRC_DIV2# Clarification

The SRC_DIV2# input is used to configure the DIF output mode to be equal to the SRC_IN input frequency or half the input frequency in a glitch-free manner. The SRC_DIV2# function may be implemented in two ways, via writing a ‘0’ to SMBus register bit or by asserting the SRC_DIV2# input pin low. In both methods, if the SMBus register bit has been written low or the SRC_DIV2# pin is low or both, all DIF outputs will configured for divide by 2 operation.

SRC_DIV2# Assertion

The impact of asserting the SRC_DIV2# is that all DIF outputs will transition cleanly in a glitch-free manner from normal operation (output frequency equal to input) to half the input frequency within 2–6 DIF clock periods.

SRC_DIV2# Deassertion

The impact of deasserting the SRC_DIV2# is that all DIF outputs will transition cleanly in a glitch-free manner from divide by 2 mode to normal (output frequency is equal to the input frequency) operation within two–six DIF clock periods.

PLL/BYPASS# Clarification

The PLL/Bypass# input is used to select between bypass mode (no PLL) and PLL mode. In bypass mode, the input clock is passed directly to the output stage resulting in 50-ps additive jitter (50 ps + input jitter) on DIF outputs. In the case of PLL mode, the input clock is pass through a PLL to reduce high-frequency jitter. The BYPASS# mode may be selected in two ways—via writing a ‘0’ to SMBus register bit or by asserting the PLL/BYPASS# pin low. In both methods, if the SMBus register bit has been written to ‘0’ or PLL/BYPASS# pin is low or both, the device will be configure for BYPASS operation.

HIGH_BW# Clarification

The HIGH_BW# input is used to set the PLL bandwidth. This mode is intended to minimize PLL peaking when two or more buffers are cascaded by staggering device bandwidths. The PLL high bandwidth mode may be selected in two ways, via writing a ‘0’ to SMBus register bit or by asserting the HIGH_BW# pin is low or both, the device will be configured for high bandwidth operation.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional		150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000		V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD_A, VDD	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.5	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.5	V
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	3.3V Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{IL}	Input Low Leakage Current	except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5		µA
I_{IH}	Input High Leakage Current	except internal pull-down resistors, $0 < V_{IN} < V_{DD}$		5	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance		–-	6	pF
L_{IN}	Pin Inductance		–	7	nH
$I_{DD3.3V}$	Dynamic Supply Current	At max. load, Full Active Bypass Mode	–	175	mA
		At max. load, Full Active PLL Mode	–	200	mA
		All OE deasserted, Bypass	–	35	mA
		SRC_STP asserted, Outputs Driven, Bypass	–	150	mA
		SRC_STP asserted, Outputs Tri-state, Bypass	–	2	mA
		SRC_STP asserted, Outputs Driven, PLL	–	160	mA
		SRC_STP asserted, Outputs Tri-State, PLL	–	2	mA
$I_{PD3.3V}$	Power-down Supply Current	PWRDWN asserted, Outputs driven	–	65	mA
		PWRDWN asserted, Outputs Tri-stated	–	5	mA

AC Electrical Specifications (Measured in High Bandwidth Mode)

Parameter	Description	Condition	Min.	Max.	Unit
SRC_IN at 0.7V					
T_{PERIOD}	Average Period	Measured at crossing point V_{OX}	9.9970	10.0533	ns
$T_{ABSMIN-IN}$	Absolute minimum clock periods	Measured at crossing point V_{OX}	9.8720		ns
T_R / T_F	DIFT and DIFC Rise and Fall Times	Single ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525V (Averaged)	0.6	4	V/ns
V_{IH}	Differential Input High Voltage		150		mV
V_{IL}	Differential Input Low Voltage			–150	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing	Measured SE	250	550	mV

AC Electrical Specifications (continued)(Measured in High Bandwidth Mode)

Parameter	Description	Condition	Min.	Max.	Unit
ΔV_{OX}	Vcross Variation over all edges	Measured SE		140	mV
V_{RB}	Differential Ringback Voltage		–100	100	mV
T_{STABLE}	Time before ringback allowed		500		ps
V_{MAX}	Absolute maximum input voltage			1.15	V
V_{MIN}	Absolute minimum input voltage		–0.3		V
T_{DC}	DIFT and DIFC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2 * (T_R – T_F)/(T_R + T_F)$	–	20	%
DIF at 0.7V					
F_{IN}	Input Frequency	Bypass or PLL 1:1	90	210	MHz
F_{ERROR}	Input/Output Frequency Error	Bypass or PLL 1:1	–	0	ppm
T_{DC}	DIFT and DIFC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	Average Period	Measured at crossing point V_{OX} at 100 MHz	9.9970	10.0533	ns
T_R / T_F	DIFT and DIFC Rise and Fall Times	Single ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525V (Averaged)	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2 * (T_R – T_F)/(T_R + T_F)$	–	20	%
$\Delta T_R/\Delta T_F$	Rise and Fall Time Variation Variation	Single ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525V (Real Time)	–	125	ps
V_{HIGH}	Voltage High	Measured SE	660	850	mv
V_{LOW}	Voltage Low	Measured SE	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing	Measured SE	250	550	mv
ΔV_{OX}	Vcross Variation over all edges	Measured SE	–	140	mV
V_{OVS}	Maximum Overshoot Voltage	Measured SE	–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage	Measured SE	–	–0.3	V
V_{RB}	Ring Back Voltage	Measured SE	0.2	N/A	V
T_{CCJ}	Cycle to Cycle Jitter	PLL Mode	–	50	ps
		Bypass Mode (Jitter is additive)	–	50	ps
T_{SKEW}	Any DIFT/C to DIFT/C Clock Skew	Measured at crossing point V_{OX}	–	50	ps
T_{PD}	Input to output skew in PLL mode	Measured at crossing point V_{OX}	–	±250	ps
	Input to output skew in Non-PLL mode	Measured at crossing point V_{OX}	2.5	4.5	ns

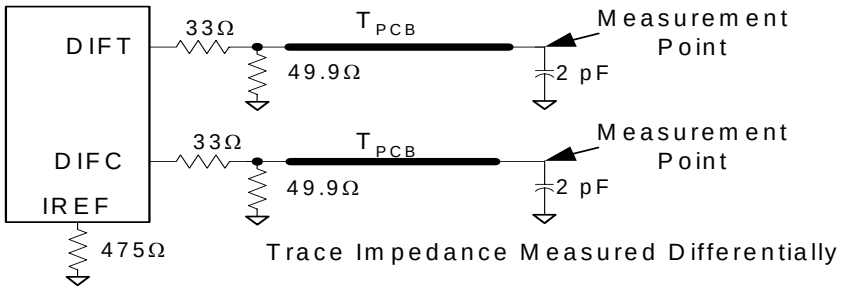


Figure 12. Differential Clock Termination

Switching Waveforms

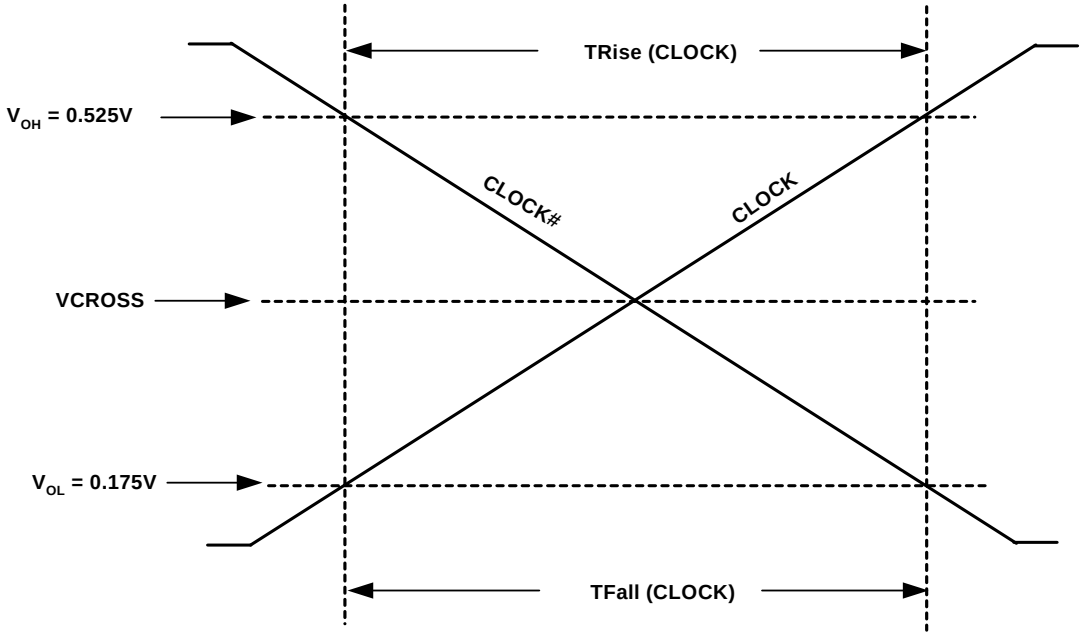


Figure 13. Single-Ended Measurement Points for TRise and TFall

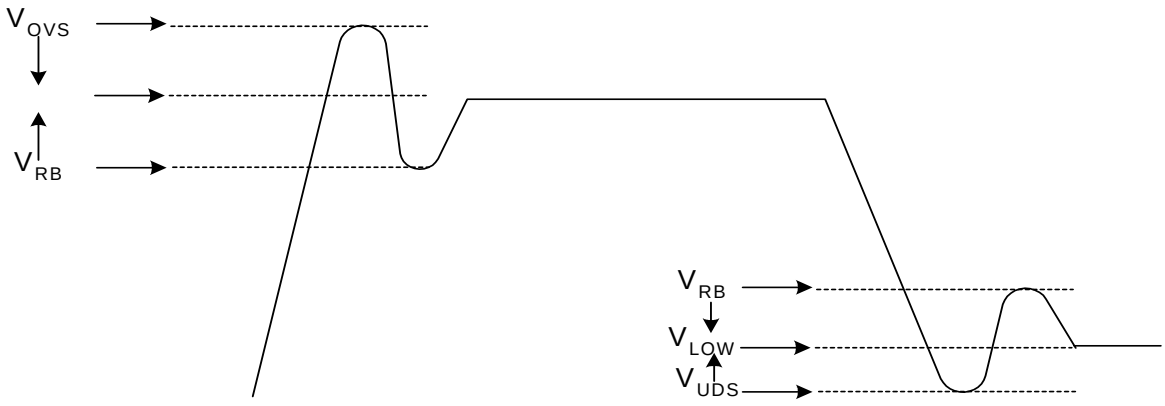


Figure 14. Single-ended Measurement Points for V_{OVS},V_{UDS} and V_{RB}

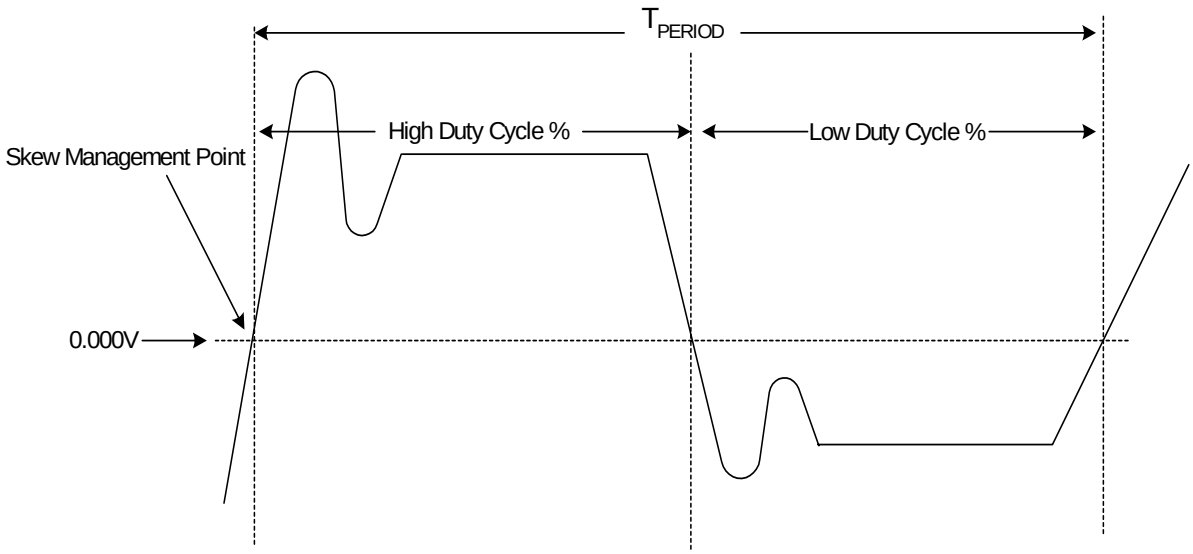


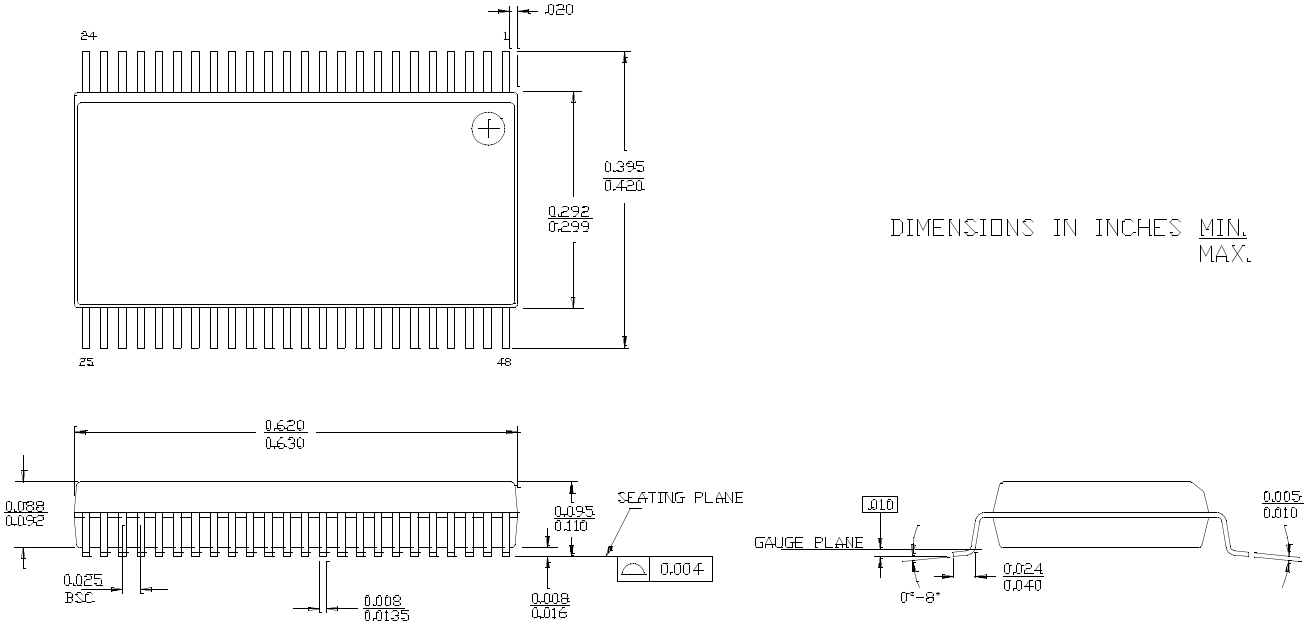
Figure 15. Differential (Clock-Clock#) Measurement Points (Tperiod, Duty Cycle and Jitter)

Ordering Information

Ordering Code	Package Type	Operating Range
Lead Free		
CY28800OXC	48-pin SSOP	Commercial, 0°C to 70 °C
CY28800OXCT	48-pin SSOP–Tape and Reel	Commercial, 0°C to 70 °C

Package Drawing and Dimensions

48-Lead Shrunk Small Outline Package O48



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Document History Page

Document Title: CY28800 100-MHz Differential Buffer for PCI Express and SATA Document Number: 38-07723				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	299711	See ECN	RGL	New data sheet
*A	404280	See ECN	RGL	IDD 3.3V Dynamic Supply Current: At max. load, Full Active Bypass Mode – 175 mA At max. load, Full Active PLL Mode – 200 mA All OE deasserted, Bypass – 35 mA
*B	465413	See ECN	RGL	Minor Change: To post on web