

SANYO**LC75345M****Electronic Volume Control System
on-Chip****Overview**

The LC75345M is an electronic volume system that can control the volume, balance, 2-band equalizer, super bass, and input switching functions by serial data input.

Functions

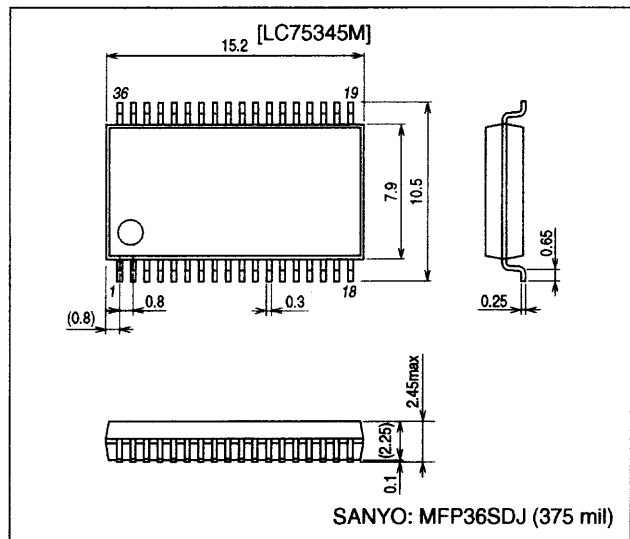
- Volume: 0 dB to -78 dB (1-dB step) and $-\infty$ (64 positions)
0 dB to -50 dB (1-dB step), -50 dB to -70 dB (2-dB step), -70-dB to -78 dB (4-dB step)
Balance function with separate L/R control
- Treble: ± 10 -dB control in 2-dB steps is possible. Shelving characteristic.
- Bass: ± 10 -dB control in 2-dB steps is possible. Peaking characteristics.
- Super bass: +10-dB control in 2-dB steps is possible. Peaking characteristics.
- Selector: 5 input signals can be selected both for L and R
- Input gain: 0 dB to +30 dB (2-dB step) amplification is possible for the input signal.
- General-purpose amp (ATT): 2 on-chip general-purpose amplifiers

Features

- On-chip buffer amplifier cuts down number of external components
- Low switching noise generated by on-chip switch due to use of silicon gate CMOS process
- On-chip reference voltage circuit for analog ground
- Controls performed with serial data input (CCB)

Package Dimensions

unit: mm

3263-MFP36SDJ (375 mil)

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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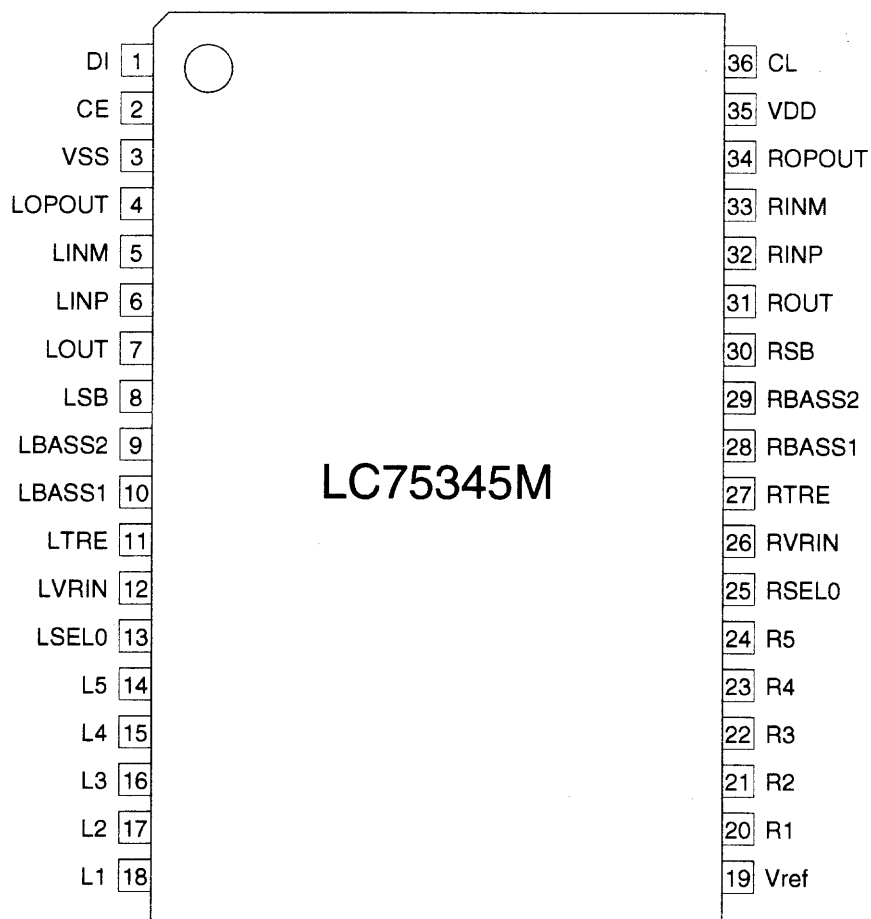
SANYO Electric Co., Ltd. Semiconductor Company

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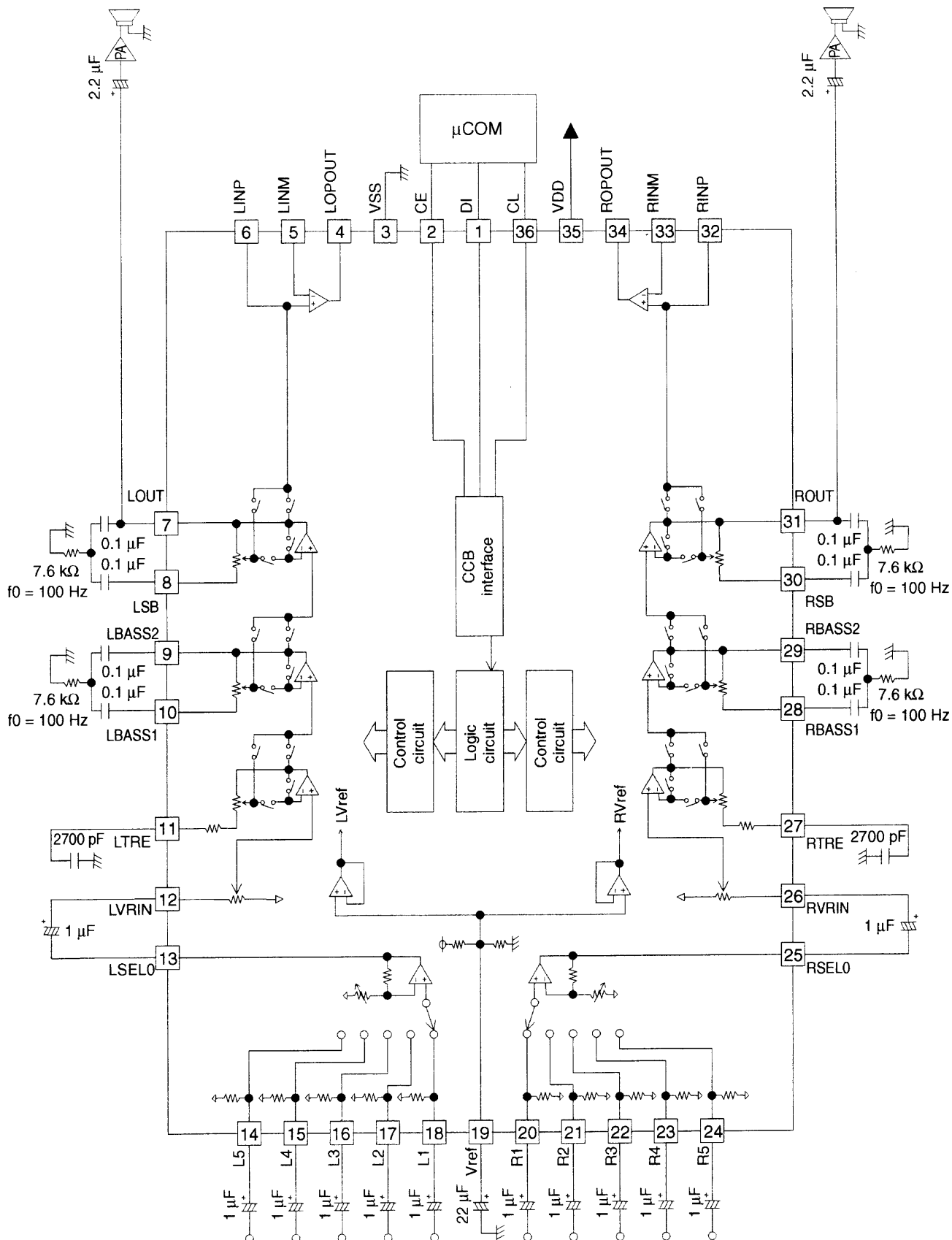
20901RM (OT) No. 6868-1/22

LC75345M

Pin Assignment



Sample Application Circuit



Note: When a general-purpose amp is not used, leave the LINP (RINP) open and connect the LINM (RINM) with the LOPOUT (ROPOUT).

Specifications

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

| Parameter | Symbol | Pin Name | Conditions | Ratings | Unit |
|-----------------------------|---------------------|--|------------------------------|--|------|
| Maximum supply voltage | V _{DD} max | V _{DD} | | 10.5 | V |
| Maximum input voltage | V _{IN} max | CE, DI, CL | | -0.3 to 10.5 | V |
| | | L1 to L5, R1 to R5, LVRIN, RVRIN, LINP, RINP, LINM, RINM | | V _{SS} - 0.3 to V _{DD} + 0.3 | V |
| Allowable power dissipation | Pdmax | | *1 Ta ≤ 75°C, independent IC | 520 | mW |
| Operating temperature | Topr | | | -30 to +75 | °C |
| Storage temperature | Tstg | | | -40 to +125 | °C |

Allowable Operating Ranges at Ta = -30 to +75°C, VSS = 0 V

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|--------------------------|--------------------|--|-----------------------------|-----------------|-----|-----------------|------|
| | | | | min | typ | max | |
| Supply voltage | V _{DD} | V _{DD} | | 4.5 | | 9 | V |
| Input high-level voltage | V _{IH} | CL, DI, CE | | 2.0 | | 9 | V |
| Input low-level voltage | V _{IL} | CL, DI, CE | 7.5 ≤ V _{DD} ≤ 9 | V _{SS} | | 0.8 | V |
| | | | 4.5 ≤ V _{DD} ≤ 7.5 | V _{SS} | | 0.3 | |
| Input amplitude voltage | V _{IN} | L1 to L5, R1 to R5, LVRIN, RVRIN, LINP, RINP, LINM, RINM | | V _{SS} | | V _{DD} | Vp-p |
| Input pulse width | t _{øW} | CL | | 1 | | | μs |
| Setup time | t _{setup} | CL, DI, CE | | 1 | | | μs |
| Hold time | t _{hold} | CL, DI, CE | | 1 | | | μs |
| Operating frequency | f _{opg} | CL | | | | 500 | kHz |

Electrical Characteristics at Ta = 25°C, VDD = 8 V, VSS = 0 V

Input block

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|------------------------|--------------------|--|-----------------------|---------|------|-----|------------------|
| | | | | min | typ | max | |
| Maximum input gain | G _{inmax} | | | | +30 | | dB |
| Step resolution | G _{step} | | | | +2 | | dB |
| Input resistance | R _{in} | L1, L2, L3, L4, L5 R1, R2, R3, R4, R5 | | | 50 | | kΩ |
| Clipping level | V _{cl} | LSELO, RSELO | THD = 1.0%, f = 1 kHz | | 2.50 | | V _{rms} |
| Output load resistance | R _l | LSELO, RSELO | | 10 | | | kΩ |

Volume block

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|------------------|-----------------|----------|------------|---------|-----|-----|------|
| | | | | min | typ | max | |
| Input resistance | R _{in} | LIN, RIN | | | 50 | | kΩ |

Treble band equalizer control block

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|------------------------------|-------------------|----------|----------------|---------|------|-----|------|
| | | | | min | typ | max | |
| Control range | Geq | | max. boost/cut | ±8 | ±10 | ±12 | dB |
| Step resolution | E _{step} | | | 1 | 2 | 3 | dB |
| Internal feedback resistance | R _{feed} | | | | 51.7 | | kΩ |

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Bass band equalizer control block

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|------------------------------|--------|----------|----------------|---------|------|-----|------|
| | | | | min | typ | max | |
| Control range | Geq | | max. boost/cut | ±8 | ±10 | ±12 | dB |
| Step resolution | Estep | | | 1 | 2 | 3 | dB |
| Internal feedback resistance | Rfeed | | | | 33.1 | | kΩ |

Super bass band equalizer control block

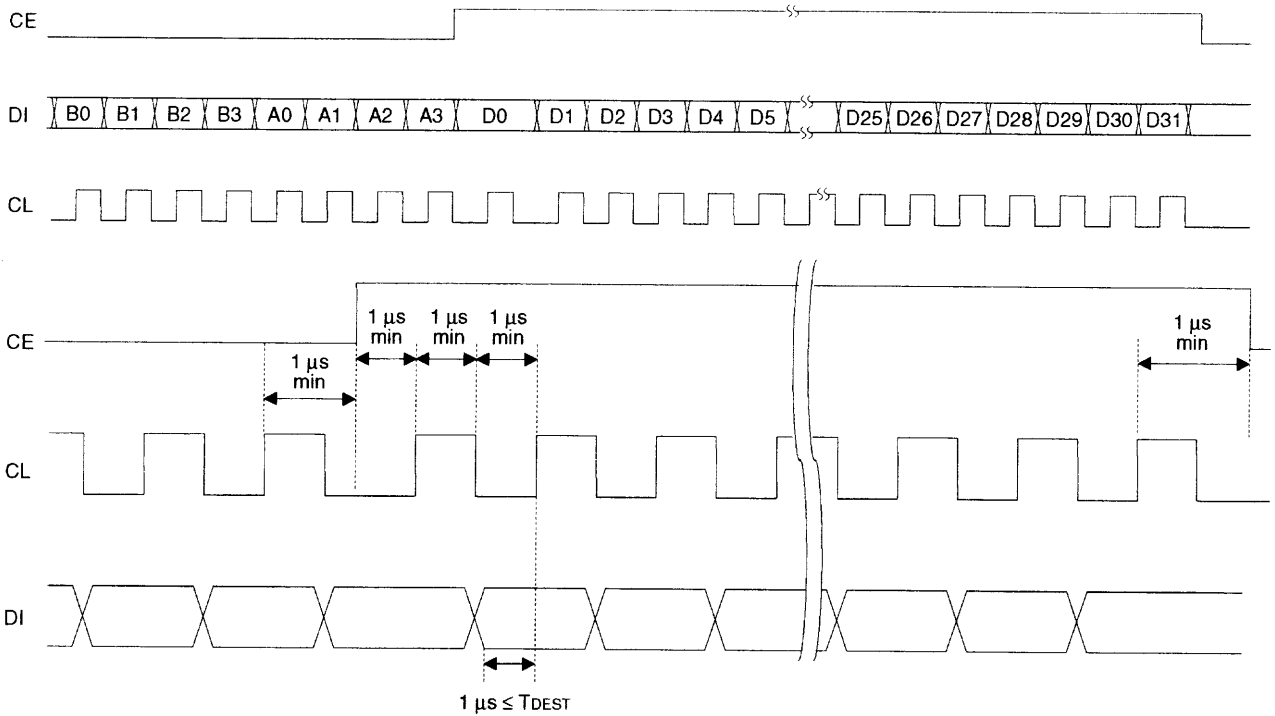
| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|------------------------------|--------|----------|------------|---------|------|-----|------|
| | | | | min | typ | max | |
| Control range | Geq | | max. boost | +8 | +10 | +12 | dB |
| Step resolution | Estep | | | 1 | 2 | 3 | dB |
| Internal feedback resistance | Rfeed | | | | 33.1 | | kΩ |

General

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|----------|---|---------|-----|------|------|
| | | | min | typ | max | |
| Total harmonic distortion | THD | $V_{IN} = 1 \text{ V}_{rms}$, $f = 1 \text{ KHz}$, total flat overall | | | 0.01 | % |
| Crosstalk | CT | $V_{IN} = 1 \text{ V}_{rms}$, $f = 1 \text{ KHz}$, $R_g = 1 \text{ k}\Omega$, total flat overall | 80 | | | dB |
| Output noise voltage | VN | Flat overall, 80 kHz L.P.F | 9.3 | | | μV |
| Maximum attenuated output | Vomin | Flat overall, $f = 1 \text{ kHz}$ | | -90 | | dB |
| Current drain | I_{DD} | $V_{DD} - V_{SS} = +9 \text{ V}$ | | 40 | | mA |
| Input high-level current | I_{IH} | CL, DI, CE: $V_{IN} = 9 \text{ V}$ | | | 10 | μA |
| Input low-level current | I_{IL} | CL, DI, CE: $V_{IN} = 0 \text{ V}$ | -10 | | | μA |

Control Timing and Data Format

To control the LC75345M, input specified serial data to the CL, DI, and CE pins. The data configuration consists of a total of 40 bits broken down into 8 address bits and 32 data bits.



• Address Code (B0 to A3)

The LC75345M has an 8-bit address code and common specifications with a SANYO serial bus CCB IC are possible.

| | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|---------|
| Address code (LSB) | B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | (82HEX) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | |

• Control Code Allocation

Input switching control

(L1, L2, L3, L4, L5, R1, R2, R3, R4, R5)

| D0 | D1 | D2 | D3 | Operation |
|----|----|----|----|---------------------------------------|
| 0 | 0 | 0 | 0 | L1 (R1) on |
| 1 | 0 | 0 | 0 | L2 (R2) on |
| 0 | 1 | 0 | 0 | L3 (R3) on |
| 1 | 1 | 0 | 0 | L4 (R4) on |
| 0 | 0 | 1 | 0 | L5 (R5) on |
| 1 | 0 | 1 | 0 | Analog ground connection |
| 0 | 1 | 1 | 0 | Test mode |
| 1 | 1 | 1 | 0 | Must not be used in normal operation. |

Input gain control

| D4 | D5 | D6 | D7 | Operation |
|----|----|----|----|-----------|
| 0 | 0 | 0 | 0 | 0 dB |
| 1 | 0 | 0 | 0 | +2 dB |
| 0 | 1 | 0 | 0 | +4 dB |
| 1 | 1 | 0 | 0 | +6 dB |
| 0 | 0 | 1 | 0 | +8 dB |
| 1 | 0 | 1 | 0 | +10 dB |
| 0 | 1 | 1 | 0 | +12 dB |
| 1 | 1 | 1 | 0 | +14 dB |
| 0 | 0 | 0 | 1 | +16 dB |
| 1 | 0 | 0 | 1 | +18 dB |
| 0 | 1 | 0 | 1 | +20 dB |
| 1 | 1 | 0 | 1 | +22 dB |
| 0 | 0 | 1 | 1 | +24 dB |
| 1 | 0 | 1 | 1 | +26 dB |
| 0 | 1 | 1 | 1 | +28 dB |
| 1 | 1 | 1 | 1 | +30 dB |

Volume control

| D8 | D9 | D10 | D11 | D12 | D13 | Operation |
|----|----|-----|-----|-----|-----|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 dB |
| 1 | 0 | 0 | 0 | 0 | 0 | -1 dB |
| 0 | 1 | 0 | 0 | 0 | 0 | -2 dB |
| 1 | 1 | 0 | 0 | 0 | 1 | -3 dB |
| 0 | 0 | 1 | 0 | 0 | 0 | -4 dB |
| 1 | 0 | 1 | 0 | 0 | 0 | -5 dB |
| 0 | 1 | 1 | 0 | 0 | 0 | -6 dB |
| 1 | 1 | 1 | 0 | 0 | 0 | -7 dB |
| 0 | 0 | 0 | 1 | 0 | 0 | -8 dB |
| 1 | 0 | 0 | 1 | 0 | 0 | -9 dB |
| 0 | 1 | 0 | 1 | 0 | 0 | -10 dB |
| 1 | 1 | 0 | 1 | 0 | 0 | -11 dB |
| 0 | 0 | 1 | 1 | 0 | 0 | -12 dB |
| 1 | 0 | 1 | 1 | 0 | 0 | -13 dB |
| 0 | 1 | 1 | 1 | 0 | 0 | -14 dB |
| 1 | 1 | 1 | 1 | 0 | 0 | -15 dB |
| 0 | 0 | 0 | 0 | 1 | 0 | -16 dB |
| 1 | 0 | 0 | 0 | 1 | 0 | -17 dB |
| 0 | 1 | 0 | 0 | 1 | 0 | -18 dB |
| 1 | 1 | 0 | 0 | 1 | 0 | -19 dB |
| 0 | 0 | 1 | 0 | 1 | 0 | -20 dB |
| 1 | 0 | 1 | 0 | 1 | 0 | -21 dB |
| 0 | 1 | 1 | 0 | 1 | 0 | -22 dB |
| 1 | 1 | 1 | 0 | 1 | 0 | -23 dB |
| 0 | 0 | 0 | 1 | 1 | 0 | -24 dB |
| 1 | 0 | 0 | 1 | 1 | 0 | -25 dB |
| 0 | 1 | 0 | 1 | 1 | 0 | -26 dB |
| 1 | 1 | 0 | 1 | 1 | 0 | -27 dB |
| 0 | 0 | 1 | 1 | 1 | 0 | -28 dB |
| 1 | 0 | 1 | 1 | 1 | 0 | -29 dB |
| 0 | 1 | 1 | 1 | 1 | 0 | -30 dB |
| 1 | 1 | 1 | 1 | 1 | 0 | -31 dB |
| 0 | 0 | 0 | 0 | 0 | 1 | -32 dB |
| 1 | 0 | 0 | 0 | 0 | 1 | -33 dB |
| 0 | 1 | 0 | 0 | 0 | 1 | -34 dB |
| 1 | 1 | 0 | 0 | 0 | 1 | -35 dB |
| 0 | 0 | 1 | 0 | 0 | 1 | -36 dB |
| 1 | 0 | 1 | 0 | 0 | 1 | -37 dB |
| 0 | 1 | 1 | 0 | 0 | 1 | -38 dB |
| 1 | 1 | 1 | 0 | 0 | 1 | -39 dB |
| 0 | 0 | 0 | 1 | 0 | 1 | -40 dB |
| 1 | 0 | 0 | 1 | 0 | 1 | -41 dB |
| 0 | 1 | 0 | 1 | 0 | 1 | -42 dB |
| 1 | 1 | 0 | 1 | 0 | 1 | -43 dB |
| 0 | 0 | 1 | 1 | 0 | 1 | -44 dB |
| 1 | 0 | 1 | 1 | 0 | 1 | -45 dB |
| 0 | 1 | 1 | 1 | 0 | 1 | -46 dB |
| 1 | 1 | 1 | 1 | 0 | 1 | -47 dB |
| 0 | 0 | 0 | 0 | 1 | 1 | -48 dB |
| 1 | 0 | 0 | 0 | 1 | 1 | -49 dB |
| 0 | 1 | 0 | 0 | 1 | 1 | -50 dB |

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| D8 | D9 | D10 | D11 | D12 | D13 | Operation |
|----|----|-----|-----|-----|-----|-----------|
| 1 | 1 | 0 | 0 | 1 | 1 | -52 dB |
| 0 | 0 | 1 | 0 | 1 | 1 | -54 dB |
| 1 | 0 | 1 | 0 | 1 | 1 | -56 dB |
| 0 | 1 | 1 | 0 | 1 | 1 | -58 dB |
| 1 | 1 | 1 | 0 | 1 | 1 | -60 dB |
| 0 | 0 | 0 | 1 | 1 | 1 | -62 dB |
| 1 | 0 | 0 | 1 | 1 | 1 | -64 dB |
| 0 | 1 | 0 | 1 | 1 | 1 | -66 dB |
| 1 | 1 | 0 | 1 | 1 | 1 | -68 dB |
| 0 | 0 | 1 | 1 | 1 | 1 | -70 dB |
| 1 | 0 | 1 | 1 | 1 | 1 | -74 dB |
| 0 | 1 | 1 | 1 | 1 | 1 | -78 dB |
| 1 | 1 | 1 | 1 | 1 | 1 | -∞ dB |

Channel selection

| D14 | D15 | Operation |
|-----|-----|------------------|
| 1 | 0 | Right channel |
| 0 | 1 | Left channel |
| 1 | 1 | L/R simultaneous |

Treble control

| D16 | D17 | D18 | D19 | Operation |
|-----|-----|-----|-----|-----------|
| 1 | 0 | 1 | 0 | +10 dB |
| 0 | 0 | 1 | 0 | +8 dB |
| 1 | 1 | 0 | 0 | +6 dB |
| 0 | 1 | 0 | 0 | +4 dB |
| 1 | 0 | 0 | 0 | +2 dB |
| 0 | 0 | 0 | 0 | 0 dB |
| 1 | 0 | 0 | 1 | -2 dB |
| 0 | 1 | 0 | 1 | -4 dB |
| 1 | 1 | 0 | 1 | -6 dB |
| 0 | 0 | 1 | 1 | -8 dB |
| 1 | 0 | 1 | 1 | -10 dB |

Bass control

| D20 | D21 | D22 | D23 | Operation |
|-----|-----|-----|-----|-----------|
| 1 | 0 | 1 | 0 | +10 dB |
| 0 | 0 | 1 | 0 | +8 dB |
| 1 | 1 | 0 | 0 | +6 dB |
| 0 | 1 | 0 | 0 | +4 dB |
| 1 | 0 | 0 | 0 | +2 dB |
| 0 | 0 | 0 | 0 | 0 dB |
| 1 | 0 | 0 | 1 | -2 dB |
| 0 | 1 | 0 | 1 | -4 dB |
| 1 | 1 | 0 | 1 | -6 dB |
| 0 | 0 | 1 | 1 | -8 dB |
| 1 | 0 | 1 | 1 | -10 dB |

Super bass control

| D24 | D25 | D26 | D27 | Operation |
|-----|-----|-----|-----|-----------|
| 1 | 0 | 1 | 0 | +10 dB |
| 0 | 0 | 1 | 0 | +8 dB |
| 1 | 1 | 0 | 0 | +6 dB |
| 0 | 1 | 0 | 0 | +4 dB |
| 1 | 0 | 0 | 0 | +2 dB |
| 0 | 0 | 0 | 0 | 0 dB |
| 1 | 0 | 0 | 1 | -2 dB |
| 0 | 1 | 0 | 1 | -4 dB |
| 1 | 1 | 0 | 1 | -6 dB |
| 0 | 0 | 1 | 1 | -8 dB |
| 1 | 0 | 1 | 1 | -10 dB |

D28 to D31 test mode

(Fixed to 0)

| D28 | D29 | D30 | D31 | Operation |
|-----|-----|-----|-----|-----------|
| 0 | 0 | 0 | 0 | |

Pin Functions

| Pin No. | Pin Name | Function | Equivalent circuit |
|--|--|--|--------------------|
| 18 17 16 15 14 20 21 22 23 24 | L1 L2 L3 L4 L5 R1 R2 R3 R4 R5 | • Input signal pins | |
| 13 25 | LSEL0 RSEL0 | • Input selector output pins | |
| 10 9 28 29 8 30 | LBASS1 LBASS2 RBASS1 RBASS2 LSB RSB | • Capacitor and resistor connection pins for configuring filter, used for bass and super bass band | |
| 7 31 | LOUT ROUT | • ATT + equalizer output pins/Capacitor connection pins used to configure super bass filter | |
| 12 26 | LVRIN RVRIN | • Volume input pins | |
| 11 27 | LTRE RTRE | • Capacitor connection pins for configuring treble band filter | |

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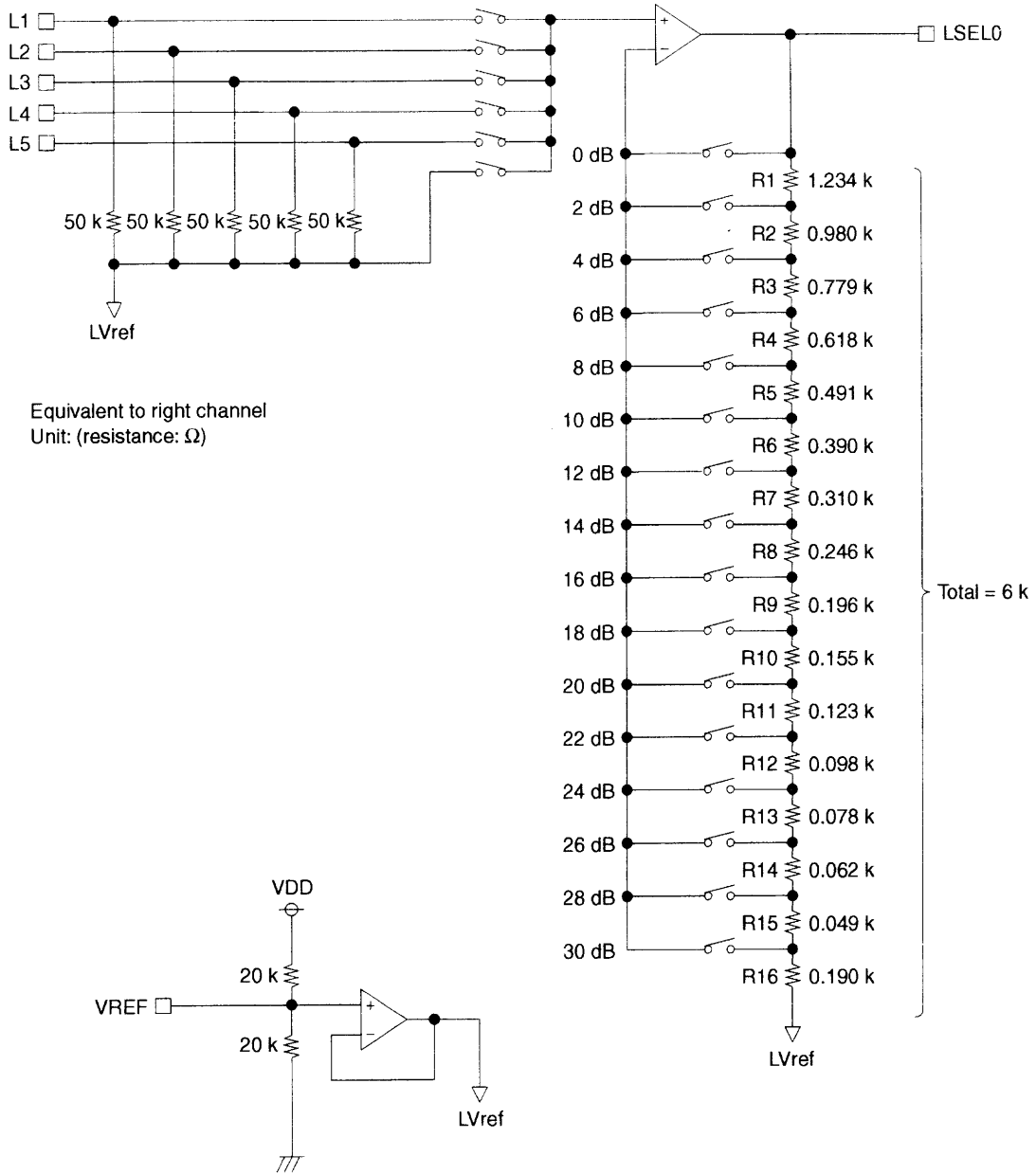
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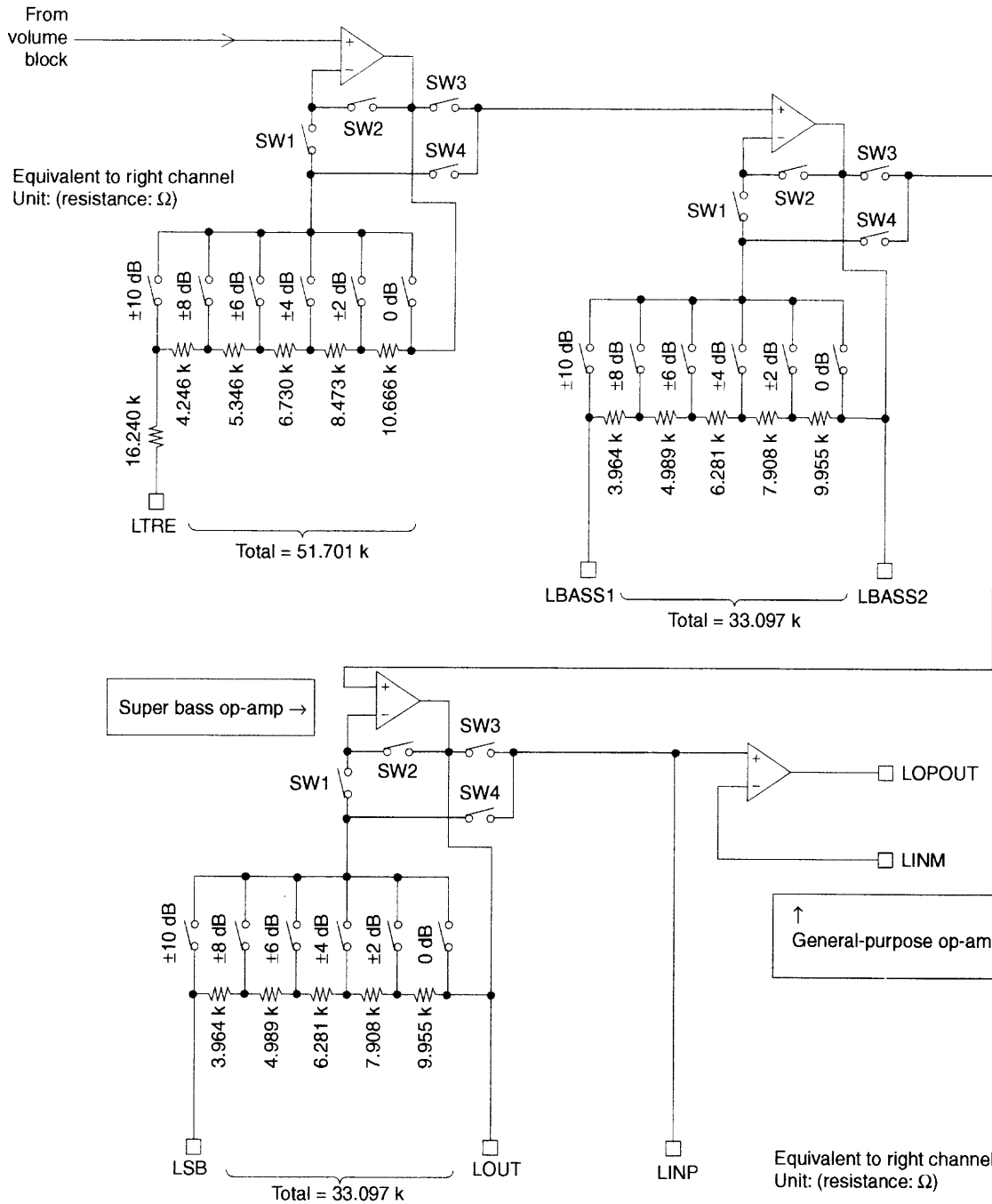
| Pin No. | Pin Name | Function | Equivalent circuit |
|---------|------------------|---|--------------------|
| 19 | Vref | <ul style="list-style-type: none"> Connect a capacitor of a few tens of μF between Vref and AVSS (V_{SS}) as a analog ground $0.5 \times V_{DD}$ voltage generator, current ripple countermeasure. | |
| 3 | VSS | <ul style="list-style-type: none"> Ground pin | |
| 35 | VDD | <ul style="list-style-type: none"> Power supply pin | |
| 2 | CE | <ul style="list-style-type: none"> Chip enable pin Data is written to the internal latch and the analog switches are operated when the level changes from high to low. Data transfer is enabled when the level is high. | |
| 1 36 | DI CL | <ul style="list-style-type: none"> Serial data pins and clock input pin for control | |
| 6 32 | LINP RINP | <p>Non-inverted input pins of general-purpose op-amp</p> <p>When not used, leave open.</p> | |
| 5 33 | LINM RINM | <p>Inverted input pins of general-purpose op-amp.</p> <p>When not used, connect these pins to the L(R) OPOUT Pins.</p> <p>(Connected between pin 5 and pin 4)</p> <p>(Connected between pin 33 and pin 34)</p> | |
| 4 34 | LOPOUT ROPOUT | <p>General-purpose op-amp output pins.</p> <p>When not used, connect these pins to the L(R) INM pins.</p> <p>(Connected between pin 5 and pin 4)</p> <p>(Connected between pin 33 and pin 34)</p> | |

Equivalent Circuit

- Selector Block/Reference Voltage Generator



• Treble/Bass/Super Bass Band Multi-Purpose Op Amp

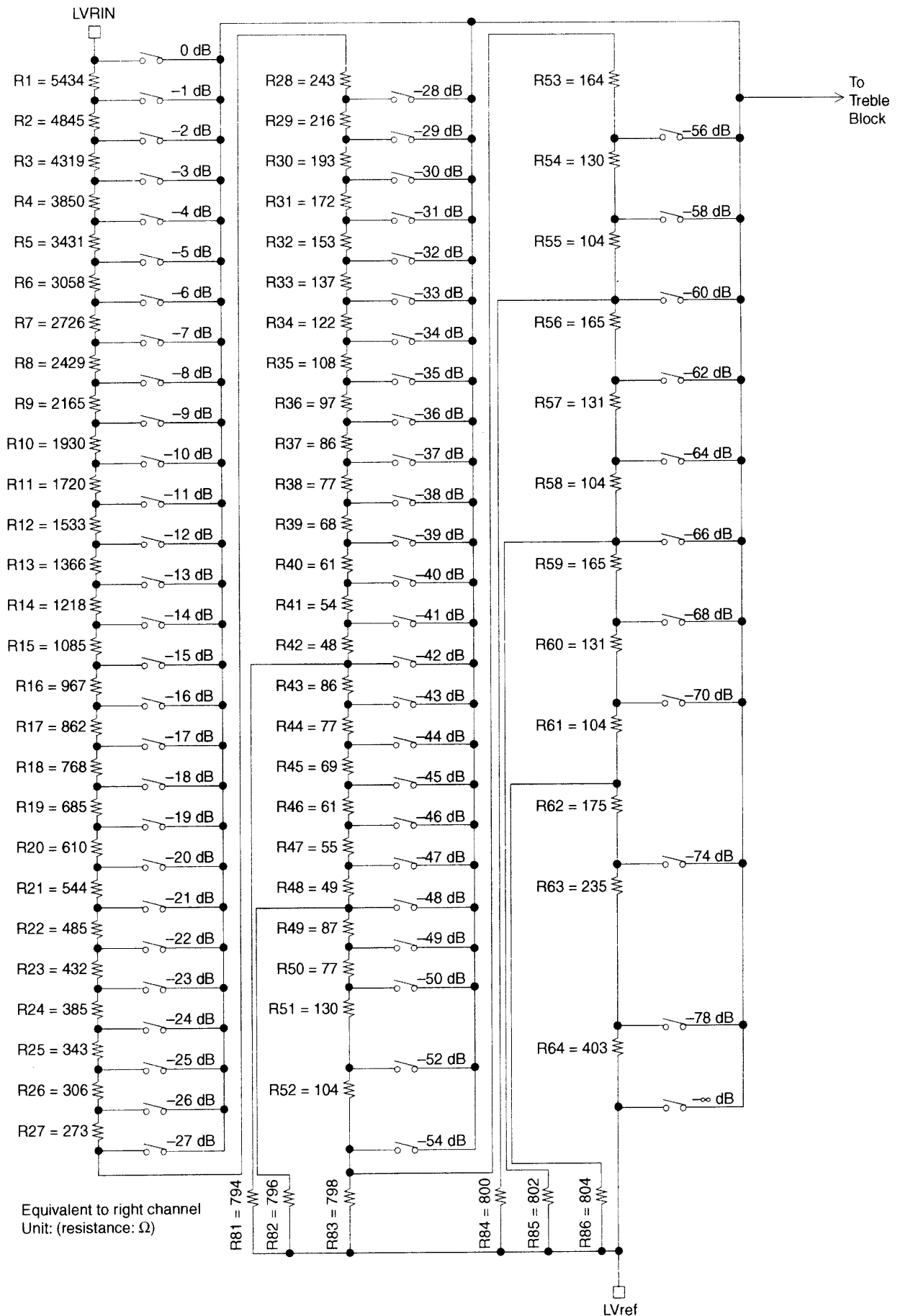


During boost, SW1 and SW3 are on, during cut, SW2 and SW4 are on, when 0 dB, 0dB SW and SW2 and SW3 are on.

SW3, SW4 of super bass block are always off.

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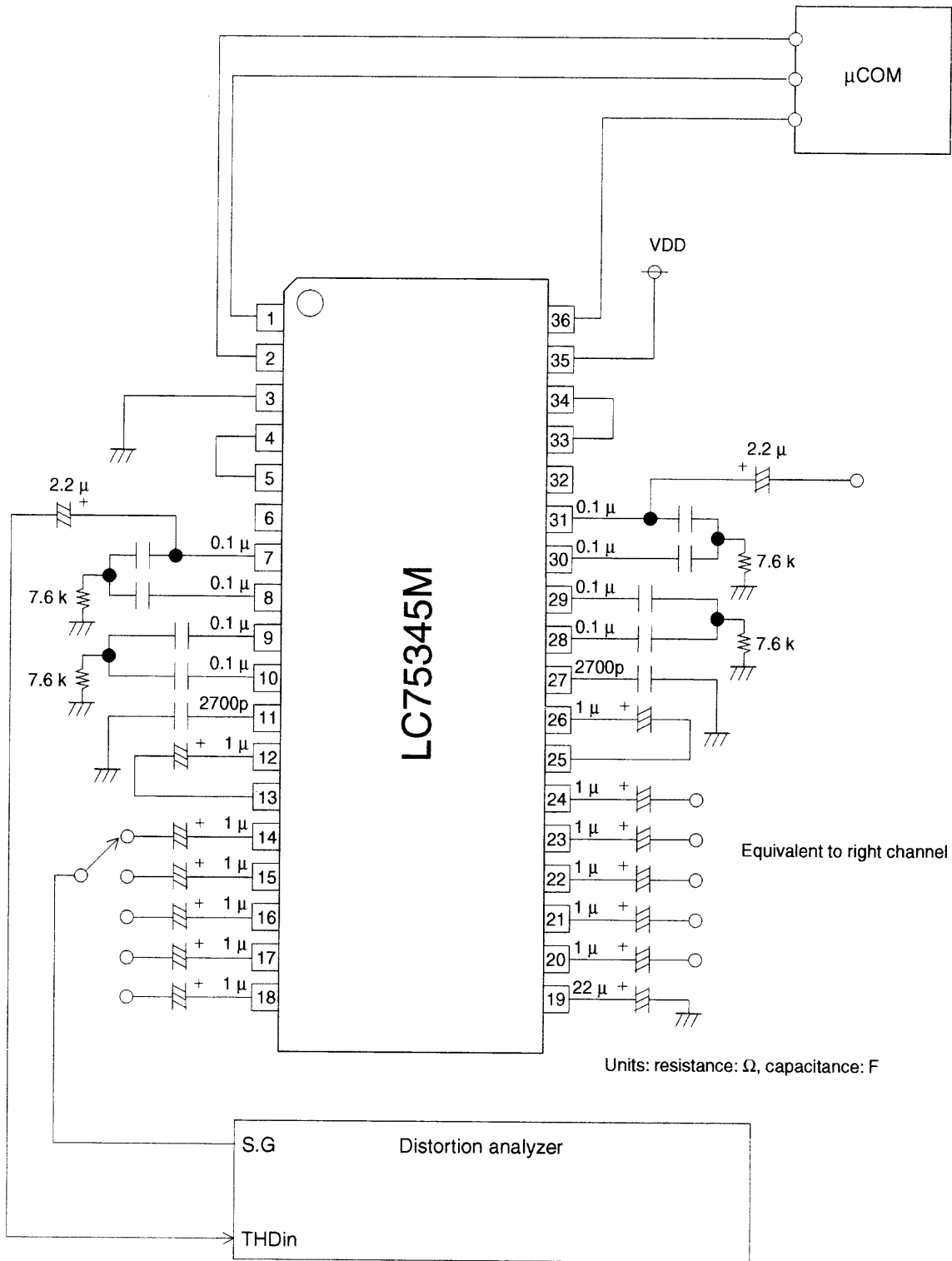
• Volume Block



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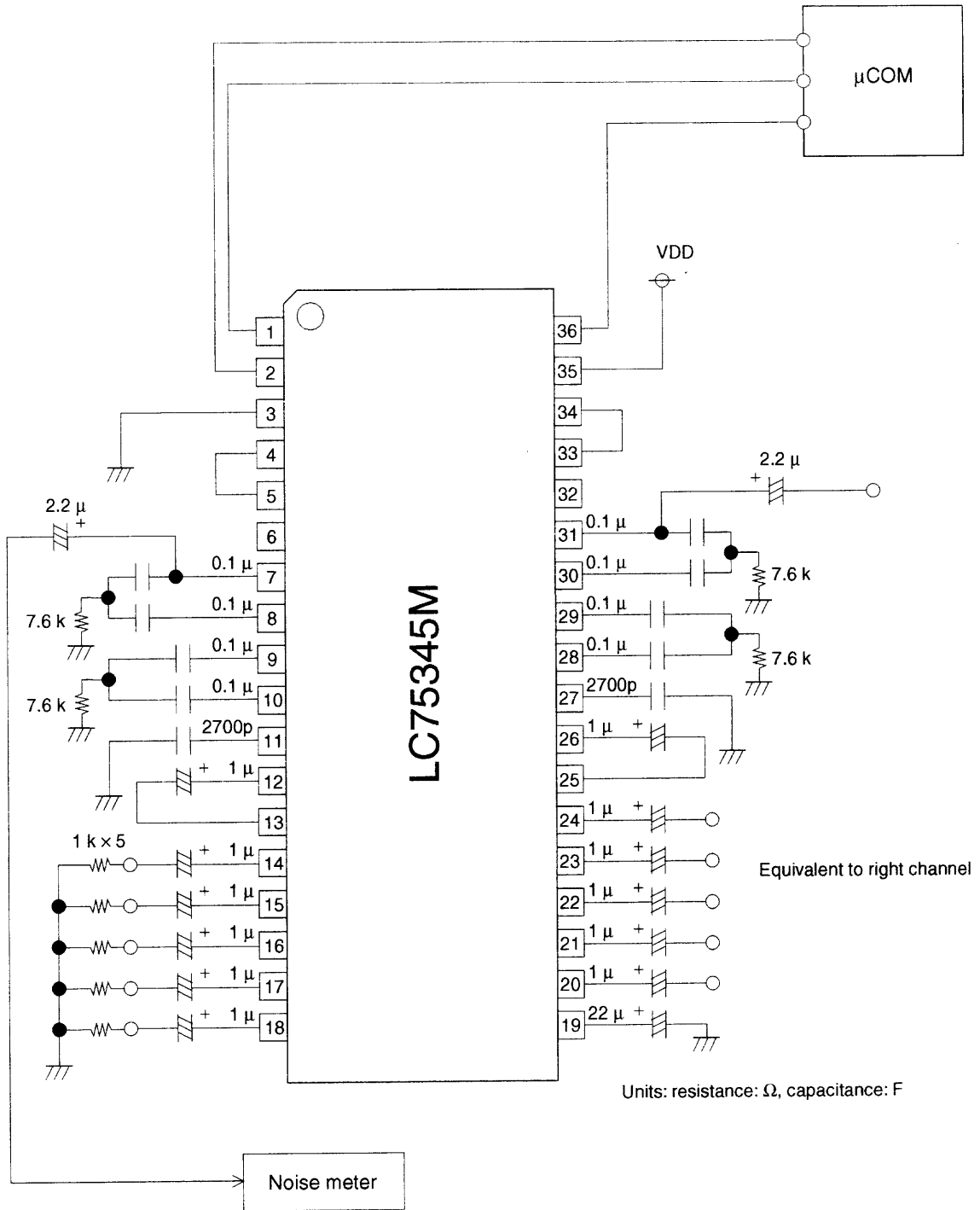
Test Circuit

- Total Harmonic Distortion



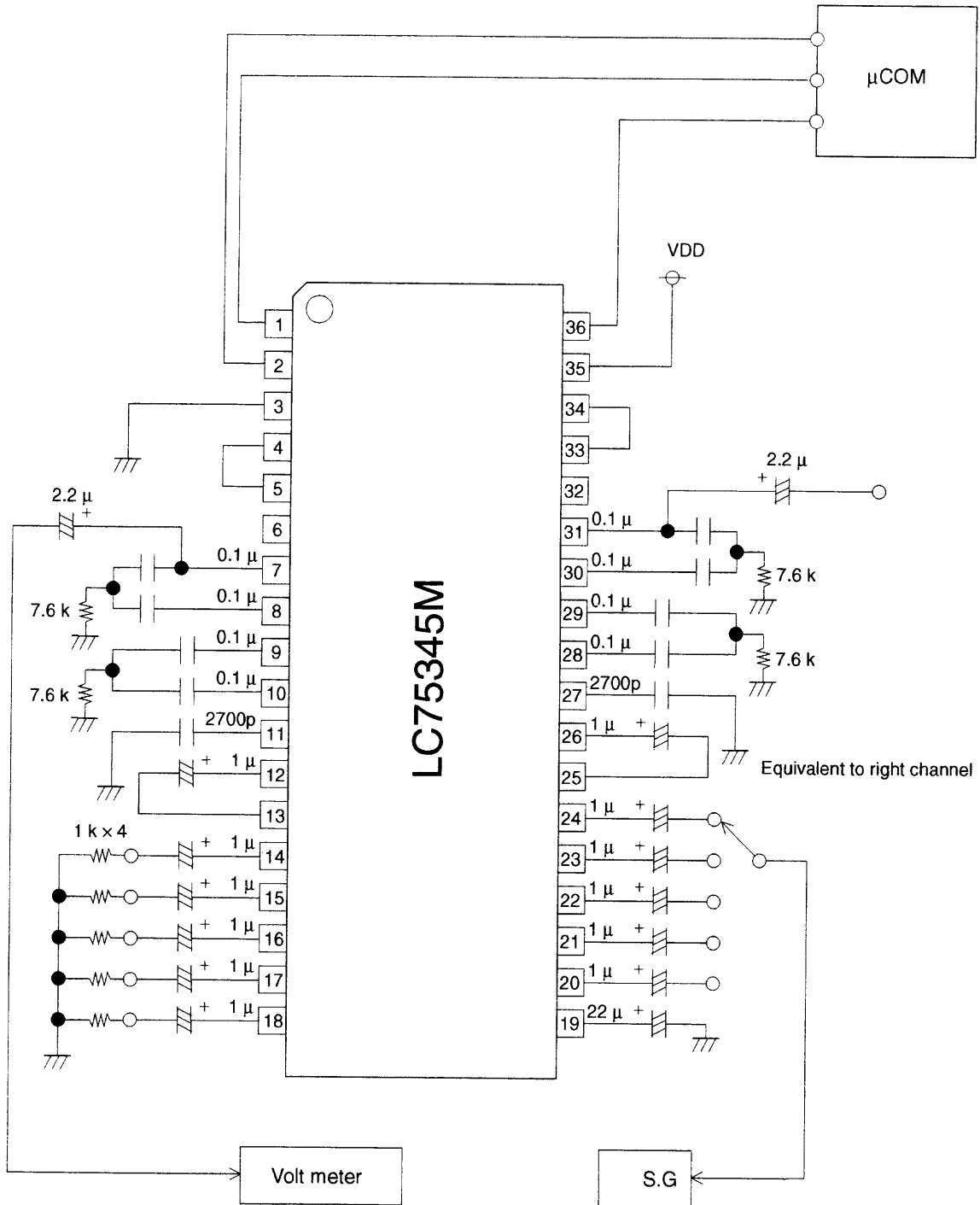
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• Output Noise Voltage



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• Crosstalk



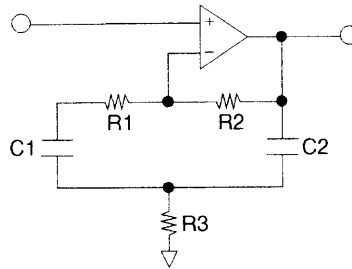
Units: resistance: Ω , capacitance: F

Calculation of External Equalizer Constant

Bass/Super Bass Circuit

The equivalent circuit and the formula for calculating the external RC with a mean frequency of 100 Hz are shown below.

- Bass/super bass band equivalent circuit block diagram



- Calculation example

Specification Mean frequency: $f_0 = 100 \text{ Hz}$
 Gain during maximum boost: $G = 10 \text{ dB}$
 Using $R_1 = 0$, $R_2 = 33.097 \text{ k}\Omega$, and $C_1 = C_2 = C$,

We obtain R_2 from $G = 10 \text{ dB}$.

$$G_{+10 \text{ dB}} = 20 \times \text{LOG}_{10} \left(1 + \frac{R_2}{2R_3} \right)$$

$$R_3 = \frac{R_2}{2(10^{G+10\text{dB}/20} - 1)} = \frac{33097}{2 \times (3.162 - 1)} \neq 7.6 \text{ K}\Omega$$

We obtain C from mean frequency $f_0 = 100 \text{ Hz}$.

$$f_0 = \frac{1}{2\pi \sqrt{R_3 R_2 C_1 C_2}}$$

$$C = \frac{1}{2\pi f_0 \sqrt{R_3 R_2}} = \frac{1}{2\pi \times 100 \sqrt{33097 \times 7600}} \neq 0.01 \mu F$$

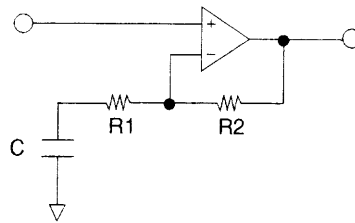
We obtain Q .

$$Q = \frac{R_3 R_2}{2R_3} \frac{1}{\sqrt{R_3 R_2}} \neq 1.04$$

Treble Band Circuit

The shelving characteristics can be obtained for the treble band.

The equivalent circuit and calculation formula during boost are indicated below.



• Calculation example

Specification Set frequency: $f = 26000 \text{ Hz}$

Gain during maximum boost: $G_{+10 \text{ dB}} = 10 \text{ dB}$

Using $R1 = 16.240 \text{ k}\Omega$ and $R2 = 35.461 \text{ k}\Omega$, and inserting the above values in the following formula, we

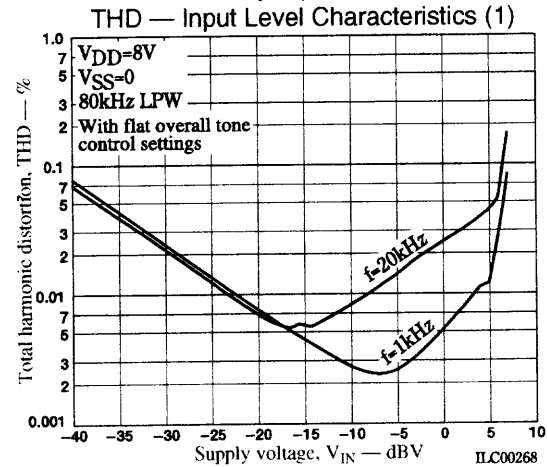
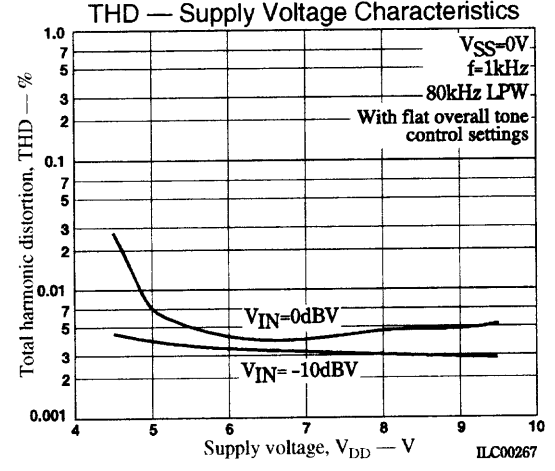
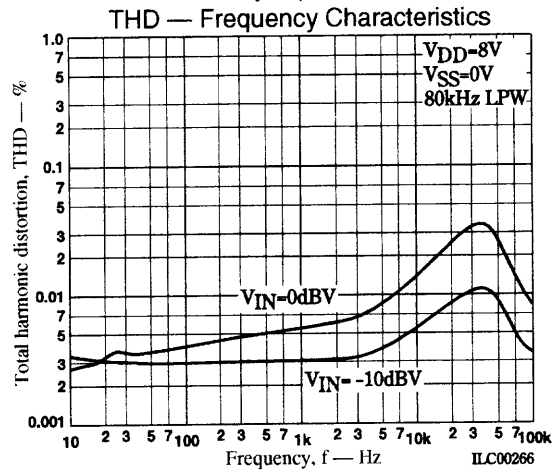
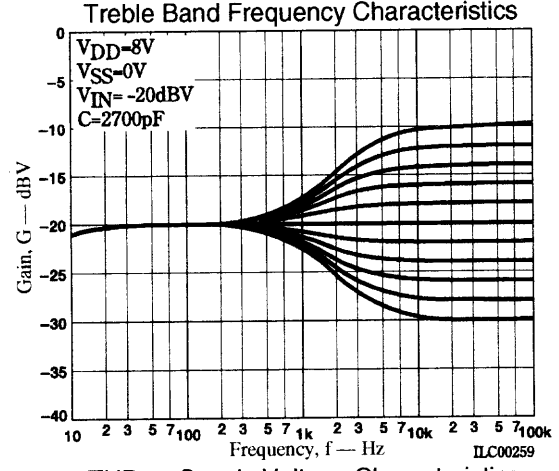
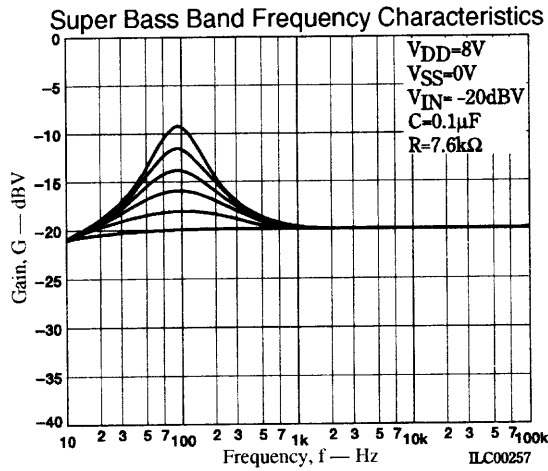
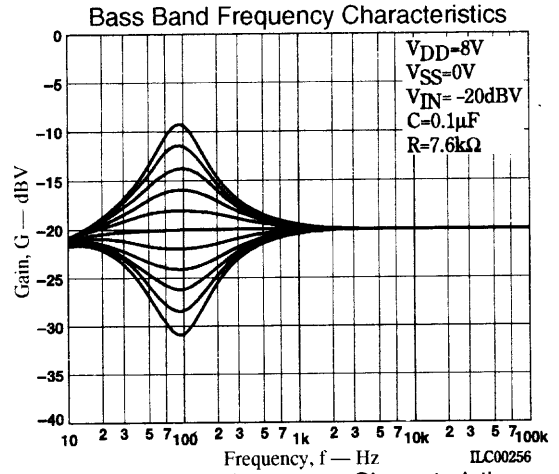
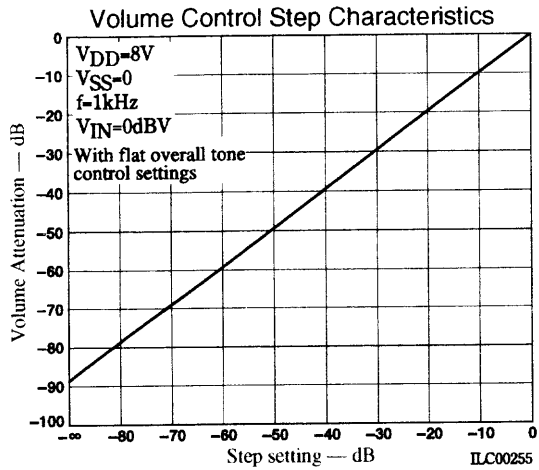
$$G = 20 \times \text{LOG}_{10} \left(1 + \frac{R2}{\sqrt{R1^2 + (1 / \omega C)^2}} \right)$$

$$C = \frac{1}{2\pi f \sqrt{\left(\frac{R2}{10^{G/20} - 1}\right)^2 - R1^2}}$$

$$= \frac{1}{2\pi 26000 \sqrt{\left(\frac{35461}{3.16 - 1}\right)^2 - 16240^2}} \approx 2700(pF)$$

Usage Cautions

- Upon power application, the internal analog switch status is undefined. Use an external countermeasure such as muting until data is set.
- When performing initial setting after applying power, send the initial setting data for the left and right channels prior to canceling mute.
- To ensure that the high-frequency digital signals sent to the CL, DI, and CE pins do not spill over to the analog signal block, either guard these signal lines with a ground pattern, or perform transmission using shielded wires.



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