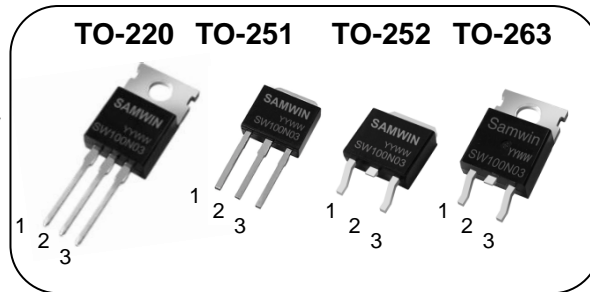


N-channel MOSFET

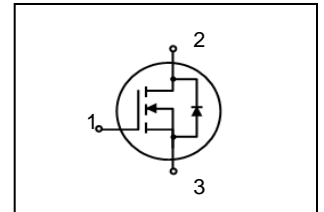
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 5.3m Ω)@ $V_{GS}=10V$
- Gate Charge (Typ 146nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS} : 30V
 I_D : 100A
 $R_{DS(ON)}$: 5.3 m Ω



General Description

This N-channel enhancement mode field-effect power transistor using SAMWIN semiconductor's advanced planar stripe, DMOS technology intended for battery Operated systems like a DC-DC converter motor control , ups ,audio amplifier. Also, especially designed to minimize $R_{DS(ON)}$, low gate charge and high rugged avalanche characteristics.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW P 100N03	SW100N03	TO-220	TUBE
2	SW I 100N03	SW100N03	TO-251	TUBE
3	SW D 100N03	SW100N03	TO-252	REEL
4	SW B 100N03	SW100N03	TO-263	REEL

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	30	V
I_D	Continuous Drain Current	100	A
I_{DM}	Drain current pulsed (note 1)	400	A
V_{GS}	Gate to Source Voltage	± 20	V
E_{AS}	Single pulsed Avalanche Energy (note 2)	875	mJ
P_D	Total power dissipation (@ $T_C=25^\circ C$)	100	W
	Derating Factor above 25 $^\circ C$	0.67	W/ $^\circ C$
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature	-55 ~ + 150	$^\circ C$
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	$^\circ C$

Thermal characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
R_{thjc}	Thermal resistance, Junction to case			1.5	$^\circ C/W$
R_{thcs}	Thermal resistance, Case to Sink		0.5		$^\circ C/W$
R_{thja}	Thermal resistance, Junction to ambient			62.5	$^\circ C/W$

Electrical characteristic ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
I_{DSS}	Drain to source leakage current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=24V, T_C=125^\circ\text{C}$	-	-	100	μA
I_{GSS}	Gate to source leakage current, forward	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
	Gate to source leakage current, reverse	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	-	3.0	V
$R_{DS(ON)}$	Drain to source on state resistance	$V_{GS}=10V, I_D = 50A$	-	4.2	5.3	m Ω
Dynamic characteristics						
C_{iss}	Input capacitance	$V_{GS}=0V, V_{DS}=15V, f=1\text{MHz}$	-	9500	-	pF
C_{oss}	Output capacitance		-	800	-	
C_{rss}	Reverse transfer capacitance		-	300	-	
$t_{d(on)}$	Turn on delay time	$V_{DS}=15V, I_D=1A, R_G=6\Omega, V_{GS}=10V$	-	25.7	50	ns
t_r	Rising time		-	10	20	
$t_{d(off)}$	Turn off delay time		-	128	200	
t_f	Fall time		-	34	70	
Q_g	Total gate charge	$V_{DS}=15V, V_{GS}=5V, I_D=16A$	-	50	65	nC
Q_{gs}	Gate-source charge		-	20.8	-	
Q_{gd}	Gate-drain charge		-	19	-	

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	90	A
V_{SD}	Diode forward voltage drop.	$I_S=110A, V_{GS}=0V$	-	-	1.5	V

※. Notes

1. Repeative rating : pulse width limited by junction temperature.
2. $L = 200\mu H, I_{AS} = 110A, V_{DD} = 25V, R_G=25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 110A, di/dt = 300A/\mu s, V_{DD} \leq BV_{DSS}, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$
5. Essentially independent of operating temperature.

Fig. 1. Output Characteristics

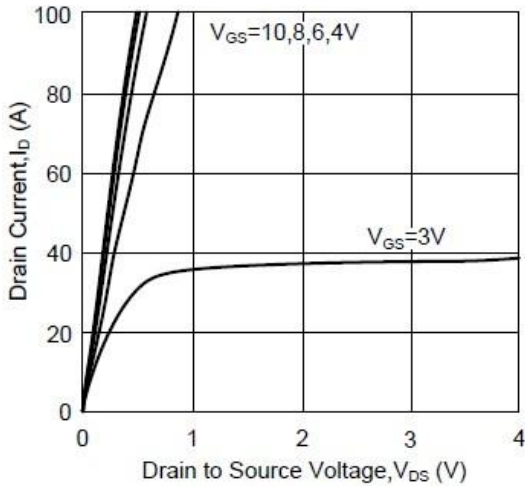


Fig. 2. Transfer characteristics

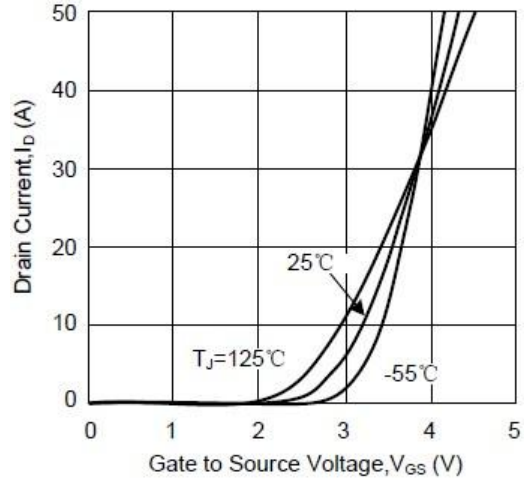


Fig. 3. On-resistance variation with Temperature

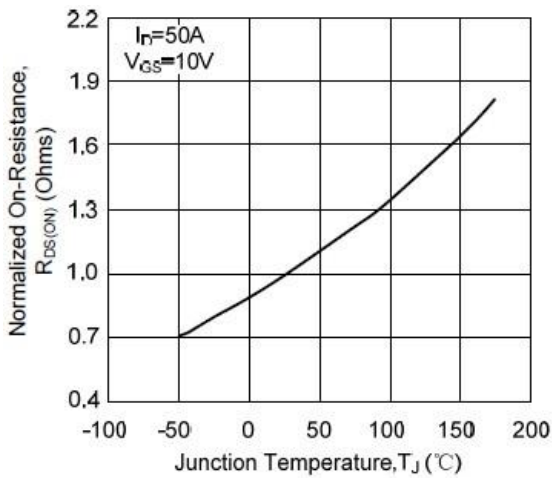


Fig. 4. Gate Threshold Variation with Temperature

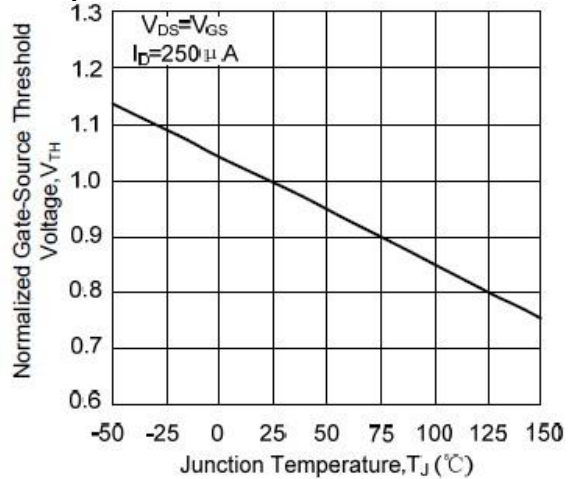


Fig. 5. Gate-Charge characteristics

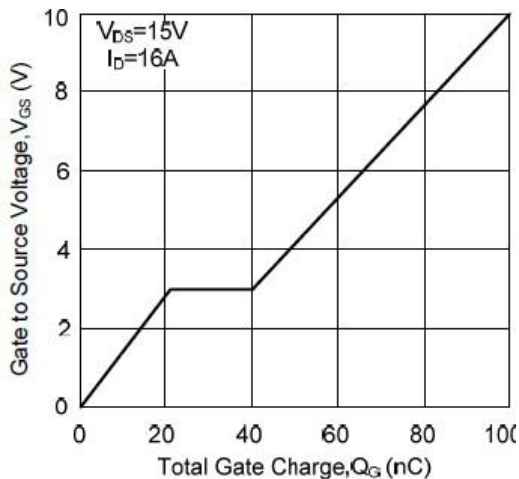


Fig. 6. Capacitance Characteristics

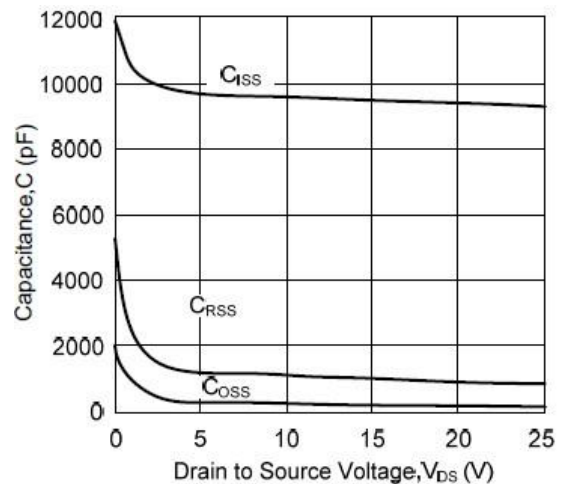


Fig 7. Body-Diode Characteristics

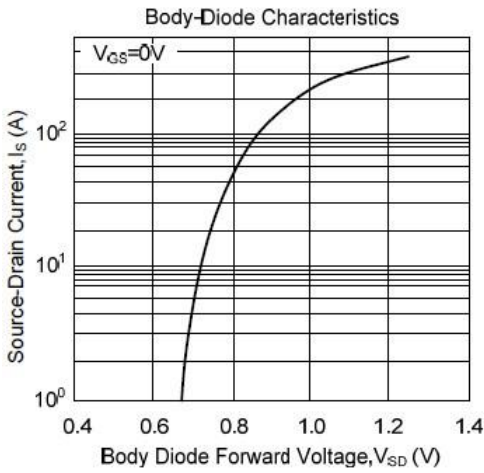


Fig. 8. Maximum Safe Operating Area

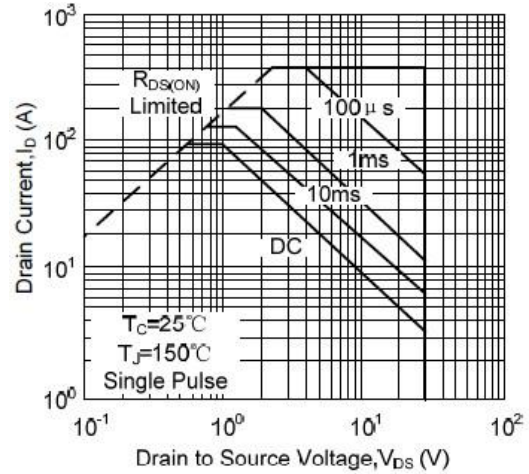


Fig. 9. Normalized Thermal Transient Impedance Curve

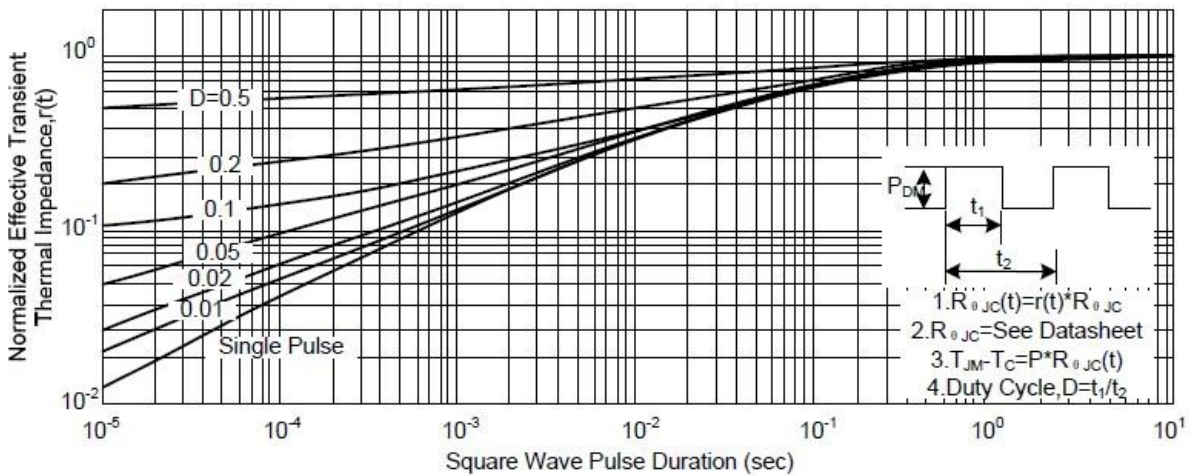
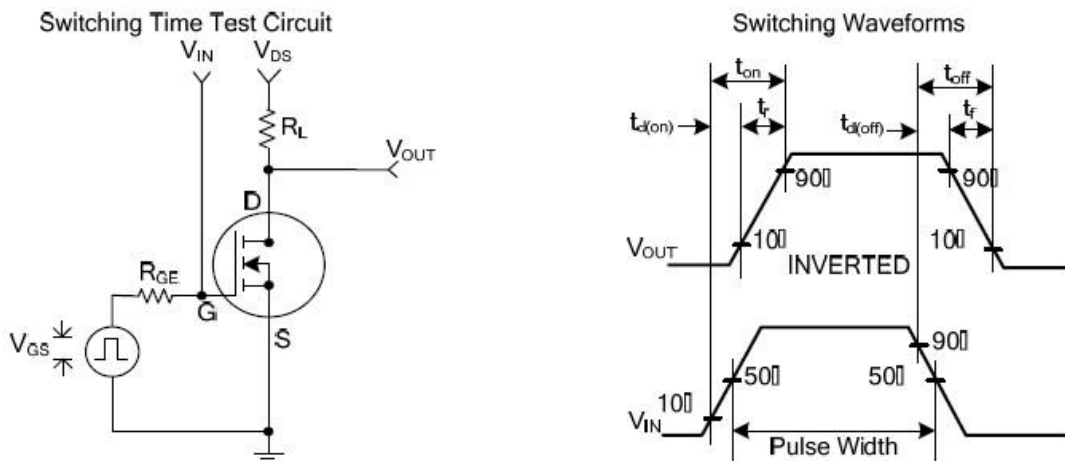


Fig.10. Test Circuit And Waveform



REVISION HISTORY

Revision No.	Changed Characteristics	Responsible	Date	Issuer
REV 1.0	Origination, First Release	Alice Nie	2010.12.05	XZQ
REV 2.0	Updated the format of datasheet and added Order Codes.	Alice Nie	2011.06.02	XZQ

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