

KMM372V320(8)0BK3 Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V320(8)0B is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V320(8)0B consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V320(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{TRAC}	t _{CAC}	t _{RC}	t _{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372V3200BK3	SOJ	4K	4K/64ms	
KMM372V3280BK3	SOJ	8K	4K/64ms	8K/64ms

Fast Page Mode Operation

CAS-before-RAS Refresh capability

RAS-only and Hidden refresh capability

LVTTL compatible inputs and outputs

Single 3.3V±0.3V power supply

JEDEC standard pinout & Buffered PDpin

Buffered input except RAS and DQ

PCB : Height(1650mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V _{ss}	29	*CAS2	57	DQ22	85	V _{ss}	113	*CAS3	141	DQ58
2	DQ0	30	RAS0	58	DQ23	86	DQ36	114	RAS1	142	DQ59
3	DQ1	31	OE0	59	V _{cc}	87	DQ37	115	RFU	143	V _{cc}
4	DQ2	32	V _{ss}	60	DQ24	88	DQ38	116	V _{ss}	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	V _{cc}	34	A2	62	RFU	90	V _{cc}	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	V _{ss}	40	V _{cc}	68	V _{ss}	96	V _{ss}	124	V _{cc}	152	V _{ss}
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	V _{ss}	71	DQ30	99	DQ47	127	V _{ss}	155	DQ66
16	DQ12	44	OE2	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	RAS2	73	V _{cc}	101	DQ49	129	RAS3	157	V _{cc}
18	V _{cc}	46	CAS4	74	DQ32	102	V _{cc}	130	CAS5	158	DQ68
19	DQ14	47	*CAS6	75	DQ33	103	DQ50	131	*CAS7	159	DQ69
20	DQ15	48	W2	76	DQ34	104	DQ51	132	PDE	160	DQ70
21	DQ16	49	V _{cc}	77	DQ35	105	DQ52	133	V _{cc}	161	DQ71
22	DQ17	50	RSVD	78	V _{ss}	106	DQ53	134	RSVD	162	V _{ss}
23	V _{ss}	51	RSVD	79	PD1	107	V _{ss}	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	V _{cc}	54	V _{ss}	82	PD7	110	V _{cc}	138	V _{ss}	166	PD8
27	W0	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	CAS0	56	DQ21	84	V _{cc}	112	CAS1	140	DQ57	168	V _{cc}

NOTE : A12 is used for only KMM372V3280BK3 (8K Ref.)

PD Note : PD & ID Terminals must each be pulled up through a register to V_{cc} at the next higher level assembly. PDs will be either open (NC) or driven to V_{ss} via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to V_{ss} without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
W0, W2	Read/Write Enable
OE0, OE2	Output Enable
RAS0 - RAS3	Row Address Strobe
CAS0, 1,4,5	Column Address Strobe
V _{cc}	Power(+3.3V)
V _{ss}	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '**' are not used in this module.

PD & ID Table

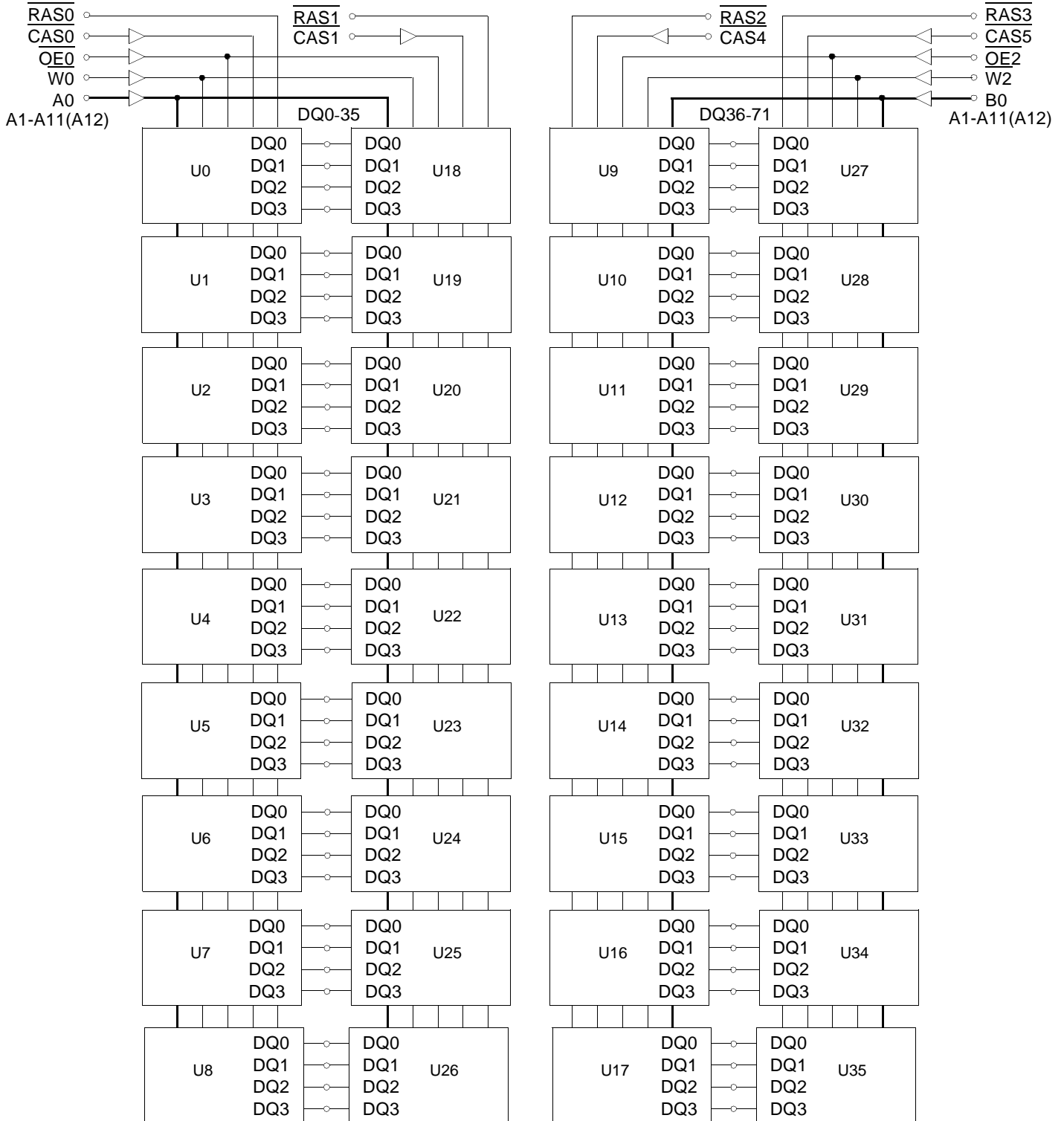
Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

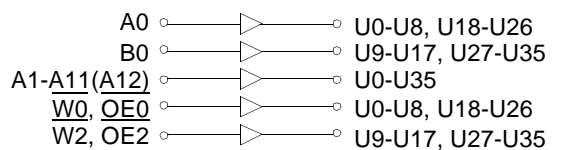
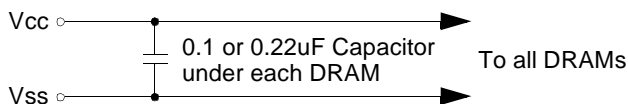
ID : 0 for V_{ss} & 1 for N.C



FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372V3280BK3(8K Ref.)



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _D	36	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V at pulse width ≤ 15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width ≤ 15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V3200BK3		KMM372V3280BK3		Unit
		Min	Max	Min	Max	
I _{CC1}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I _{CC2}	Don't care	-	100	-	100	mA
I _{CC3}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I _{CC4}	-5	-	1360	-	1180	mA
	-6	-	1180	-	1000	mA
I _{CC5}	Don't care	-	30	-	30	mA
I _{CC6}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I _{I(L)}	Don't care	-10	10	-10	10	µA
I _{O(L)}		-10	10	-10	10	µA
V _{OH}	Don't care	2.4	-	2.4	-	V
V _{OL}		-	0.4	-	0.4	V

I_{CC1}* : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)

I_{CC2}* : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{IH}$)

I_{CC3}* : RAS Only Refresh Current * ($\overline{\text{CAS}}=V_{IH}$, $\overline{\text{RAS}}$ cycling @trc=min)

I_{CC4}* : Fast Page Mode Current * ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$ cycling : t_{PC}=min)

I_{CC5}* : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{CC}-0.2V$)

I_{CC6}* : CAS-Before-RAS Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.3V$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{\text{RAS}}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	CIN1	-	20	pF
Input capacitance[W0, W2, OE0, OE2]	CIN2	-	20	pF
Input capacitance[RAS0 - RAS3]	CIN3	-	73	pF
Input capacitance[CAS0, 1, 4, 5]	CIN4	-	20	pF
Input/Output capacitance[DQ0 - 71]	CDQ	-	24	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 3.3V ± 0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il} = 2.2/0.7V, V_{oh}/V_{ol} = 2.0/0.8V, output loading CL = 100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		ns	
Read-modify-write cycle time	t _{RWC}	133		155		ns	
Access time from <u>RAS</u>	t _{RAC}		50		60	ns	3,4,10
Access time from <u>CAS</u>	t _{CAC}		18		20	ns	3,4,5,11
Access time from column address	t _{AA}		30		35	ns	3,10,11
<u>CAS</u> to output in Low-Z	t _{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t _{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t _T	1	50	1	50	ns	2
<u>RAS</u> precharge time	t _{RP}	30		40		ns	
<u>RAS</u> pulse width	t _{RAS}	50	10K	60	10K	ns	
<u>RAS</u> hold time	t _{RSH}	18		20		ns	11
<u>CAS</u> hold time	t _{CSH}	48		58		ns	11
<u>CAS</u> pulse width	t _{CAS}	13	10K	15	10K	ns	
<u>RAS</u> to <u>CAS</u> delay time	t _{RCD}	18	32	18	40	ns	4,11
<u>RAS</u> to column address delay time	t _{RAD}	13	20	13	25	ns	10,11
<u>CAS</u> to <u>RAS</u> precharge time	t _{CRP}	10		10		ns	11
Row address set-up time	t _{ASR}	5		5		ns	11
Row address hold time	t _{RAH}	8		8		ns	11
Column address set-up time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	10		10		ns	
Column address to <u>RAS</u> lead time	t _{RAL}	30		35		ns	11
Read command set-up time	t _{RCS}	0		0		ns	
Read command hold referencde to <u>CAS</u>	t _{RCH}	0		0		ns	8
Read command hold referenced to <u>RAS</u>	t _{RRH}	-2		-2		ns	8,11
Write command hold time	t _{WCH}	10		10		ns	
Write command pulse width	t _{WP}	10		10		ns	
Write command to <u>RAS</u> lead time	t _{RWL}	20		20		ns	11
Write command to <u>CAS</u> lead time	t _{CWL}	13		15		ns	
Data in set-up time	t _{DS}	-2		-2		ns	9,11
Data in hold time	t _{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t _{REF}		64		64	ms	
Write command set-up time	t _{WCS}	0		0		ns	7
<u>CAS</u> to <u>W</u> delay time	t _{CWD}	36		40		ns	7
Column address to <u>W</u> delay time	t _{AWD}	48		55		ns	7
<u>CAS</u> prechange to <u>W</u> delay time	t _{CPWD}	53		60		ns	7

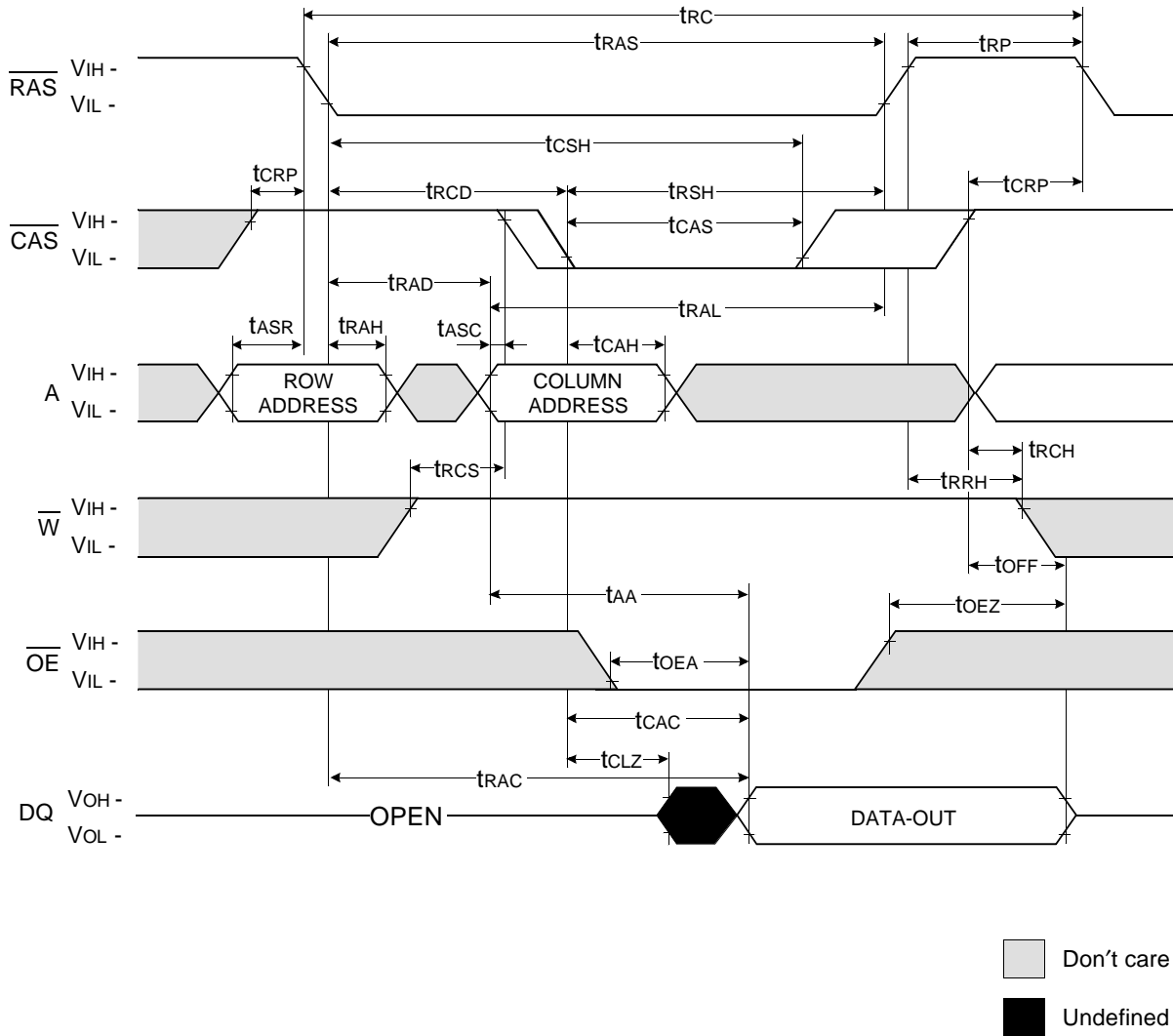
AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 3.3V ± 0.3V. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
RAS to \overline{W} delay time	t _{RWD}	71		83		ns	7,11
CAS setup time(CAS-before-RAS refresh)	t _{CSR}	10		10		ns	11
CAS hold time(CAS-before-RAS refresh)	t _{CHR}	8		8		ns	11
RAS to CAS precharge time	t _{RPC}	3		3		ns	11
Access time from CAS precharge	t _{CPA}		35		40	ns	3,11
Fast page mode cycle time	t _{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t _{PRWC}	76		85		ns	
CAS precharge time(Fast page cycle)	t _{CP}	10		10		ns	
RAS pulse width(Fast page cycle)	t _{RASP}	50	200K	60	200K	ns	
RAS hold time from CAS precharge	t _{RHCP}	35		40		ns	11
\overline{W} to RAS precharge time(C-B-R refresh)	t _{WRP}	15		15		ns	11
\overline{W} to RAS hold time(C-B-R refresh)	t _{WRH}	8		8		ns	11
\overline{OE} access time	t _{OEa}		18		20	ns	11
\overline{OE} to data delay	t _{OEaD}	18		20		ns	11
Output buffer turn off delay time from \overline{OE}	t _{OEZ}	5	18	5	20	ns	11
\overline{OE} command hold time	t _{OEh}	13		15		ns	
Present Detect Read Cycle							
\overline{PDE} to Valid PD bit	t _{PD}		10		10	ns	
\overline{PDE} to PD bit Inactive	t _{PDoff}	2	7	2	7	ns	

NOTES

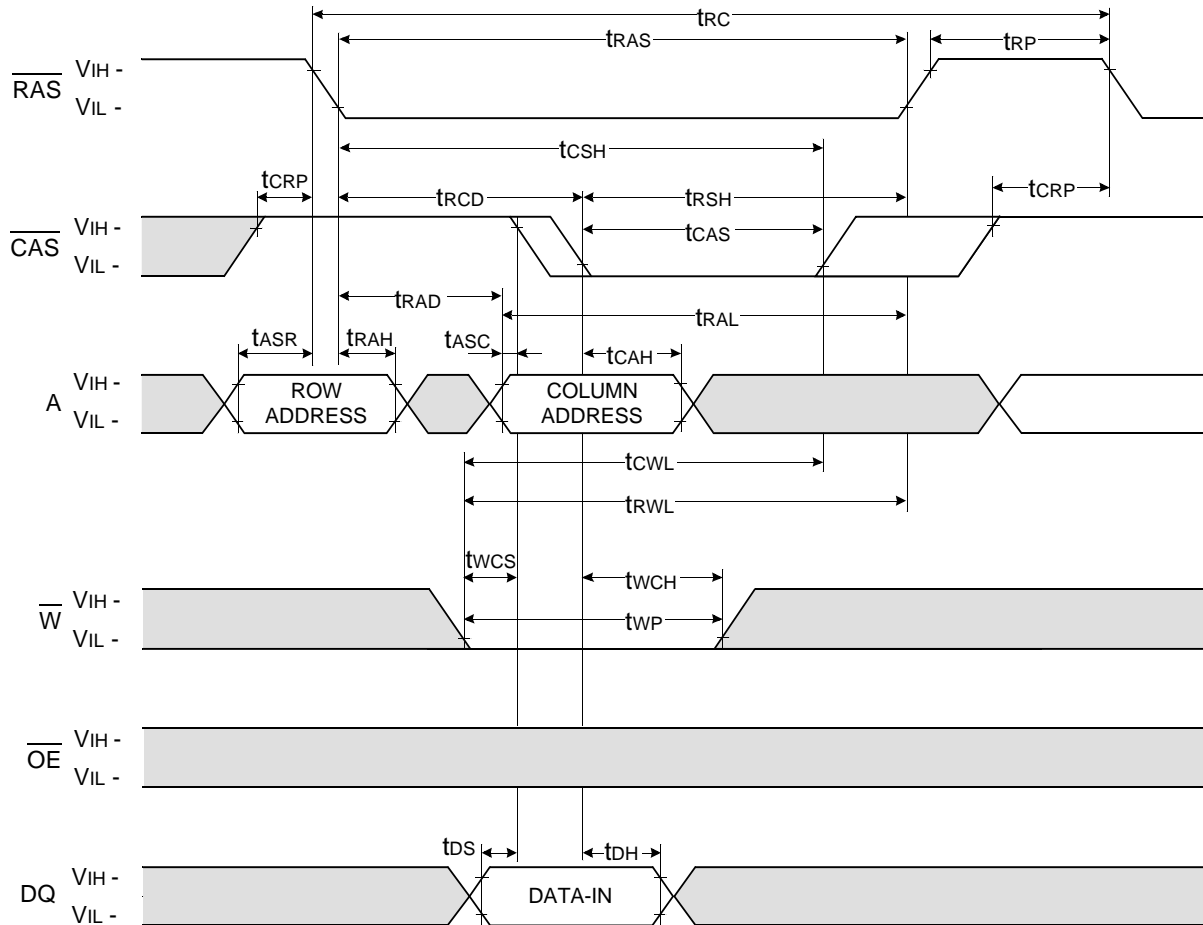
- An initial pause of 200us is required after power-up followed by any 8 \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh cycles before proper device operation is achieved.
- Input voltage levels are V_{Ih}/V_{Il}. V_{Ih}(min) and V_{Il}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{Ih}(min) and V_{Il}(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 1 TTL loads and 100pF.
- Operation within the t_{RCd}(max) limit insures that t_{RAc}(max) can be met. t_{RCd}(max) is specified as a reference point only. If t_{RCd} is greater than the specified t_{RCd}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RCd} ≥ t_{RCd}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS}(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{RWD} ≥ t_{RWD}(min), t_{CWD} ≥ t_{CWD}(min), t_{AWD} ≥ t_{AWD}(min) and t_{CPWD} ≥ t_{CPWD}(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to the \overline{CAS} leading edge in early write cycles.
- Operation within the t_{RAc}(max) limit insures that t_{RAc}(max) can be met. t_{RAc}(max) is specified as reference point only. If t_{RAc} is greater than the specified t_{RAc}(max) limit, then access time is controlled by t_{AA}.
- The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

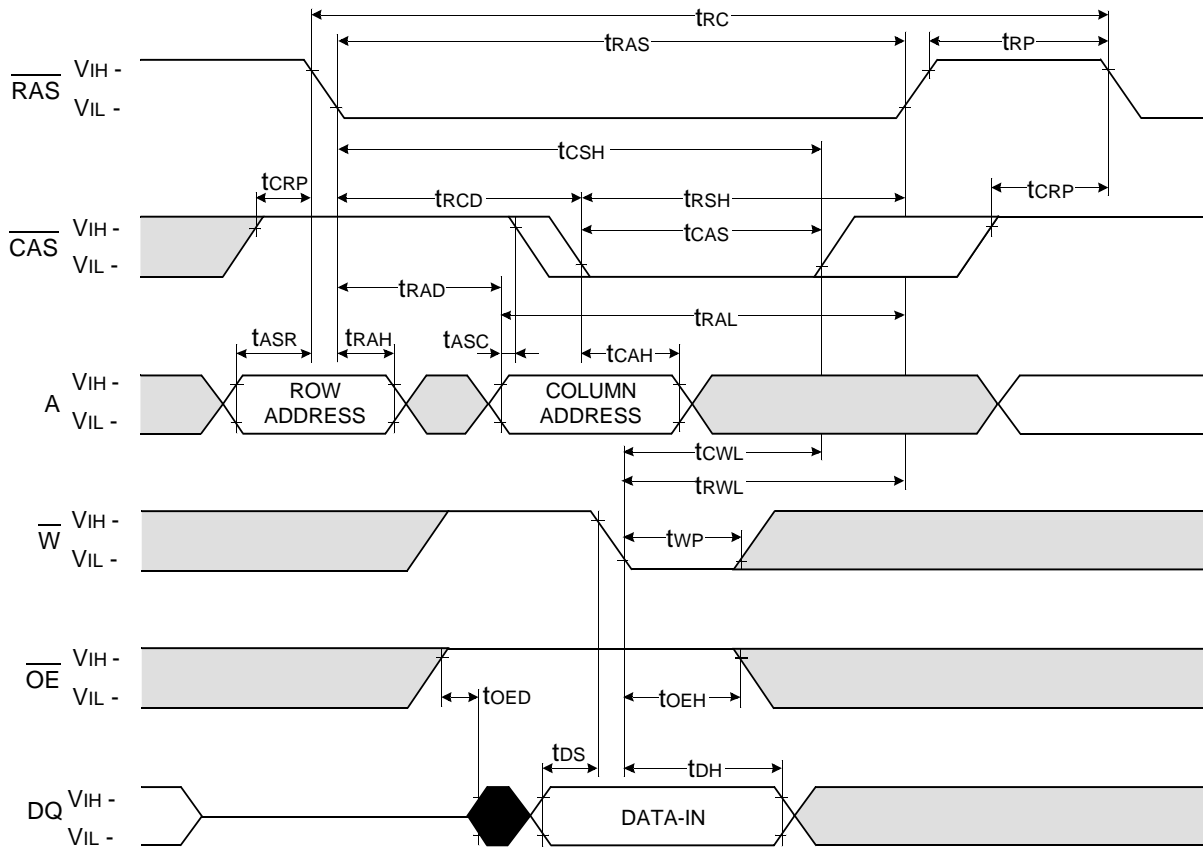


□ Don't care

■ Undefined

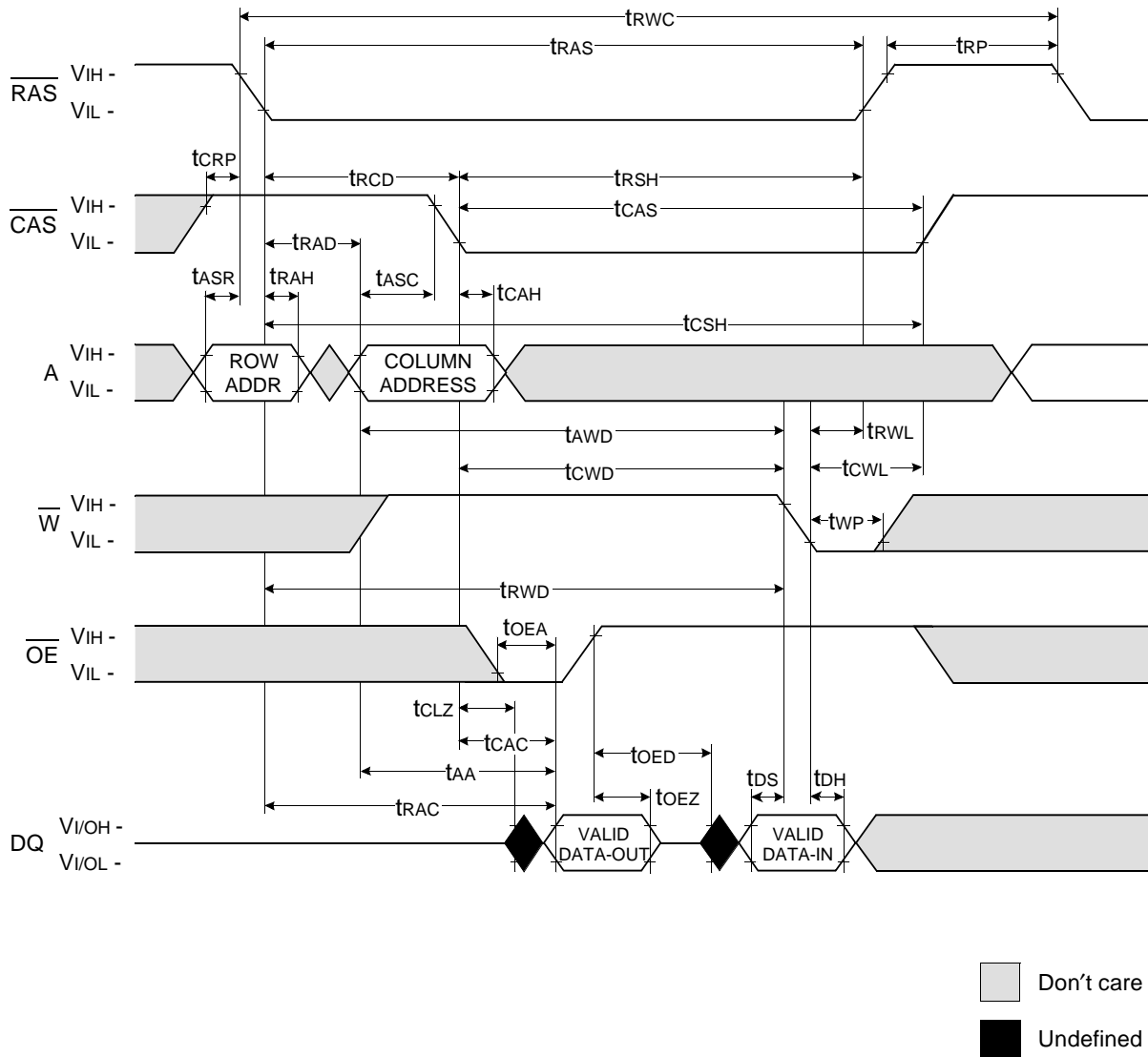
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



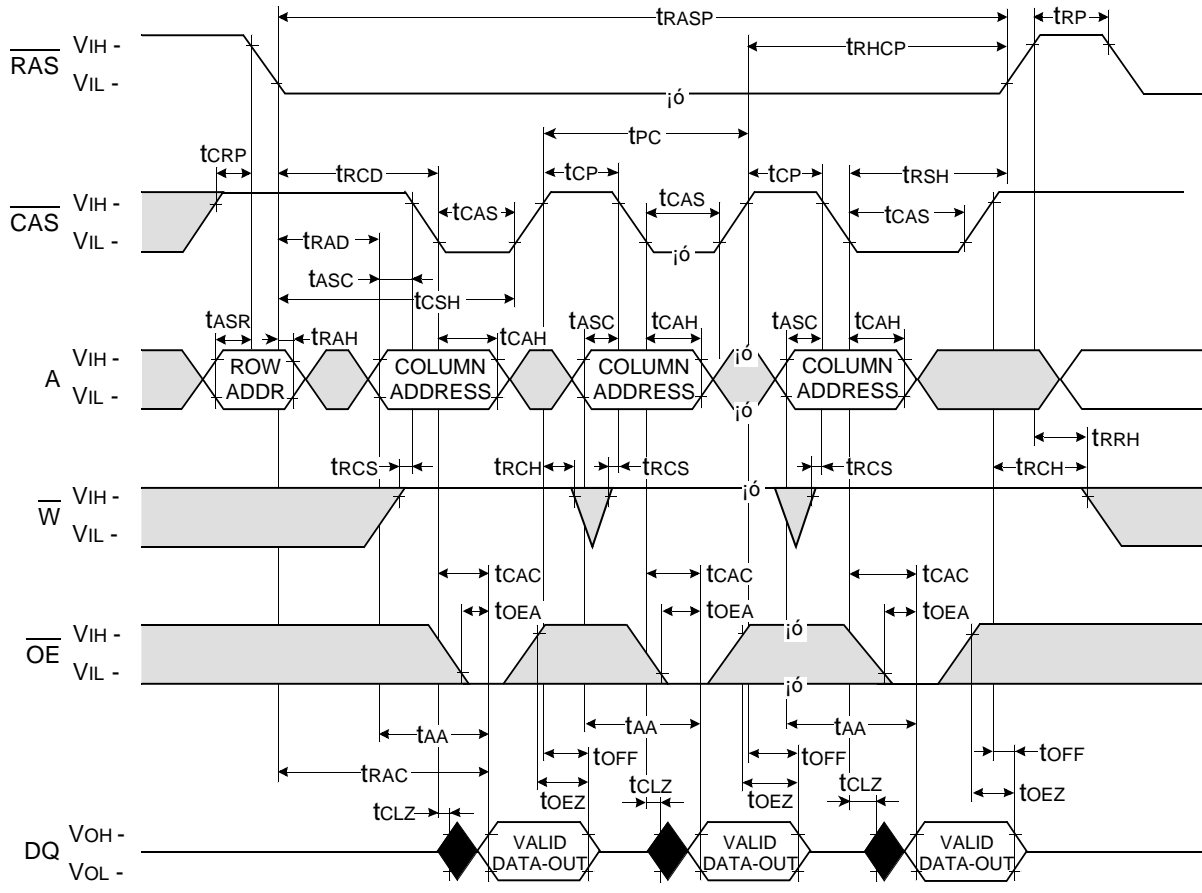
Don't care
 Undefined

READ - MODIFY - WRITE CYCLE



FAST PAGE READ CYCLE

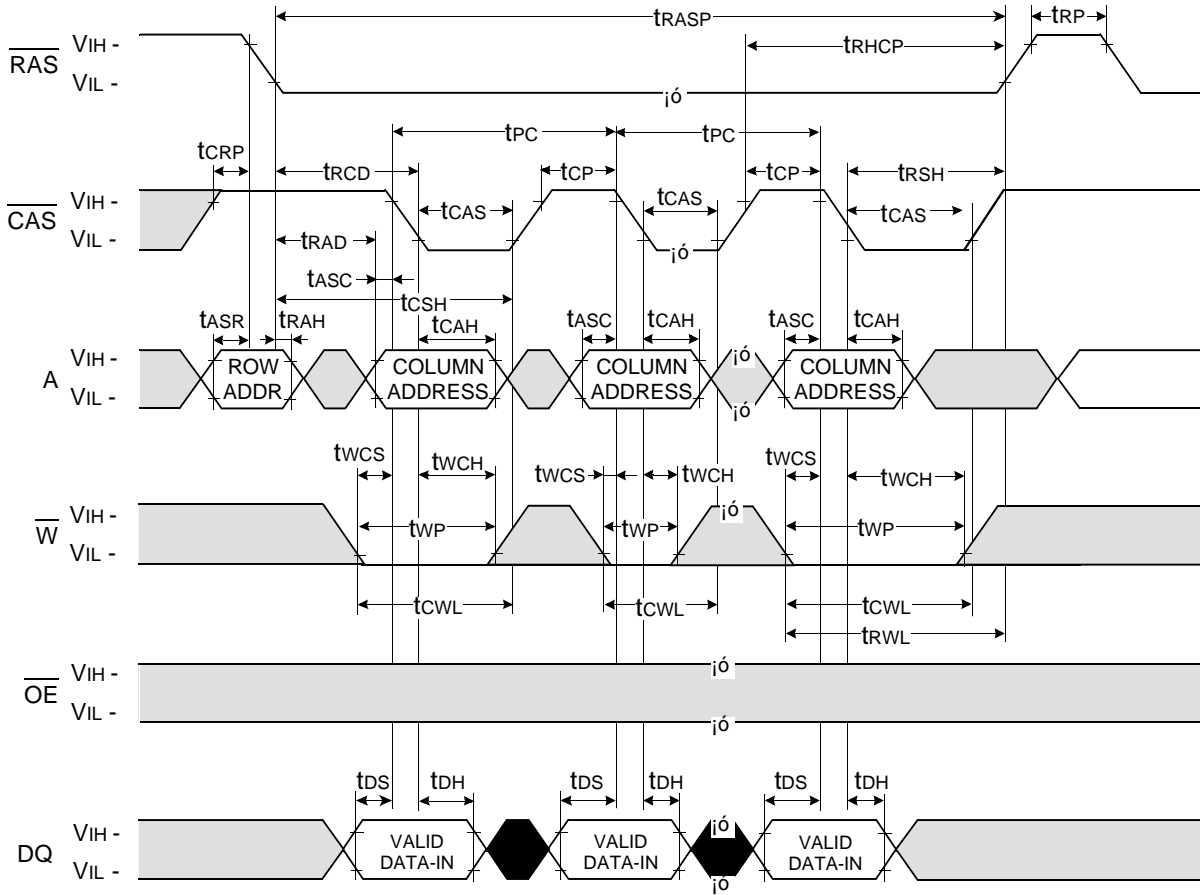
NOTE : DOUT = OPEN



Don't care
 Undefined

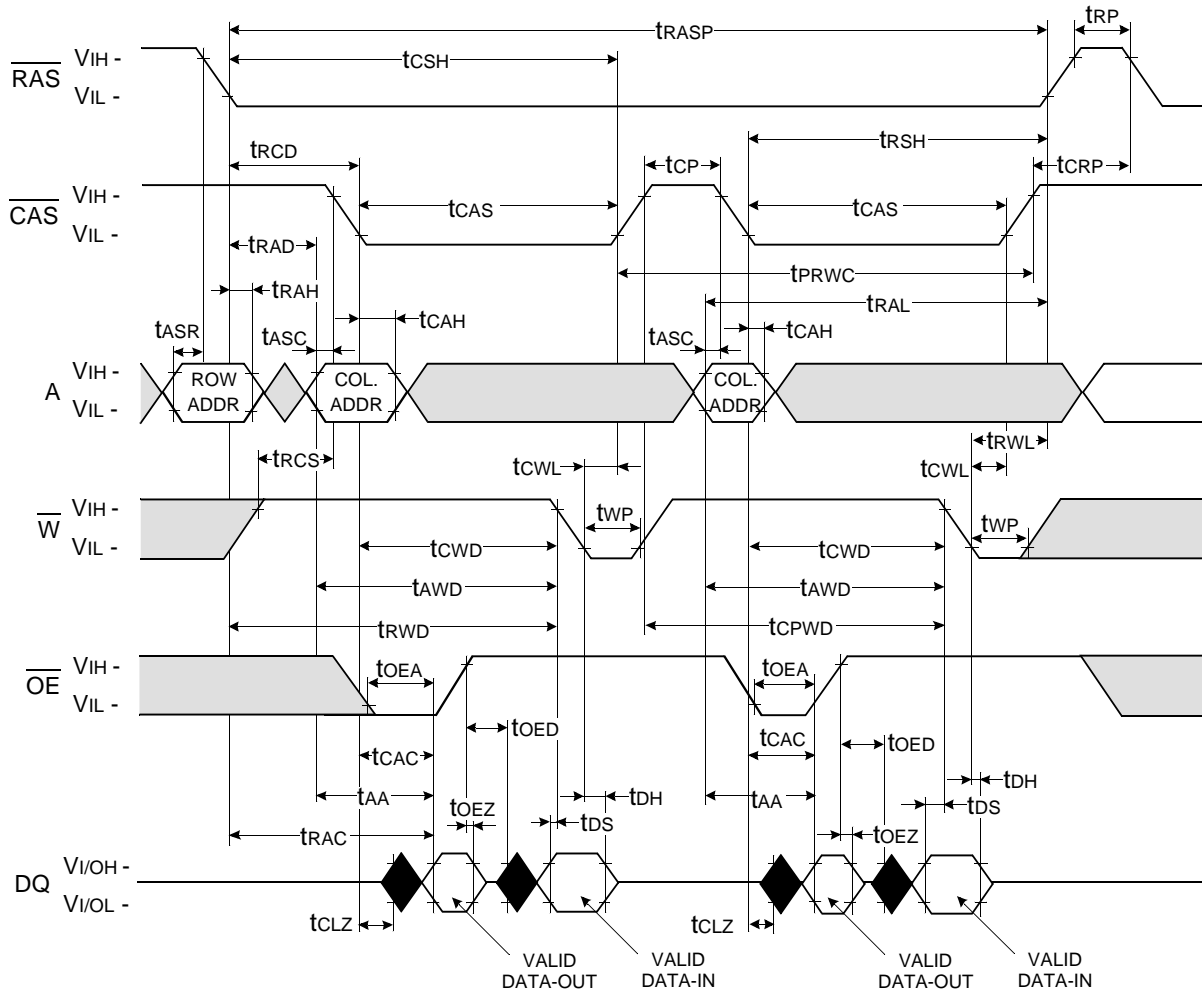
FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

FAST PAGE READ - MODIFY - WRITE CYCLE

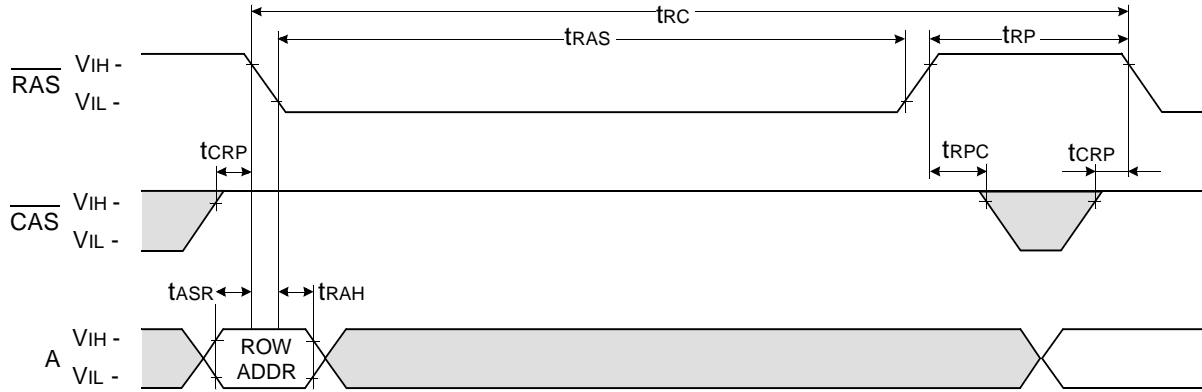


□ Don't care
■ Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

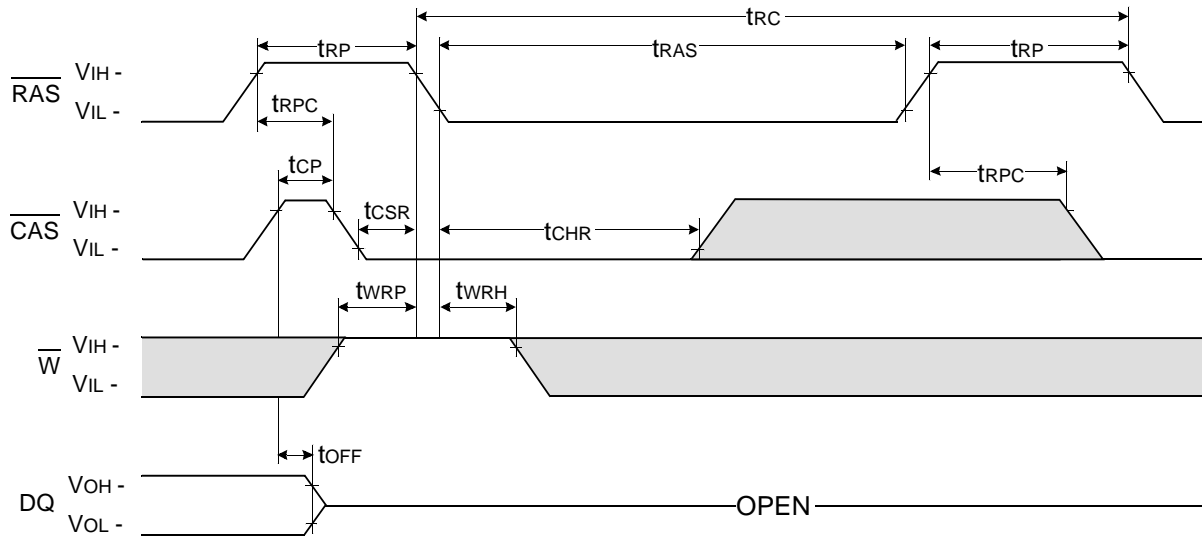
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



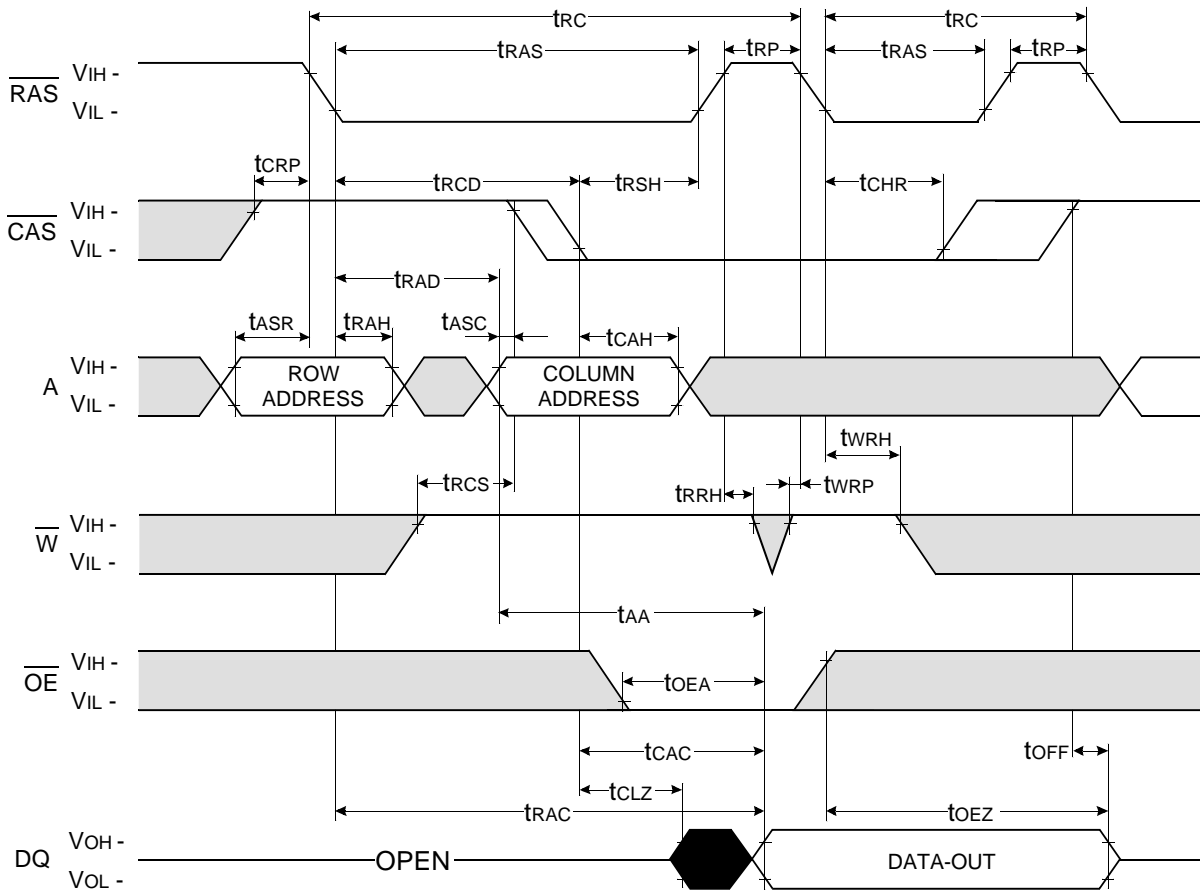
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

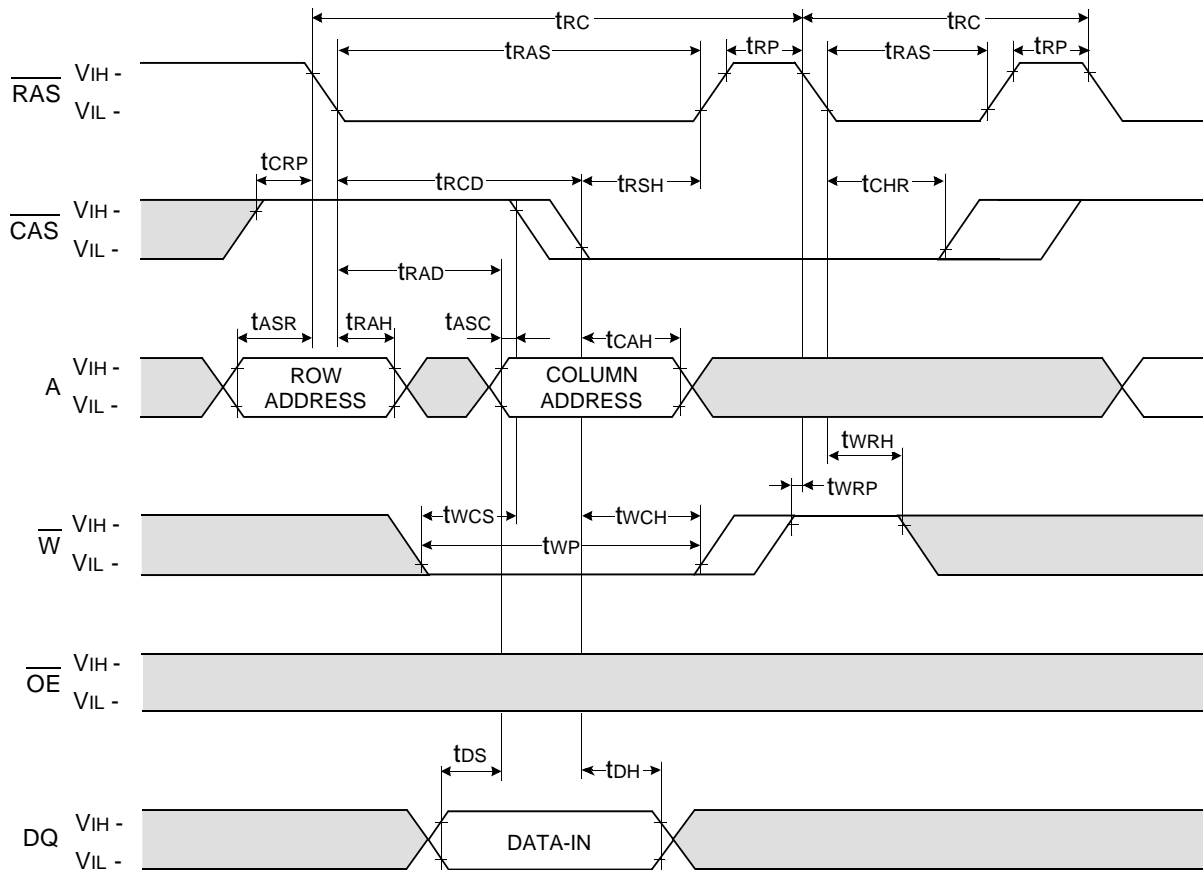
HIDDEN REFRESH CYCLE (READ)



Don't care
 Undefined

HIDDEN REFRESH CYCLE (WRITE)

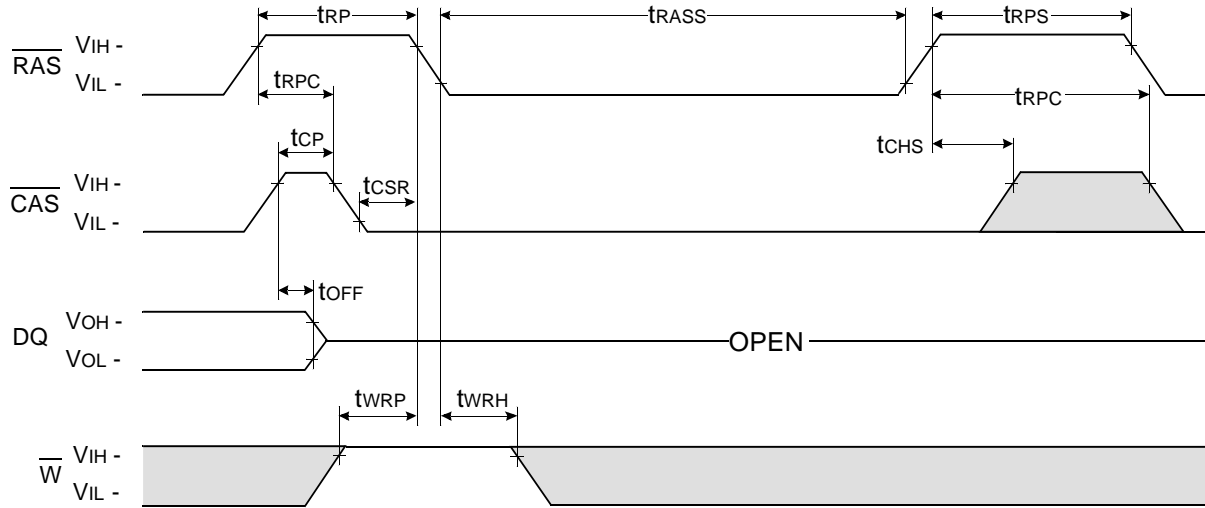
NOTE : DOUT = OPEN



Don't care
 Undefined

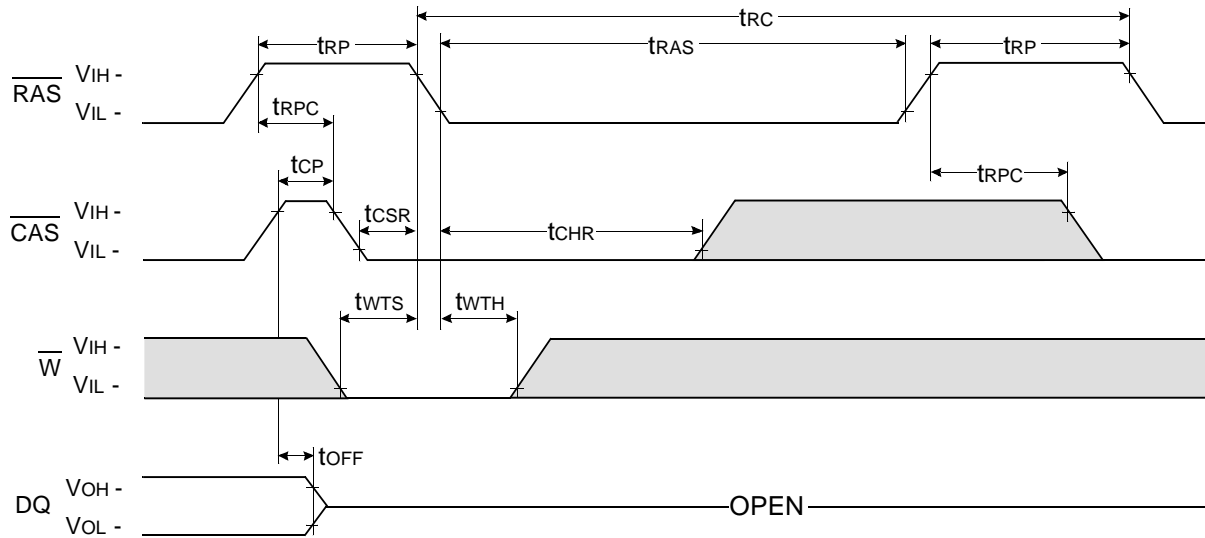
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



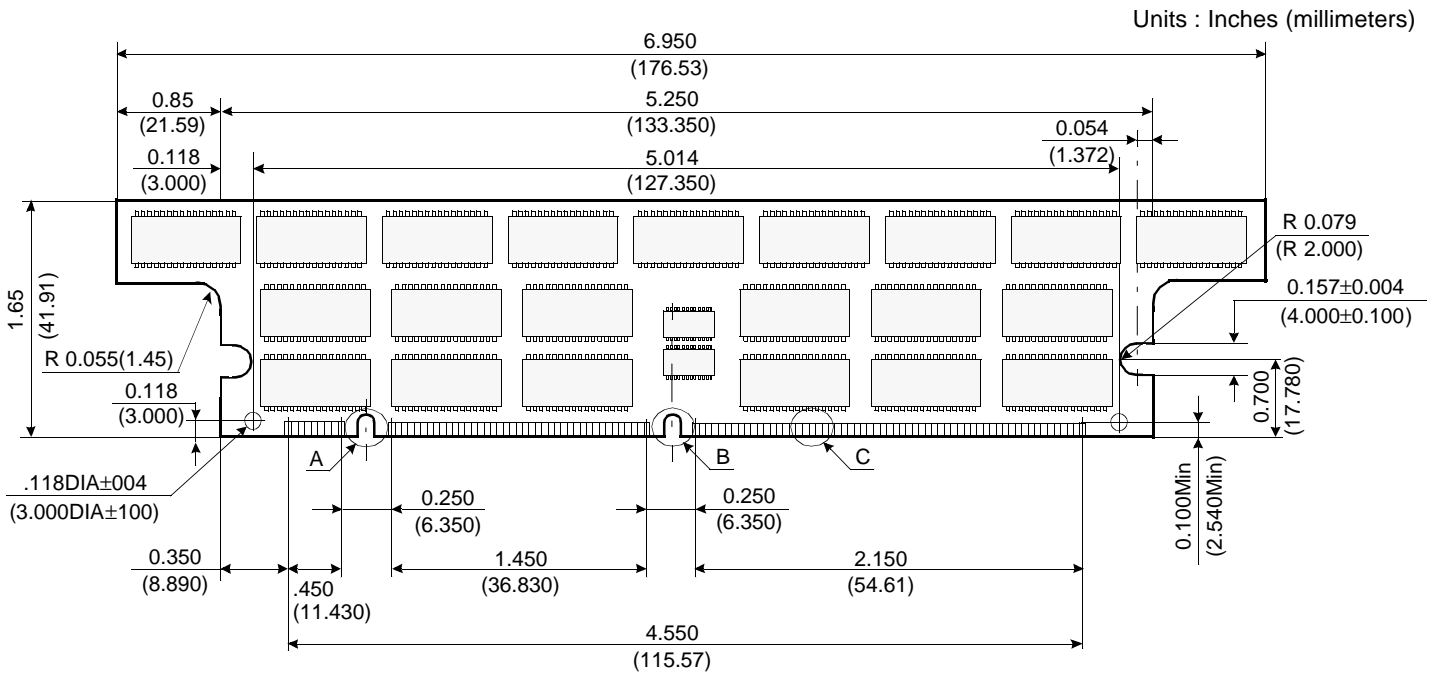
TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

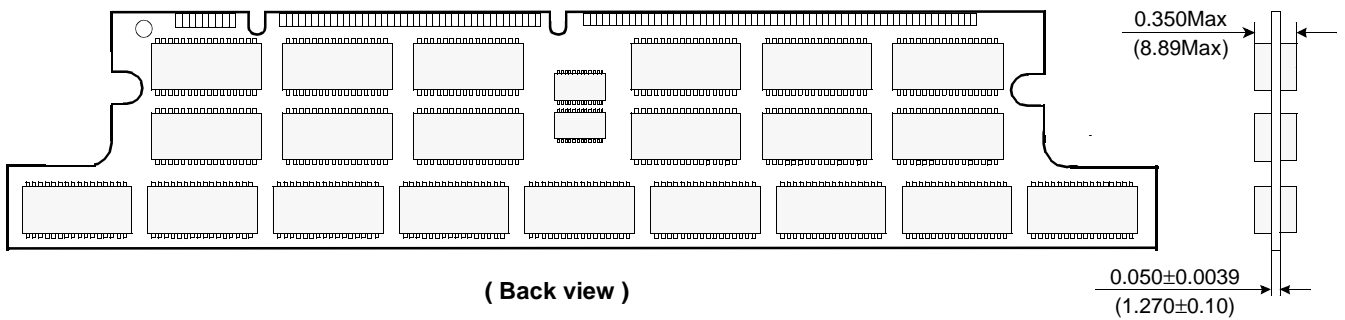


Don't care
 Undefined

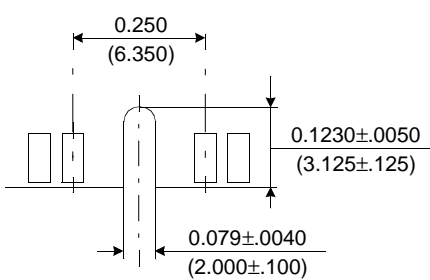
PACKAGE DIMENSIONS



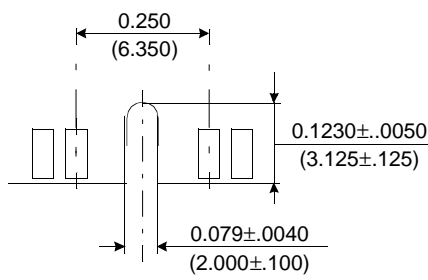
(Front view)



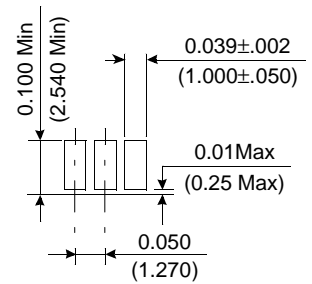
(Back view)



Detail A



Detail B



Detail C

Tolerances : ± 0.005 (.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ
 DRAM Part No. : KMM372V3200BK3 - KM44V16100BK.
 KMM372V3280BK3 - KM44V16000BK.