AMENDMENT

Am29LV004T/Am29LV004B Data Sheet

INTRODUCTION

This amendment supersedes information in the Am29LV004 data sheet, PID 20510C.

This amendment will be available online via AMD's World Wide Web site (http://www.amd.com), in addition to the literature ordering hotline. All changes contained in this document will be included in the next release of the Flash Products Data Book/Handbook.

DOCUMENT ORGANIZATION

Table 1 lists the data book pages affected by this document and contains a description of changes. The remainder of this document contains the changes. The section title and page number are provided for each change. The footers also indicate the pages affected.

Table 1. Am29LV004 Data Sheet Changes

Amendment Page	Data Sheet Page	Description of Changes
3	1	**Distinctive Characteristics:** Rearranged bullets. Renamed "2.7 to 3.6 volt, extended voltage range..." to "Single power supply operation." Under "Single power supply operation" and "High performance" bullets, defined standard and extended voltage ranges and added 90 ns speed option. Combined "Advanced power management" and "Low current consumption" bullets into new "Ultra low power consumption" bullet. Under that bullet, revised the typical standby and automatic sleep mode current specifications from 1 µA to 200 nA; revised read current specification from 10 mA to 2 mA/MHz. Combined "Sector protection" and "Flexible sector architecture" bullets. Under flexible sector architecture bullet, added temporary sector unprotect feature description. Combined Embedded Program and Embedded Erase bullets under new "Embedded Algorithms" bullet; removed ™ designations. Clarified descriptions of sector protection, erase suspend/resume, hardware reset pin, ready/busy pin, and data polling and toggle bits. **General Description:** Added text on new speed option and voltage range in second paragraph.
4	3	**Product Selector Guide:** Added -90R voltage range and speed option.
4	5	**Pin Configuration:** Added new voltage range for -90R to V_{CC} specification.
5	6	**Ordering Information, Standard Products:** The -90R speed option is now listed in the example. Revised "Speed Option" section to indicate both voltage ranges. *Valid Combinations:* Added -90R speed option and voltage range.
6	8	**Automatic Sleep Mode:** Revised addresses stable time to 200 ns and current draw to 200 nA.

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Table 1. Am29LV004 Data Sheet Changes (Continued)

Amend-ment Page	Data Sheet Page	Description of Changes
6	11	**Table 5, Command Definitions:** Grouped address designators PA, PD, RA, RD, and SA under the legend heading. Modified SA definition to accommodate the sector protect verify command. Since unlock addresses only require address bits A0–A10 to be valid, the number of hexadecimal digits in the unlock addresses were changed from four to three. The remaining upper address bits are don't care. Removed "H" designation from hexadecimal values in table and replaced with new Note 1. Revised Notes 5 and 6 to indicate when commands are valid; are now Notes 4 and 5. Expanded autoselect section to show each function separately: manufacturer ID, device ID, and sector protect verify. Added note 3 to explain sector protect codes. In Note 8, changed A13 to A11, added "unless otherwise noted"; is now new Note 6.
7	16	**$\overline{\text{RESET}}$: Hardware Reset Pin:** Fourth paragraph: Revised standby mode specification to 200 nA.
7	23	**Operating Ranges:** *V_{CC} Supply Voltages:* Added 3.0 to 3.6 V voltage range and -90R speed option.
8	24	**DC Characteristics:** *CMOS Compatible:* Changed I_{CC1} from 30 mA maximum at 6 MHz to 16 mA maximum at 5 MHz and 4 mA maximum at 1 MHz. Changed I_{CC2} from 35 mA to 30 mA maximum. In the V_{OL} specification, changed the I_{OL} test condition from 5.8 mA to 4.0 mA. In Note 1, changed 6 MHz to 5 MHz. In Note 3, changed address stable time from 300 ns to 200 ns; changed typical automatic sleep mode current from 1 µA to 200 nA.
9	24A	**Figure 8A, I_{CC} Current vs. Time, and Figure 8B, I_{CC} vs. Frequency:** Figure 8A illustrates current draw during the Automatic Sleep Mode after the addresses are stable. Figure 8B shows how frequency affects the current draw curves for both voltage ranges.
10	25	**AC Characteristics:** *Read Only Operations Characteristics:* Added -90R column. **Test Conditions, Figure 9:** Added 90 ns speed to C_L note.
11	26	**AC Characteristics:** *Write/Erase/Program Operations:* Added the -90R column.
12	28	**Figure 13, AC Waveforms for Program Operations:** Changed 5555H to 555H in addresses waveform to match command definitions (Table 5).
12	29	**Figure 14, AC Waveforms for Chip/Sector Erase Operations:** Changed 5555H to 555H in addresses waveform to match command definitions (Table 5).
13	31	**Figure 19, Temporary Sector Unprotect Diagram:** Corrected callouts on $\overline{\text{RESET}}$ waveform to "0 V or 3 V".
13	32	**AC Characteristics:** *Alternate $\overline{CE}$ Controlled Writes:* Added the -90R column. Changed t_{AH} from 45 to 50 ns for -100, from 50 to 65 ns for -150. Changed t_{DS} from 50 to 65 ns for -150. Changed t_{CP} from 45 to 50 ns for -100, from 50 to 65 ns for -150. Changed t_{CPH} from 20 to 30 ns for -100, -120; from 20 to 35 ns for -150.
14	33	**Figure 20, Alternate $\overline{\text{CE}}$ Controlled Write Operation Timings:** Changed 5555H to 555H in addresses waveform to match command definitions (Table 5).
15	34	**Erase and Programming Performance:** Added typical chip erase specification. Renamed erase/program cycles specification to erase/program endurance. Corrected to indicate 1,000,000 cycle endurance is typical, not maximum, and that 100,000 cycle endurance is minimum, not typical. Revised Note 1 to include write endurance; moved Note 1 references in table to table head. Consolidated and moved Note 1 and Note 3 references in table to table head. Combined Note 2 and Note 5 into new Note 1, which applies to the entire table; revised to indicate that DQ5=1 after any maximum time. Comments for program and erase now straddle parameter rows. Separated the two sentences in Note 4 into new Notes 4 and 5; added corresponding note references to comment section.

PRELIMINARY

AMD

Am29LV004T/Am29LV004B

4 Megabit (524,288 x 8-Bit) CMOS 3.0 Volt-only Sector Architecture Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Extended voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Standard voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **High performance**
  - — Extended voltage range: access times as fast as 100 ns
  - — Standard voltage range: access times as fast as 90 ns
- **Ultra low power consumption**
  - — Automatic Sleep Mode: 200 nA typical
  - — Standby mode: 200 nA typical
  - — Read mode: 2 mA/MHz typical
  - — Program/erase mode: 20 mA typical
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors
  - — Supports control code and data storage on a single device
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithms automatically preprogram and erase the entire chip or any combination of designated sectors
  - — Embedded Program algorithms automatically write and verify bytes or words at specified addresses
- **Minimum 100,000 write cycle guarantee per sector**
- **Package option**
  - — 40-pin TSOP
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **$\overline{\text{Data}}$ Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/$\overline{\text{Busy}}$ pin**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase suspend/resume feature**
  - — Provides the ability to suspend the erase operation in any sector, read data from or program data to any other sector, then return to the original sector and complete the initial erase operation
- **Hardware reset pin ($\overline{\text{RESET}}$)**
  - — Hardware method to reset the device to the read mode

GENERAL DESCRIPTION (PARAGRAPH 2)

The Am29LV004 provides two levels of performance. The first level offers access times as fast as 100 ns with a V_{CC} range as low as 2.7 volts, which is optimal for battery powered applications. The second level offers a 90 ns access time, optimizing performance in systems where the power supply is in the regulated range of 3.0 to 3.6 volts. To eliminate bus contention, the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$), and output enable ($\overline{\text{OE}}$) controls.

PRODUCT SELECTOR GUIDE (PAGE 3)

Family Part Number		Am29LV004T/Am29LV004B			
Ordering Part Number:	V_{CC} = 3.0–3.6 V	**-90R**			
	V_{CC} = 2.7–3.6 V		**-100**	**-120**	**-150**
Max access time (ns)		90	100	120	150
$\overline{CE}$ access time (ns)		90	100	120	150
$\overline{OE}$ access time (ns)		40	40	50	55

PIN CONFIGURATION (PAGE 5)

A0–A18 = 19 addresses

DQ0–DQ7 = 8 data inputs/outputs

$\overline{CE}$ = Chip enable

$\overline{OE}$ = Output enable

$\overline{WE}$ = Write enable

$\overline{RESET}$ = Hardware reset pin, active low

RY/$\overline{BY}$ = Ready/$\overline{Busy}$ output

V_{CC} = Standard voltage range
(3.0 V to 3.6 V) for -90R

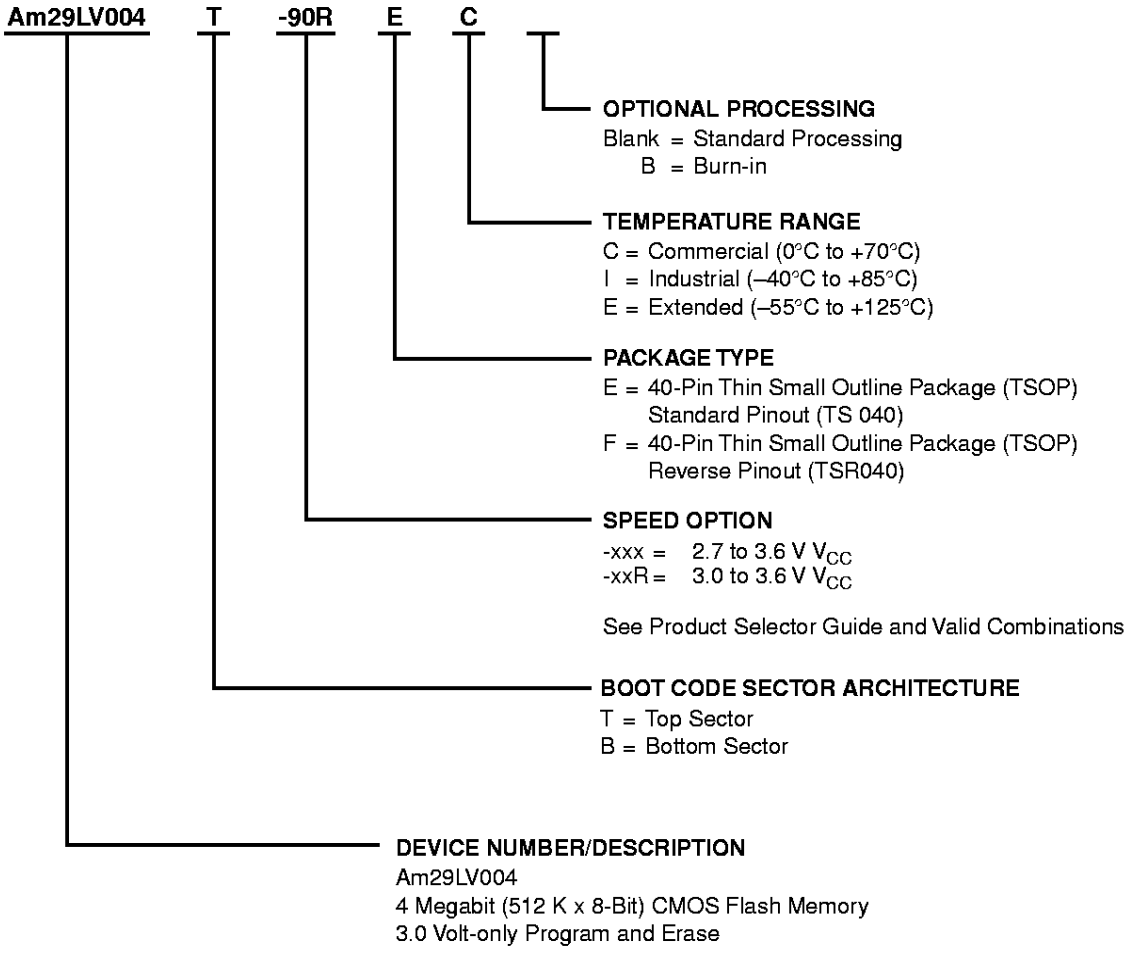
Extended voltage range
(2.7 to 3.6 V) for -100, -120, -150

V_{SS} = Device ground

NC = Pin not connected internally

ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29LV004T-90R, Am29LV004B-90R V_{CC} = 3.0–3.6 V	EC, EI, FC, FI
Am29LV004T-100, Am29LV004B-100	EC, EI, EE, EEB, FC, FI, FE, FEB
Am29LV004T-120, Am29LV004B-120	
Am29LV004T-150, Am29LV004B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

USER BUS OPERATIONS (PAGE 8)

Automatic Sleep Mode

Advanced power management features such as the automatic sleep mode minimize Flash device energy consumption. This is extremely important in battery-powered applications. The Am29LV004 automatically enables the low-power, automatic sleep mode when addresses remain stable for 200 ns. Automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ control signals. Typical sleep mode current draw is 200 nA (for CMOS-compatible operation). Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

TABLE 5, COMMAND DEFINITIONS (PAGE 11)

Table 5. Am29LV004 Command Definitions

Command Sequence Read/Reset (Note 2)	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Read/Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset/Read	1	XXX	F0	RA	RD								
Autoselect Manufacturer ID	3	555	AA	2AA	55	555	90	X00	01				
Autoselect Device ID (Top Boot Block)	3	555	AA	2AA	55	555	90	X01	B5				
Autoselect Device ID (Bottom Boot Block)	3	555	AA	2AA	55	555	90	X01	B6				
Autoselect Sector Protect Verify (Note 3)	3	555	AA	2AA	55	555	90	SA X02	00				
									01				
Byte Program	4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 4)	1	XXX	B0										
Erase Resume (Note 5)	1	XXX	30										

Legend:

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse.

PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ pulse.

SA = Address of the sector to be erased or verified. Address bits A18–A13 uniquely select any sector.

Notes:

1. *All values are in hexadecimal.*
2. *See Table 1 for description of bus operations.*
3. *The data is 00h for an unprotected sector and 01h for a protected sector. The complete bus address is composed of the sector address on A18–A13 and 02h on A7–A0.*
4. *Read and program functions in non-erasing sectors are allowed in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
5. *The Erase Resume command is valid only during the Erase Suspend mode.*
6. *Unless otherwise noted, address bits A18–A11 = X = don't care.*

WRITE OPERATION STATUS (PAGE 16)

$\overline{\text{RESET}}$: Hardware Reset Pin

The $\overline{\text{RESET}}$ pin is an active low signal. A logic '0' on this pin will force the device out of any mode that is currently executing back to the reset state. This allows a system reset to take effect immediately without having to wait for the device to finish a long execution cycle. To avoid a potential bus contention during a system reset, the device is isolated from the data I/O bus by tri-stating the data output pins for the duration of the $\overline{\text{RESET}}$ pulse.

If $\overline{\text{RESET}}$ is asserted during a program or erase operation, the RY/$\overline{\text{BY}}$ pin will remain low until the reset operation is internally complete. This will require between 1 µs and 20 µs. Hence the RY/$\overline{\text{BY}}$ pin can be used to signal that the reset operation is complete. Otherwise, allow for the maximum reset time of 20 µs. If $\overline{\text{RESET}}$ is asserted when a program or erase operation is not executing (RY/$\overline{\text{BY}}$ pin is high), the reset operation will be complete within 500 ns.

Asserting $\overline{\text{RESET}}$ during a program or erase operation leaves erroneous data stored in the address locations being operated on at the time of device reset. These locations need updating after the reset operation is complete. See Figure 2 for timing specifications.

The device enters I_{CC4} standby mode (200 nA) when $V_{SS} \pm 0.3$ V is applied to the $\overline{\text{RESET}}$ pin. The device can enter this mode at any time, regardless of the logical condition of the $\overline{\text{CE}}$ pin. Furthermore, entering I_{CC4} during a program or erase operation leaves erroneous data in the address locations being operated on at the time of the $\overline{\text{RESET}}$ pulse. These locations need updating after the device resumes standard operations. After the $\overline{\text{RESET}}$ pin goes high, a minimum latency period of 50 ns must occur before a valid read can take place.

OPERATING RANGES (PAGE 23)

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for Am29LV004T/B-90R . . . . . +3.0 V to 3.6 V

V_{CC} for Am29LV004T/B-100, -120, -150. . . . . +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

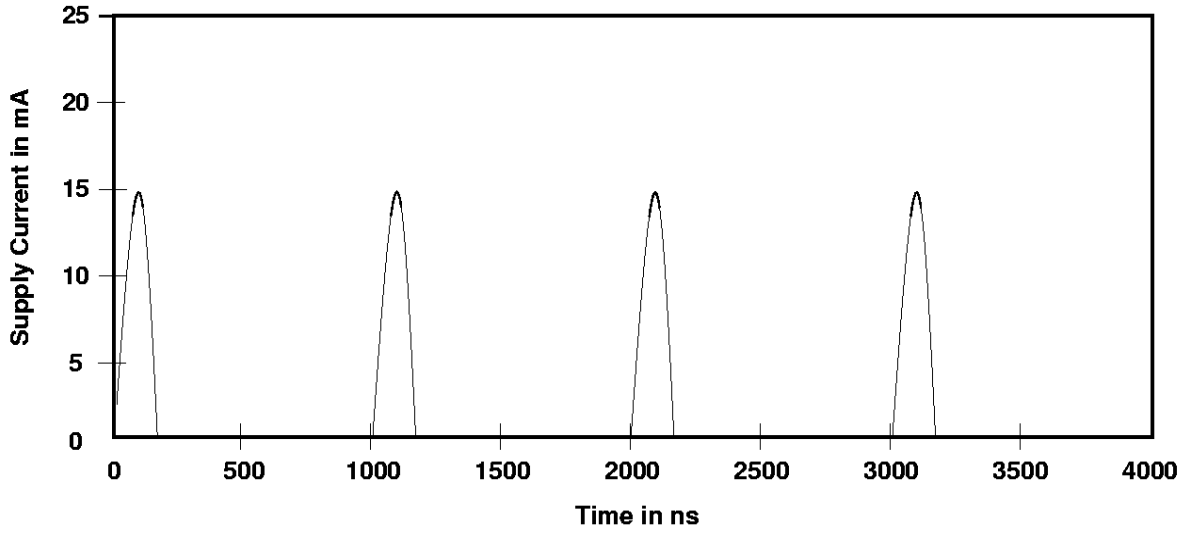
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 13.0 V		35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ at 5 MHz		16	mA
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ at 1 MHz		4	mA
I_{CC2}	V_{CC} Active Current (Notes 1, 2, and 4)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC\ max}$; $\overline{CE}$, $\overline{RESET} = V_{CC} \pm 0.3$ V		5	µA
I_{CC4}	V_{CC} Standby Current During Reset	$V_{CC} = V_{CC\ max}$; $\overline{CE} = V_{CC} \pm 0.3$ V; $\overline{RESET} = V_{SS} \pm 0.3$ V		5	µA
I_{CC5}	Automatic Sleep Mode (Note 3)	$V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V		5	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, $V_{CC} = V_{CC\ min}$	0.85 V_{CC}		V
V_{OH2}		I_{OH} = -100 µA, $V_{CC} = V_{CC\ min}$	V_{CC}-0.4		
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)		2.3	2.5	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
3. *Automatic sleep mode enables the low power mode when addresses remain stable for 200 ns. Typical sleep mode current is 200 nA.*
4. *Not 100% tested.*

DC CHARACTERISTICS (CONTINUED)



Note: *Addresses are switching at 1 MHz*

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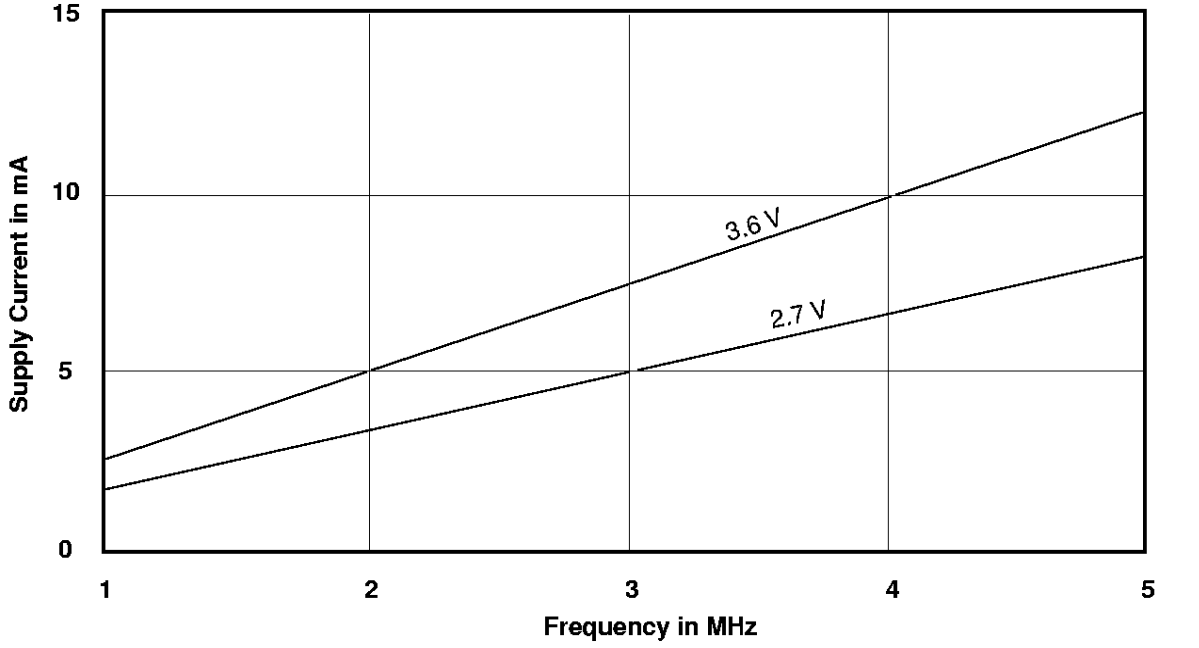
Figure 8A. I_{CC} Current vs. Time



Note: *T = 25 °C*

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Figure 8B. I_{CC} vs. Frequency

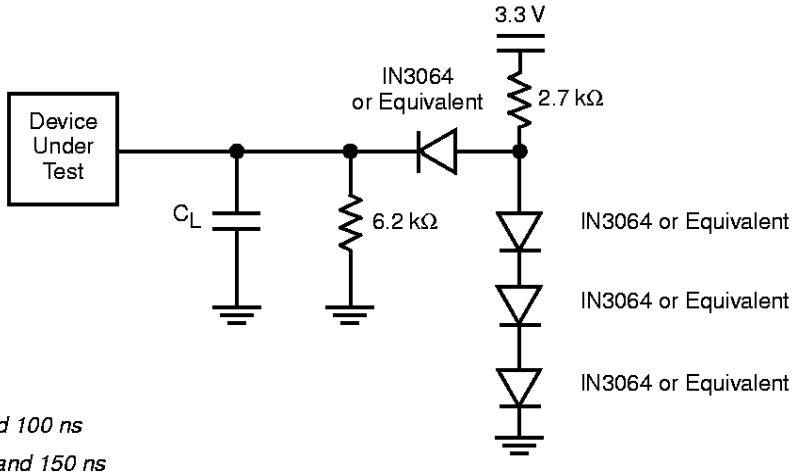
AC CHARACTERISTICS

Read-Only Operations Characteristics

Parameter Symbols		Description	Test Setup		Speed Option (Note 1)				Unit
JEDEC	Standard				-90R	-100	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)		Min	90	100	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	90	100	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	90	100	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	40	40	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 2, 3)		Max	30	30	30	40	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 2, 3)		Max	30	30	30	40	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First (Note 3)		Min	0	0	0	0	ns
	t_{Ready}	$\overline{RESET}$ Pin Low to Read Mode (Note 3)		Max	20	20	20	20	µs

Notes:

1. *Test Conditions*
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level:
   Input: 1.5 V
   Output: 1.5 V
2. *Output Driver Disable Time*
3. *Not 100% tested.*



Notes:

C_L = 30 pF for 90 and 100 ns

C_L = 100 pF for 120 and 150 ns

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Figure 9. Test Conditions

AC CHARACTERISTICS

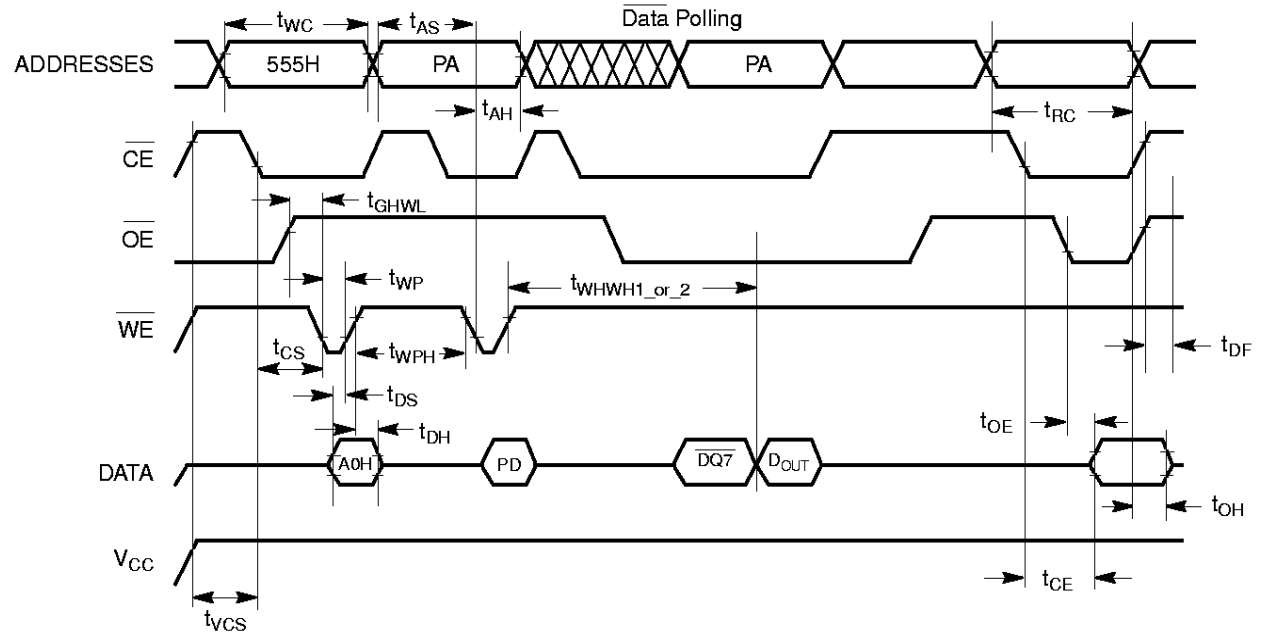
Write (Erase/Program) Operations

Parameter Symbols		Description			-90R	-100	-120	-150	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	90	100	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	50	50	50	65	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	50	50	50	65	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note 2)		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling (Note 2)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	50	50	50	65	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	9	9	9	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1	1	1	1	sec
	t_{VCS}	V_{CC} Setup Time		Min	50	50	50	50	µs
	t_{RB}	Write Recovery Time from RY/$\overline{BY}$		Min	0	0	0	0	ns
	t_{RH}	$\overline{RESET}$ High Time Before Read		Min	50	50	50	50	ns
	t_{RPD}	$\overline{RESET}$ To Power Down Time		Min	20	20	20	20	µs
	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min	90	90	90	90	ns
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	500	500	500	ns
	t_{RRB}	$\overline{RESET}$ Low to RY/$\overline{BY}$ High		Max	20	20	20	20	µs
	t_{RSP}	$\overline{RESET}$ Setup Time for Temporary Sector Unprotect		Min	4	4	4	4	µs

Notes:

1. *The duration of the program or erase operation is variable and is calculated in the internal algorithms.*
2. *Note 100% tested.*

SWITCHING WAVEFORMS (PAGE 28)



Notes:

1. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
2. *D_{OUT} is the output of the data written to the device.*
3. *PA is the address of the memory location to be programmed.*
4. *PD is the data to be programmed at the byte address.*
5. *Illustration shows the last two cycles of a four-bus-cycle sequence*

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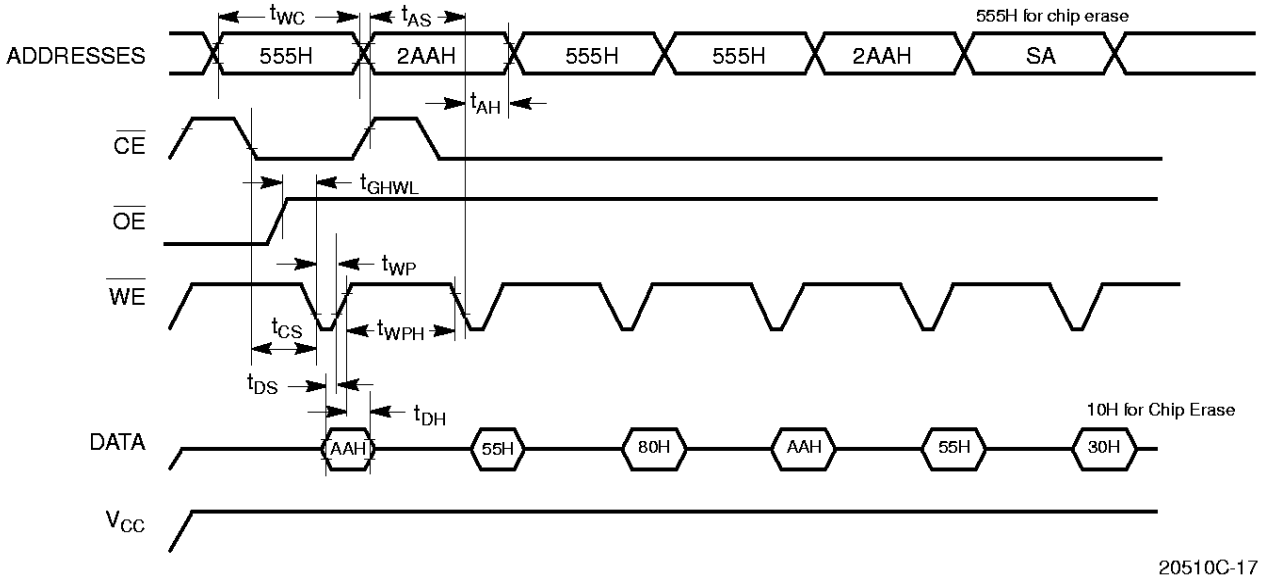
Figure 13. AC Waveforms for Program Operations

SWITCHING WAVEFORMS (PAGE 29)



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Note: *SA is the sector address for Sector Erase*

Figure 14. AC Waveforms for Chip/Sector Erase Operations

SWITCHING WAVEFORMS (PAGE 31)

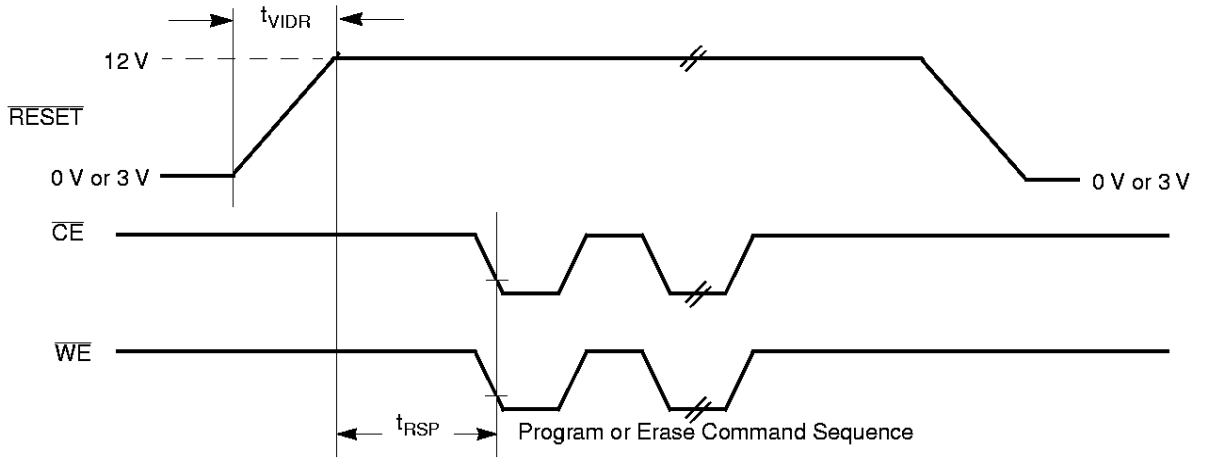


Figure 19. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS (PAGE 32)

Write (Erase/Program) Operations

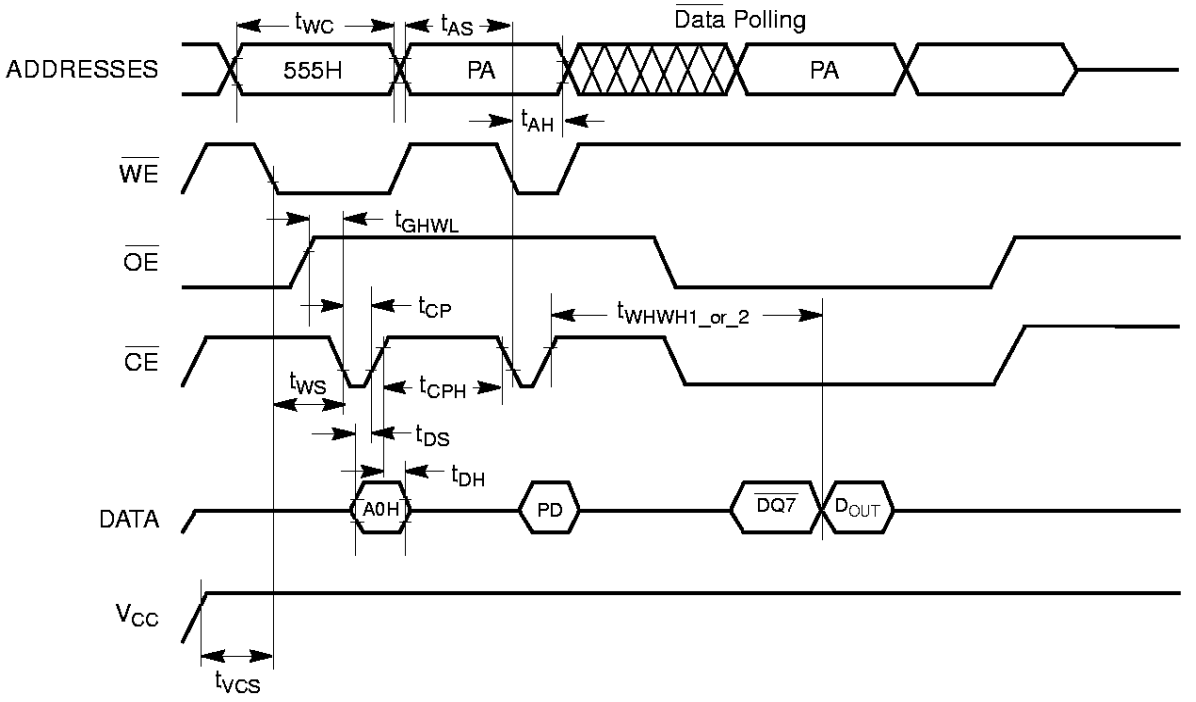
Alternate CE Controlled Writes

Parameter Symbols		Description			-90R	-100	-120	-150	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	50	50	50	65	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	50	50	50	65	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 1)	Min	0	0	0	0	ns
			Toggle and Data Polling (Note 1)	Min	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	50	50	50	65	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	9	9	9	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1	1	1	1	sec

Notes:

1. *Not 100% tested.*
2. *Does not include the preprogramming time.*
3. *The duration of the program or erase operation is variable and is calculated in the internal algorithms.*

SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the complement of the data written to the device.*
4. *D_{OUT} is the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

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Figure 20. Alternate $\overline{CE}$ Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE (PAGE 34)

Parameter	Typ (Note 2)	Max (Note 3)	Unit	Comments
Sector Erase Time	1	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	11		s	
Byte Programming Time	9	300	µs	Excludes system level overhead (Note 5)
Chip Programming Time	4.5	13.5	s	
Erase/Program Endurance	1,000,000		cycles	Minimum 100,000 cycles guaranteed

Notes:

1. *The typical program and erase times are considerably less than the maximum times since most bytes program or erase significantly faster than the worst case byte. The device enters the failure mode (DQ5="1") only after the maximum times given are exceeded. See the section on DQ5 for further information.*
2. *Except for erase and program endurance, the typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
3. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 100,000 cycles.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.*

Trademarks