FAIRCHILD SEMICONDUCTOR®

January 2012

FPF1320 / FPF1321
IntelliMAX™ Dual-Input Single-Output Advanced Power Switch with True Reverse-Current Blocking

Features

- DISO Load Switches
- Input Supply Operating Range: 1.5V ~ 5.5V
- R_{ON} 50mΩ at V_{IN}=3.3V Per Channel (Typical)
- True Reverse-Current Blocking (TRCB)
- Fixed Slew Rate Controlled 130µs for < 1µF C_{OUT}
- I_{SW}: 1.5A Per Channel (Maximum)
- Quick Discharge Feature on FPF1321
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: >6kV
  - Charged Device Model: >1.5kV
  - IEC 61000-4-2 Air Discharge: >15kV
  - IEC 61000-4-2 Contact Discharge: >8kV

Applications

- Smart phones / Tablet PCs
- Portable Devices
- Near Field Communication (NFC) Capable SIM Card Power Supply

Description

The FPF1320/21 is a Dual-Input Single-Output (DISO) load switch consisting of two sets of slew-rate controlled, low on-resistance, P-channel MOSFET switches and integrated analog features. The slew-rate-controlled turn-on characteristic prevents inrush current and the resulting excessive voltage droop on the power rails. The input voltage range operates from 1.5V to 5.5V to align with the requirements of low-voltage portable device power rails. FPF1320/21 performs seamless power-source transitions between two input power rails using the SEL pin with advanced break-before-make operation.

FPF1320/21 has a TRCB function to block unwanted reverse current from output to input during ON/OFF states. The switch is controlled by logic inputs of the SEL and EN pins, which are capable of interfacing directly with low-voltage control signals (GPIO).

FPF1321 has 65Ω on-chip load resistor for output quick discharge when EN is LOW.

FPF1320/21 is available in 1.0mm x 1.5mm WLCSP, 6-bump, with 0.5mm pitch.

Ordering Information

Part Number	Top Mark	Channel	Switch Per Channel (Typ.) at $3.3V_{IN}$	Reverse Current Blocking	Output Discharge	Rise Time (t_R)	Package
FPF1320UCX	QS	DISO	50mΩ	Yes	NA	130µs	1.0mmX1.5mm Wafer-Level Chip-Scale Package (WLCSP) 6-Bumps, 0.5mm Pitch
FPF1321UCX	QT	DISO	50mΩ	Yes	65Ω	130µs	

Application Diagram

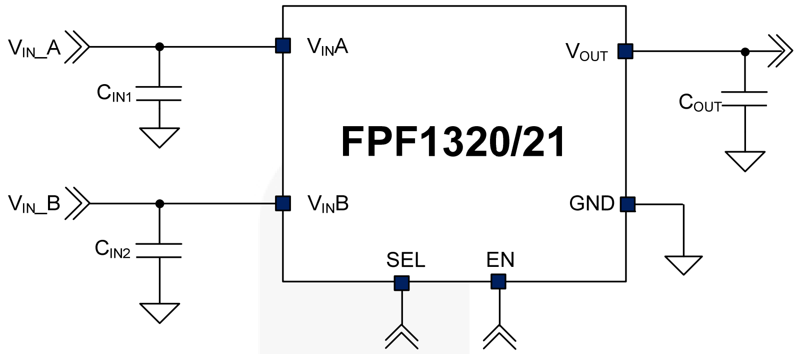


Figure 1. Typical Application

Block Diagram

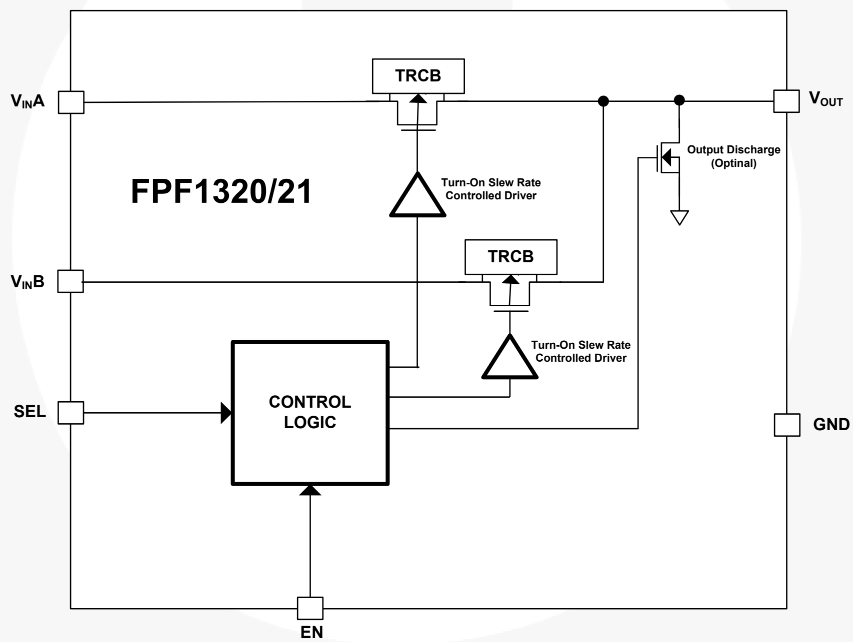
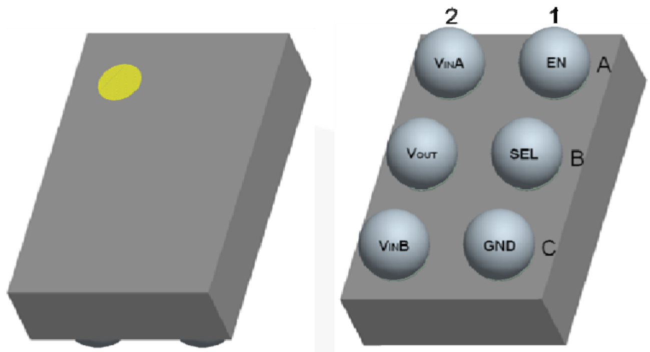


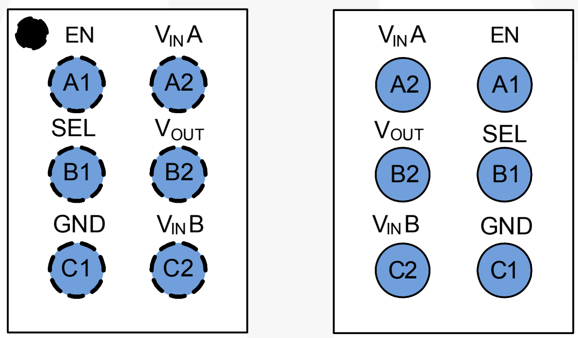
Figure 2. Functional Block Diagram (Output Discharge Path for FPF1321 Only)

Pin Configuration



Top View Bottom View

Figure 3. Pin Configuration in Package View with Pin 1 Indicator



Top View Bottom View

Figure 4. Pin Assignments

Pin Description

Pin #	Name	Description
A1	EN	Enable input. Active HIGH. There is an internal pull-down resistor at the EN pin.
B1	SEL	Input power selection inputs. *See Table 1*. There are internal pull-down resistors at the SEL pins.
A2	$V_{IN}A$	Supply Input. Input to the power switch A.
B2	V_{OUT}	Switch output
C1	GND	Ground
C2	$V_{IN}B$	Supply Input. Input to power switch B.

Table 1. Truth Table

SEL	EN	Switch A	Switch B	V_{OUT}	Status
LOW	HIGH	ON	OFF	$V_{IN}A$	$V_{IN}A$ Selected
HIGH	HIGH	OFF	ON	$V_{IN}B$	$V_{IN}B$ Selected
X	LOW	OFF	OFF	Floating for FPF1320 GND for FPF1321	Both Switches are OFF

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<tr><th>Symbol</th><th colspan="2">Parameters</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>V_{IN}</td><td colspan="2">$V_{IN}A$, $V_{IN}B$, V_{SEL}, V_{EN}, V_{OUT} to GND</td><td>-0.3</td><td>6</td><td>V</td></tr>
<tr><td>I_{SW}</td><td colspan="2">Maximum Continuous Switch Current per Channel</td><td></td><td>1.5</td><td>A</td></tr>
<tr><td>P_D</td><td colspan="2">Total Power Dissipation at T_A=25°C</td><td></td><td>1.2</td><td>W</td></tr>
<tr><td>T_{STG}</td><td colspan="2">Operating and Storage Junction Temperature</td><td>-65</td><td>150</td><td>°C</td></tr>
<tr><td rowspan="2">Θ_{JA}</td><td colspan="2" rowspan="2">Thermal Resistance, Junction-to-Ambient
(1in.^{2} Pad of 2-oz. Copper)</td><td></td><td>85[1]</td><td rowspan="2">°C/W</td></tr>
<tr><td></td><td>110[2]</td></tr>
<tr><td rowspan="4">ESD</td><td rowspan="4">Electrostatic Discharge Capability</td><td>Human Body Model, JESD22-A114</td><td>6.0</td><td></td><td rowspan="4">kV</td></tr>
<tr><td>Charged Device Model, JESD22-C101</td><td>1.5</td><td></td></tr>
<tr><td>Air Discharge ($V_{IN}A$, $V_{IN}B$ to GND), IEC61000-4-2 System Level</td><td>15.0</td><td></td></tr>
<tr><td>Contact Discharge ($V_{IN}A$, $V_{IN}B$ to GND), IEC61000-4-2 System Level</td><td>8.0</td><td></td></tr>
</table>

Notes:
1. Measured using 2S2P JEDEC std. PCB.
2. Measured using 2S2P JEDEC PCB cold-plate method.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Min.	Max.	Unit
V_{IN}	Input Voltage on $V_{IN}A$, $V_{IN}B$	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	85	°C

Electrical Characteristics

$V_{IN}A$=$V_{IN}B$=1.5 to 5.5V, T_A=-40 to 85°C unless otherwise noted. Typical values are at $V_{IN}A$=$V_{IN}B$=3.3V and T_A=25°C.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
$V_{IN}A$, $V_{IN}B$	Input Voltage		1.5		5.5	V
I_{SD}	Shutdown Current	SEL=HIGH or LOW, EN=GND, V_{OUT}=GND, $V_{IN}A$=$V_{IN}B$=5.5V			5	µA
I_Q	Quiescent Current	I_{OUT}=0mA, SEL=HIGH or LOW, EN=HIGH, $V_{IN}A$=$V_{IN}B$=5.5V		12	22	µA
R_{ON}	On-Resistance	$V_{IN}A$=$V_{IN}B$=5.5V, I_{OUT}=200mA, T_A=25°C		42	60	mΩ
		$V_{IN}A$=$V_{IN}B$=3.3V, I_{OUT}=200mA, T_A=25°C		50		
		$V_{IN}A$=$V_{IN}B$=1.8V, I_{OUT}=200mA, T_A=25°C to 85°C		80		
		$V_{IN}A$=$V_{IN}B$=1.5V, I_{OUT}=200mA, T_A=25°C			170	
V_{IH}	SEL, EN Input Logic High Voltage	$V_{IN}A$, $V_{IN}B$=1.5V – 5.5V	1.15			V
V_{IL}	SEL, EN Input Logic Low Voltage	$V_{IN}A$, $V_{IN}B$=1.8V – 5.5V			0.65	V
	SEL, EN Input Logic Low Voltage	$V_{IN}A$, $V_{IN}B$=1.5V – 1.8V			0.60	
V_{DROOP_OUT}	Output Voltage Droop while Channel Switching from Higher Input Voltage Lower Input Voltage[3]	$V_{IN}A$=3.3V, $V_{IN}B$=5V, Switching from $V_{IN}A$ → $V_{IN}B$, R_L=150Ω, C_{OUT}=1µF			100	mV
I_{SEL}/I_{EN}	Input Leakage at SEL and EN Pin				1.2	µA
R_{SEL_PD}/R_{EN_PD}	Pull-Down Resistance at SEL or EN Pin			7		MΩ
R_{PD}	Output Pull-Down Resistance	SEL=HIGH or LOW, EN=GND, I_{FORCE}=20mA, T_A=25°C, FPF1321		65		Ω
True Reverse Current Blocking						
V_{T_RCB}	RCB Protection Trip Point	V_{OUT} - $V_{IN}A$ or $V_{IN}B$		45		mV
V_{R_RCB}	RCB Protection Release Trip Point	$V_{IN}A$ or $V_{IN}B$ -V_{OUT}		25		mV
I_{RCB}	$V_{IN}A$ or $V_{IN}B$ Current During RCB	V_{OUT}=5.5V, $V_{IN}A$ or $V_{IN}B$=Short to GND		9	15	µA
t_{RCB_ON}	RCB Response Time when Device is ON[3]	$V_{IN}A$ or $V_{IN}B$=5V, $V_{OUT}V_{INA,B}$=100mV		5		µs

Continued on the following page…

Electrical Characteristics (Continued)

$V_{IN}A$=$V_{IN}B$=1.5 to 5.5V, T_A=-40 to 85°C unless otherwise noted. Typical values are at $V_{IN}A$=$V_{IN}B$=3.3V and T_A=25°C.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Unit
Dynamic Characteristics						
t_{DON}	Turn-On Delay(4)	$V_{IN}A$ or $V_{IN}B$=3.3V, R_L=150Ω, C_L=1μF, T_A=25°C, SEL: HIGH, EN: LOW → HIGH		120		μs
t_R	V_{OUT} Rise Time(4)			130		μs
t_{ON}	Turn-On Time(6)			250		μs
t_{DOFF}	Turn-Off Delay(4)	$V_{IN}A$ or $V_{IN}B$=3.3V, R_L=150Ω, C_L=1μF, T_A=25°C, SEL: HIGH, EN: HIGH → LOW		15		μs
t_F	V_{OUT} Fall Time(4)			320		μs
t_{OFF}	Turn-Off Time(7)			335		μs
t_{DOFF}	Turn-Off Delay(4,5)	$V_{IN}A$ or $V_{IN}B$ =3.3V, R_L=150Ω, C_L=1μF, T_A=25°C, SEL: HIGH, EN: HIGH → LOW, Output Discharge Mode, FPF1321		6		μs
t_F	V_{OUT} Fall Time(4,5)			110		μs
t_{OFF}	Turn-Off Time(5,7)			116		μs
t_{TRANR}	Transition Time LOW → HIGH(4)	$V_{IN}A$=3.3V, $V_{IN}B$=5V, Switching from $V_{IN}A$ → $V_{IN}B$, SEL: LOW → HIGH, EN: HIGH, R_L=150Ω, C_L=1μF, T_A=25°C		3		μs
t_{SLH}	Switch-Over Rising Delay(4)			1		μs
t_{TRANF}	Transition Time HIGH → LOW(4)	$V_{IN}A$=3.3V, $V_{IN}B$=5V, Switching from VINB → $V_{IN}A$, SEL: HIGH → LOW, EN: HIGH, R_L=150Ω, C=1μF, T_A=25°C		45		μs
t_{SHL}	Switch-Over Falling Delay(4)			5		μs

Notes:

3. This parameter is guaranteed by design and characterization; not production tested.
4. t_{DON}/t_{DOFF}/t_R/t_F/t_{TRANR}/t_{TRANF}/t_{SLH}/t_{SHL} are defined in Figure 5.
5. FPF1321 output discharge is enabled during off.
6. t_{ON}=t_R + t_{DON}.
7. t_{OFF}=t_F + t_{DOFF}.

Timing Diagram

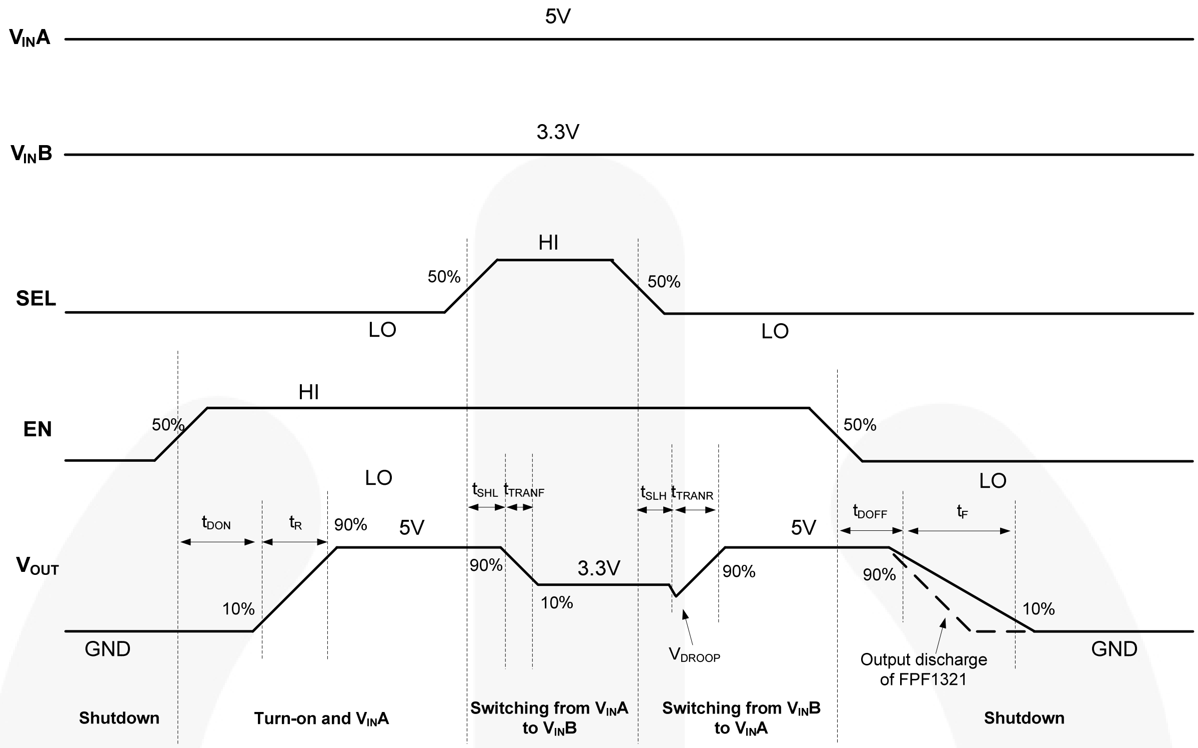


Figure 5. Dynamic Behavior Timing Diagram

Typical Characteristics

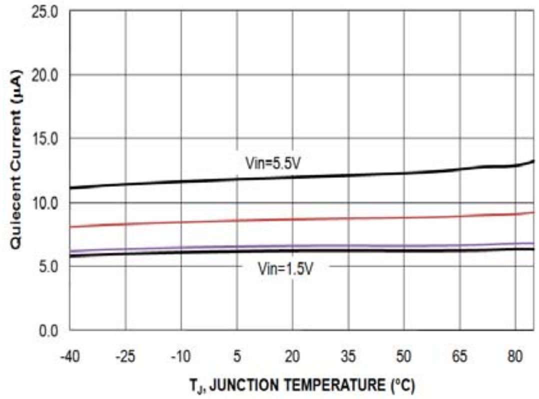


Figure 6. Supply Current vs. Temperature

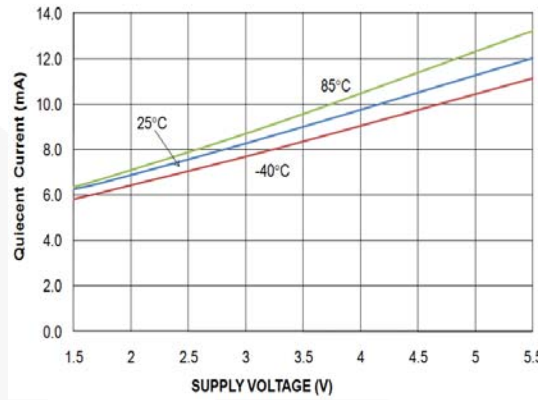


Figure 7. Supply Current vs. Supply Voltage

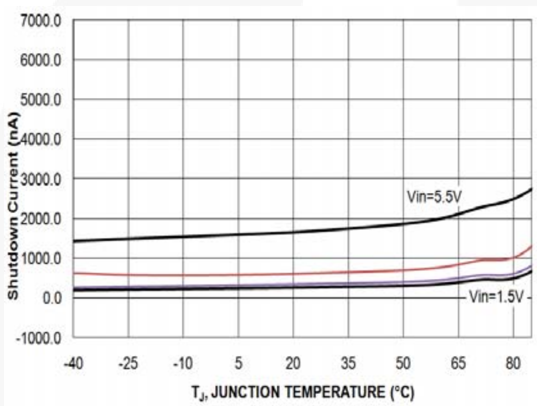


Figure 8. Shutdown Current vs. Temperature

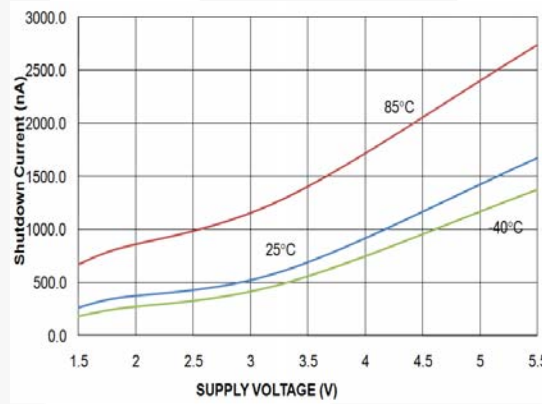


Figure 9. Shutdown Current vs. Supply Voltage

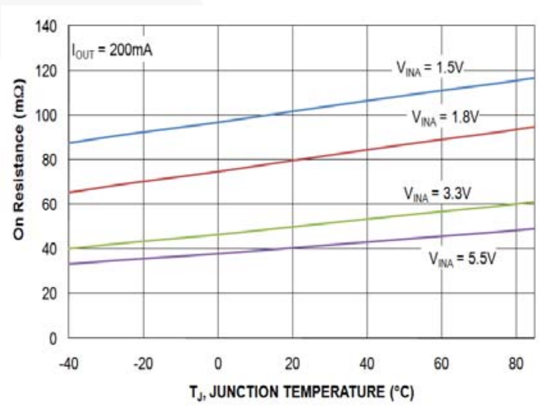


Figure 10. R_{ON} vs. Temperature

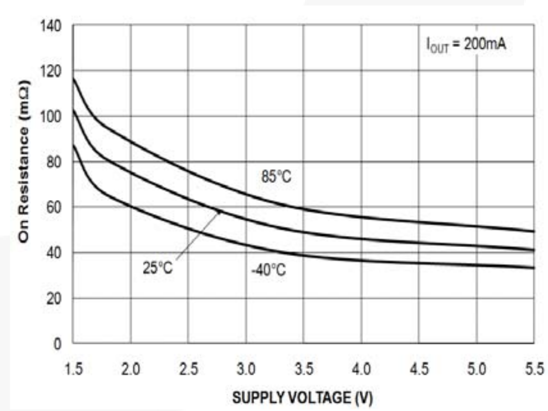


Figure 11. R_{ON} vs. Supply Voltage

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Typical Characteristics

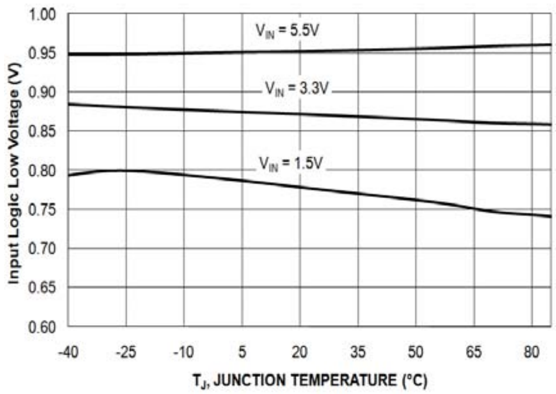

Figure 12. V_{IL} vs. Temperature

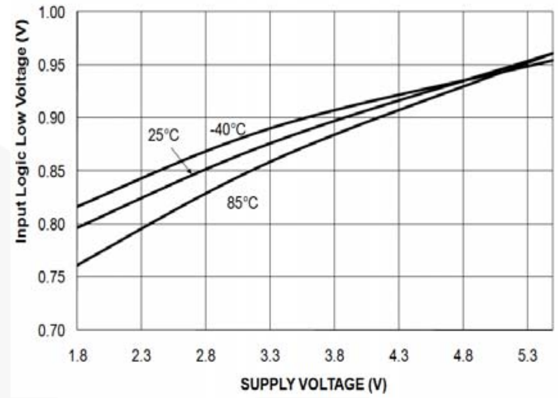

Figure 13. V_{IL} vs. Supply Voltage

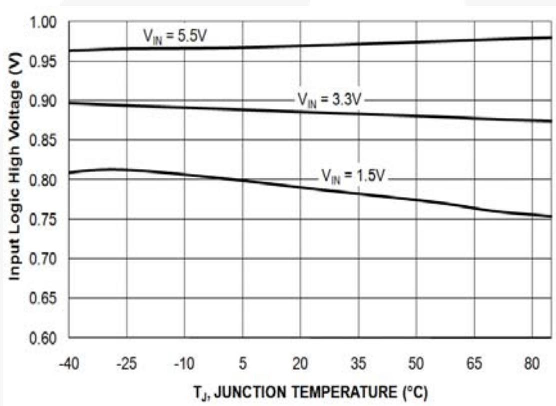

Figure 14. V_{IH} vs. Temperature

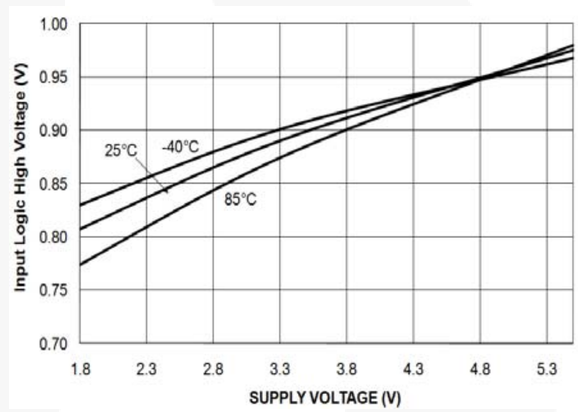

Figure 15. V_{IH} vs. Supply Voltage

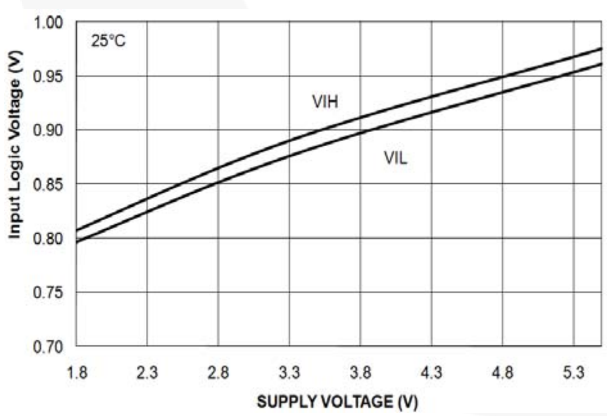

Figure 16. V_{IH} / V_{IL} vs. Supply Voltage

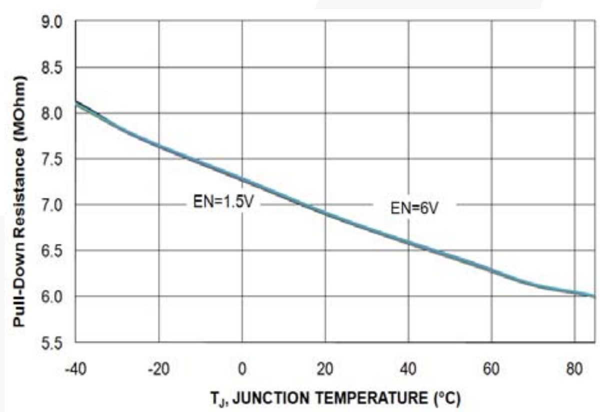

Figure 17. R_{SEL_PD} and R_{EN_PD} vs. Temperature

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Typical Characteristics

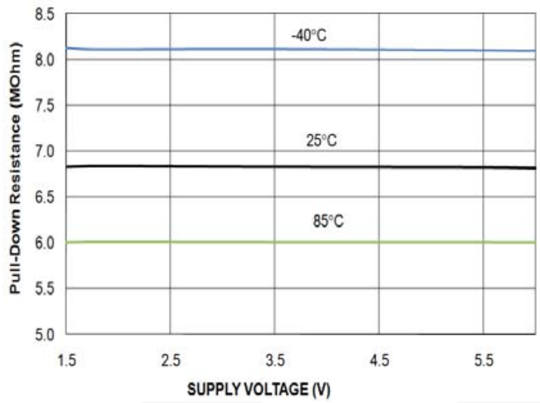

Figure 18. R_{SEL_PD} and R_{EN_PD} vs. Supply Voltage

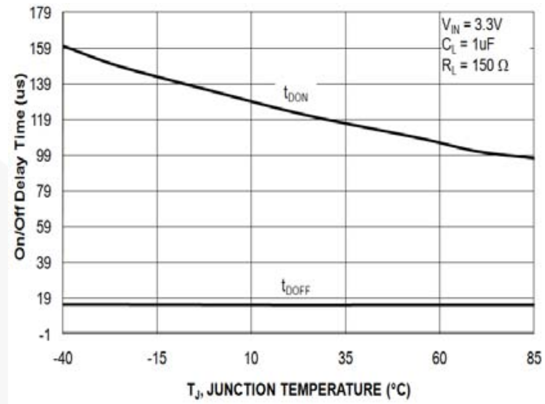

Figure 19. t_{DON} and t_{DOFF} vs. Temperature

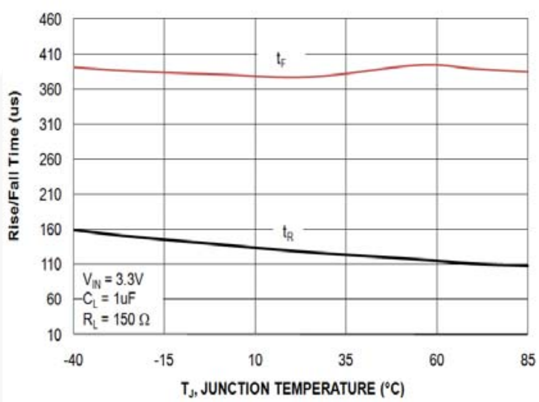

Figure 20. t_R and t_F with FPF1320 vs. Temperature

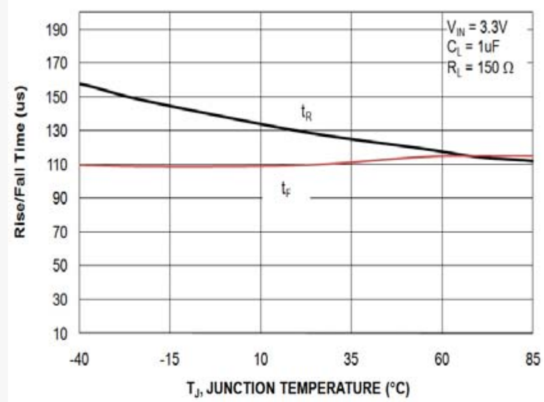

Figure 21. t_R and t_F with FPF1321 vs. Temperature

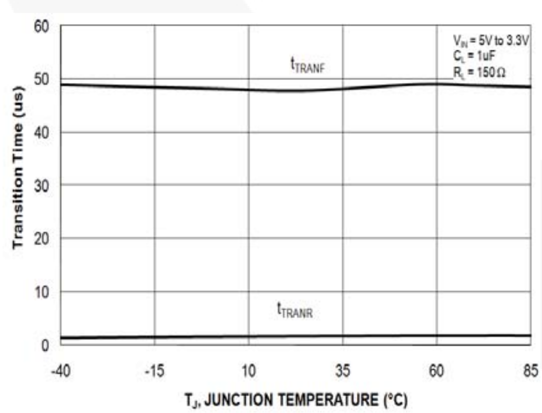

Figure 22. Transition Time vs. Temperature

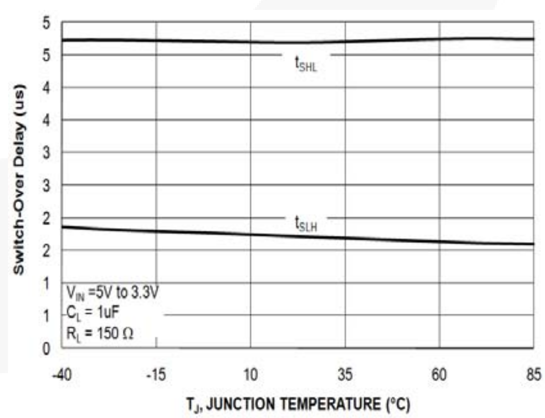

Figure 23. Switch Over Time vs. Temperature

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Typical Characteristics

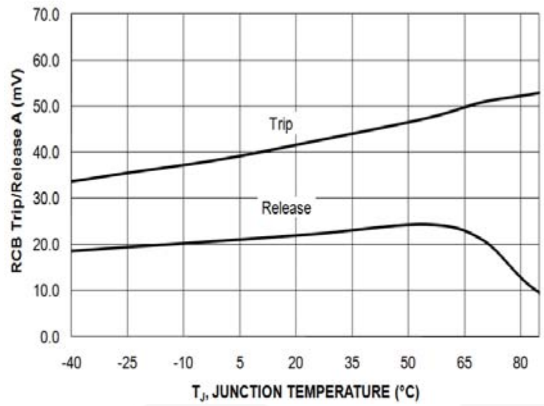

Figure 24. TRCB Trip and Release vs. Temperature

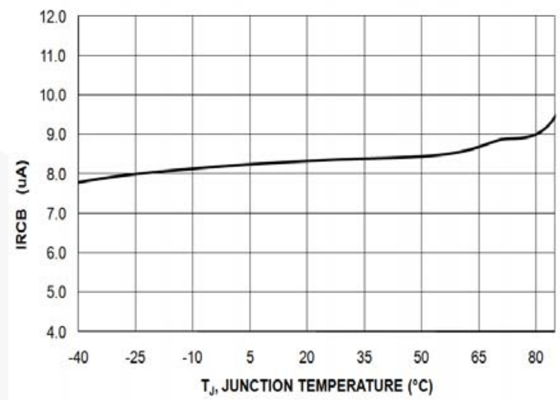

Figure 25. I_{RCB} vs. Temperature

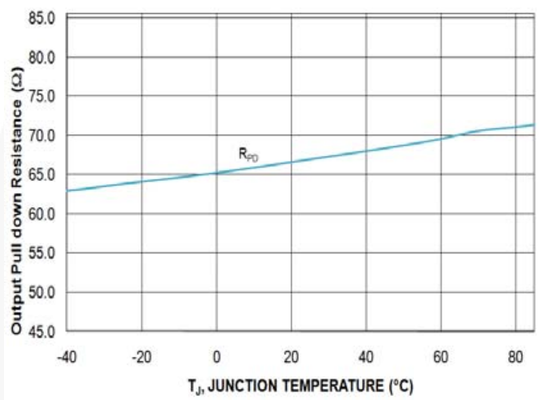

Figure 26. R_{PD} with FPF1321 vs. Temperature

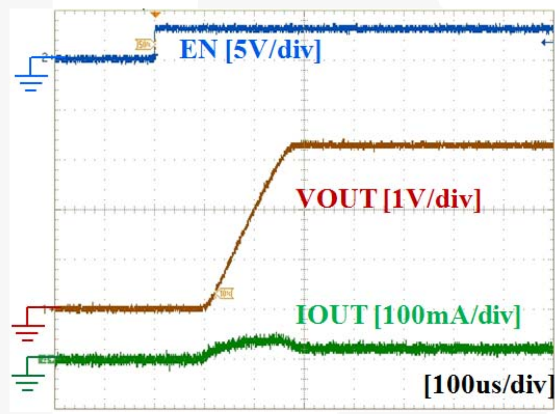

Figure 27. Turn-On Response
(V_{IN}A=3.3V, C_{IN}=1μF, C_{OUT}=1μF, R_L=150Ω, SEL=LO)

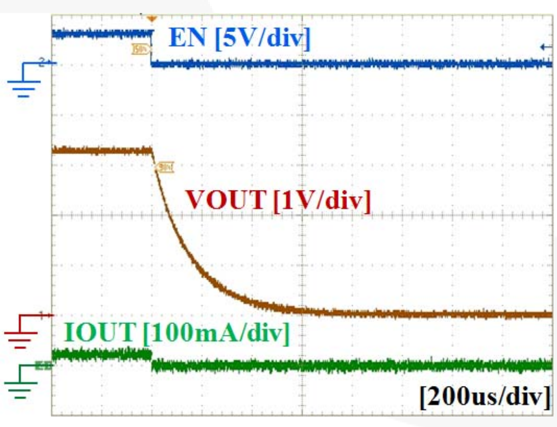

Figure 28. Turn-Off Response with FPF1320
(V_{IN}A=3.3V, C_{IN}=1μF, C_{OUT}=1μF, R_L=150Ω,
SEL=LOW)

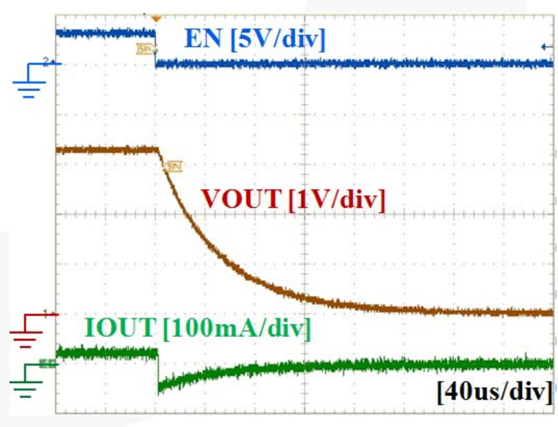

Figure 29. Turn-Off Response with FPF1321
(V_{IN}A=3.3V, C_{IN}=1μF, C_{OUT}=1μF, R_L=150Ω
SEL=LOW)

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Typical Characteristics

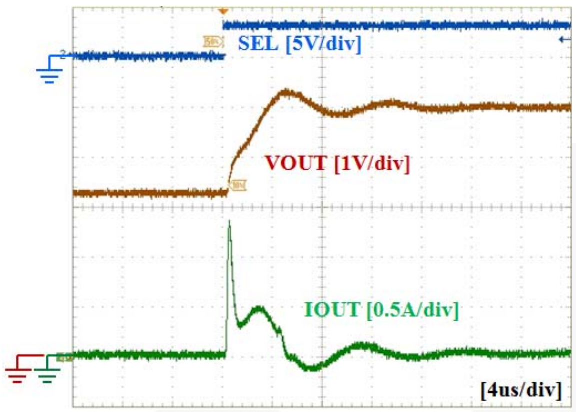

Figure 30. Power Source Transition from 3.3V to 5V ($V_{IN}A$=3.3V, $V_{IN}B$=5V, C_{IN}=1μF, C_{OUT}=1μF, R_L=150Ω)

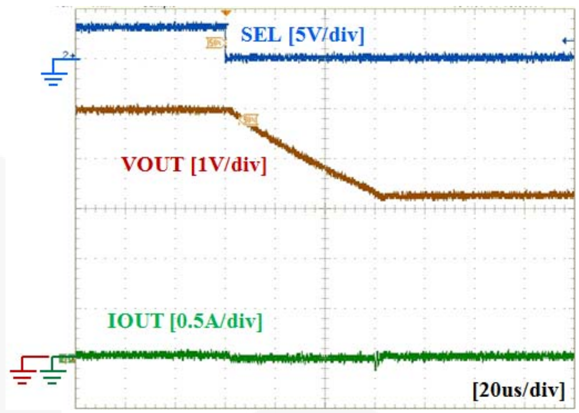

Figure 31. Power Source Transition from 5V to 3.3V ($V_{IN}A$=3.3V, $V_{IN}B$=5V, C_{IN}=1μF, C_{OUT}=1μF, R_L=150Ω)

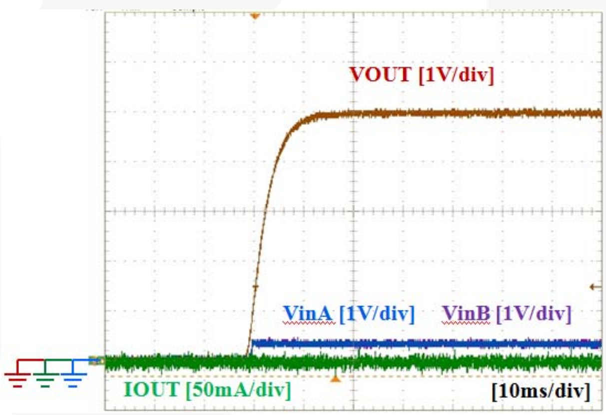

Figure 32. TRCB During Off ($V_{IN}A$=$V_{IN}B$=Floating, V_{OUT}=5V, C_{IN}=1μF, C_{OUT}=1μF, EN=LOW, No R_L)

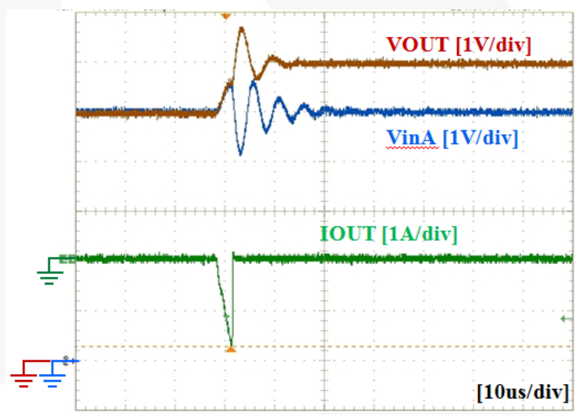

Figure 33. TRCB During On ($V_{IN}A$=5V, V_{OUT}=6V, C_{IN}=1μF, C_{OUT}=1μF, EN=HIGH, No R_L)

Operation and Application Description

The FPF1320 and FPF1321 are dual-input single-output power multiplexer switches with controlled turn-on and seamless power source transition. The core is a 50mΩ P-channel MOSFET and controller capable of functioning over a wide input operating range of 1.5V to 5.5V per channel. The EN and SEL pins are active-HIGH, GPIO/CMOS-compatible input. They control the state of the switch and input power source selection, respectively. TRCB functionality blocks unwanted reverse current during both ON and OFF states when higher V_{OUT} than $V_{IN}A$ or $V_{IN}B$ is applied. FPF1321 has a 65Ω output discharge path during off.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor; a capacitor must be placed between the $V_{IN}A$ or $V_{IN}B$ pins to the GND pin. At least 1µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher-value C_{IN} can be used to reduce more the voltage drop.

Inrush Current

Inrush current occurs when the device is turned on. Inrush current is dependent on output capacitance and slew rate control capability, as expressed by:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN} - V_{INITIAL}}{t_R} + I_{LOAD} \qquad (1)$$

where:

C_{OUT}: Output capacitance;

t_R: Slew rate or rise time at V_{OUT};

V_{IN}: Input voltage, $V_{IN}A$ or $V_{IN}B$;

$V_{INITIAL}$: Initial voltage at C_{OUT}, usually GND; and

I_{LOAD}: Load current.

Higher inrush current causes higher input voltage drop, depending on the distributed input resistance and input capacitance. High inrush current can cause problems.

FPF1320/1 has a 130µs of slew rate capability under $3.3V_{IN}$ at 1µF of C_{OUT} and 150Ω of R_L so inrush current and input voltage drop can be minimized.

Power Source Selection

Input power source selection can be controlled by the SEL pin. When SEL is LOW, output is powered from $V_{IN}A$ while SEL is HIGH, $V_{IN}B$ is powering output. The SEL signal is ignored during device OFF.

Output Voltage Drop during Transition

Output voltage drop usually occurs during input power source transition period from low voltage to high voltage. The drop is highly dependent on output capacitance and load current.

FPF1320/1 adopts an advanced break-before-make control, which can result in minimized output voltage drop during the transition time.

Output Capacitor

Capacitor C_{OUT} of at least 1µF is highly recommended between the V_{OUT} and GND pins to achieve minimized output voltage drop during input power source transition. This capacitor also prevents parasitic board inductance.

True Reverse-Current Blocking

The true reverse-current blocking feature protects the input source against current flow from output to input regardless of whether the load switch is on or off.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance on normal and short-circuit operation. Wide traces or large copper planes for power pins ($V_{IN}A$, $V_{IN}B$, V_{OUT} and GND) minimize the parasitic electrical effects and the thermal impedance.

Physical Dimensions

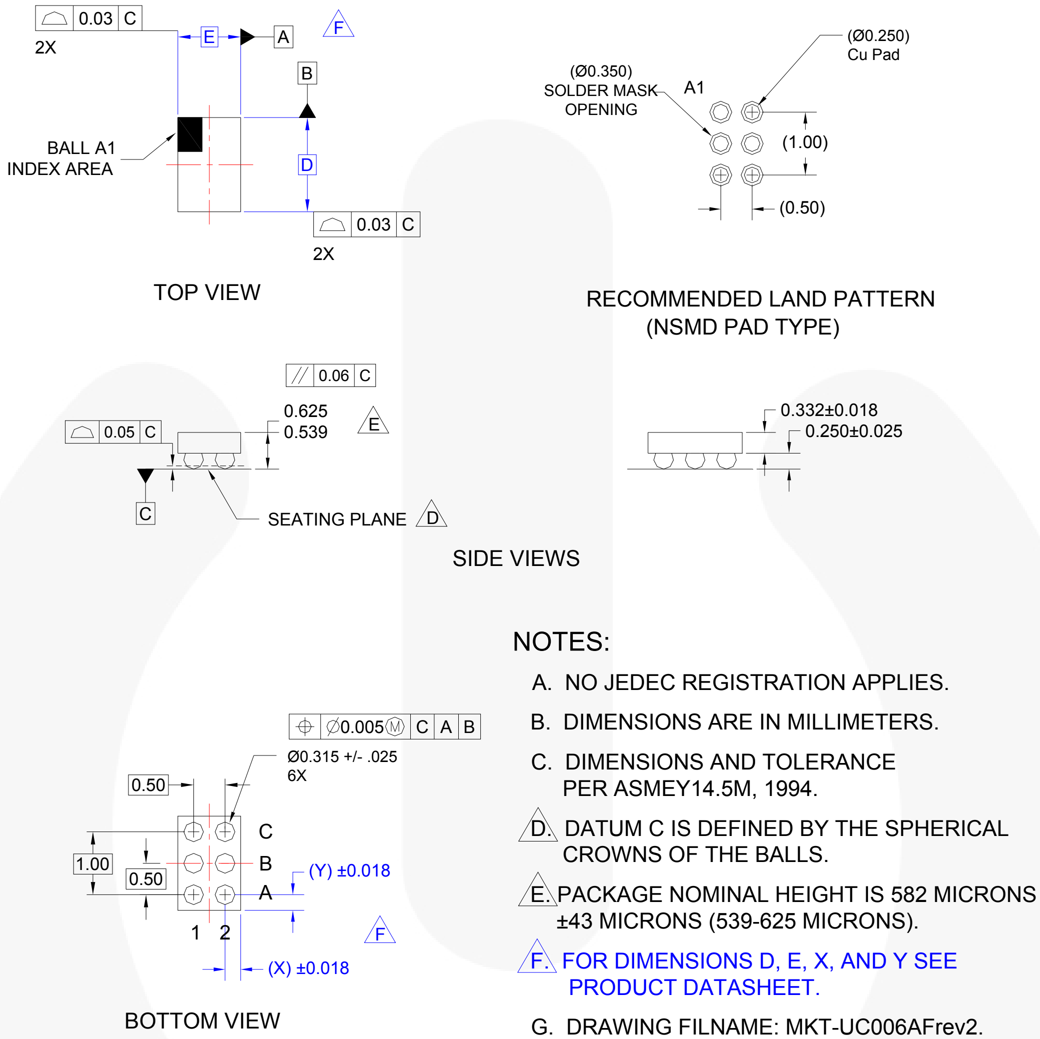

Figure 34. 6 Ball, 1.0 x 1.5mm, Wafer-Level Chip-Scale Package (WLCSP)

Product-Specific Dimensions

Product	D	E	X	Y
FPF1320UCX	1460μm+/-30μm	960μm+/-30μm	230μm	230μm
FPF1321UCX	1460μm+/-30μm	960μm+/-30μm	230μm	230μm

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