HD151TS302BST

Spread Spectrum Clock for EMI Solution

REJ03D0215–0101Z
Preliminary
Rev.1.01
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Description

The HD151TS302BST is a high-performance Spread Spectrum Clock modulator. It is suitable for low EMI solution.

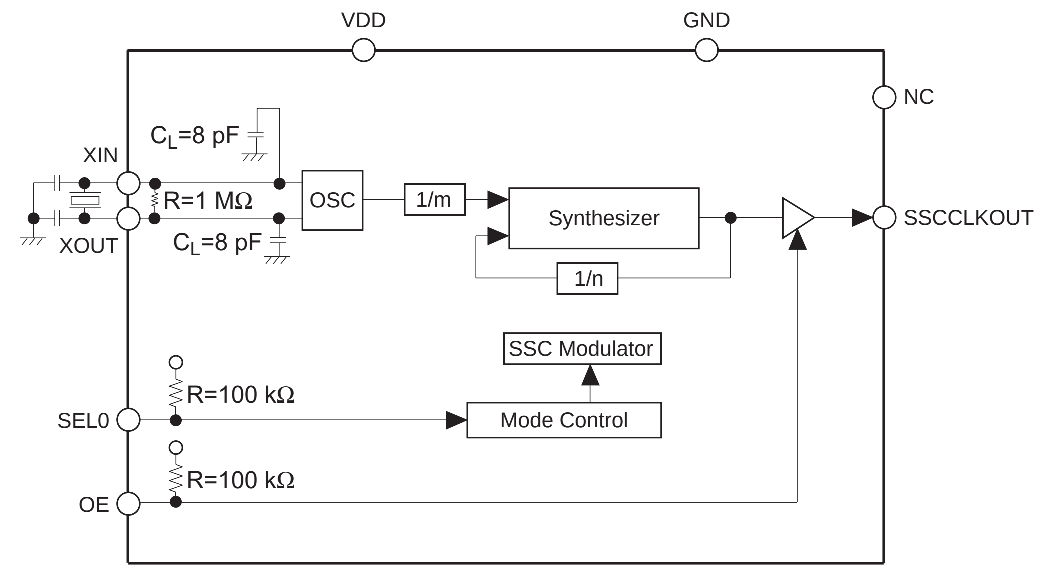
Features

- Supports 10 MHz to 60 MHz operation (Designed for XIN = 48 MHz)
- 1 copy of clock out with spread spectrum modulation @3.3 V
- Programmable spread spectrum modulation (–1.0%, –3.0% down spread modulation.)
- Output Enable function tri-state output

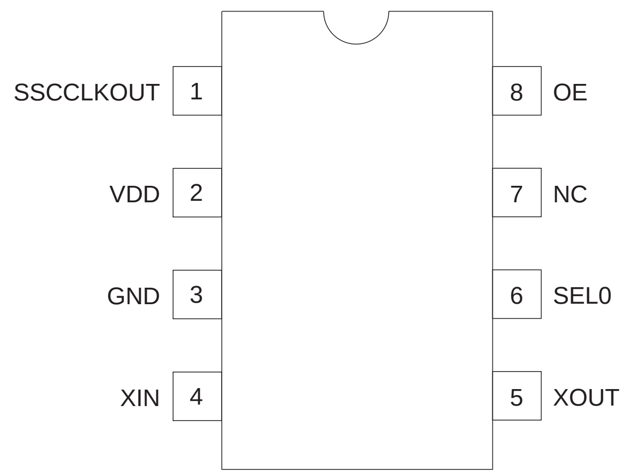
Key Specifications

- Supply voltages : VDD = 3.3 V±0.165 V
- Clock output duty cycle = 50±5%
- Cycle to cycle jitter = ±250 ps typ.
- Output slew rate = 0.8V/ns min.

Block Diagram



Pin Arrangement



(Top view)

SSC Function Table

OE: SEL0	Spread Percentage
0 0	Hi–Z
0 1	Hi–Z
1 0	–1.0%
1 1	–3.0%

Note: –3.0% SSC is selected for default by internal pull-up resistors.

Clock Frequency Table

XIN(MHz)	SSCCLKOUT(MHz)
48	48*[1]
24	24*[1]

Notes: 1. With spread spectrum modulation.

Pin Descriptions

Pin name	No.	Type	Description
GND	3	Ground	GND pin
VDD	2	Power	Power supplies pin. Normally 3.3 V.
NC	7	NC	Don't connect any VDD or GND.
SSCCLKOUT	1	Output	Spread spectrum modulated clock output.
XIN	4	Input	Oscillator input.
XOUT	5	Output	Oscillator output.
SEL0	6	Input	SSC mode select pin. LVCMOS level input. Pull-up by internal resistor. (100 kΩ).
OE	8	Input	Output Enable. Tri-state output when low. Pull–up by internal resistor (100 kΩ).

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	–0.5 to 4.6	V	
Input voltage	V_I	–0.5 to 4.6	V	
Output voltage *[1]	V_O	–0.5 to VDD+0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	VDD	3.135	3.3	3.465	V	
DC input signal voltage		–0.3	—	VDD+0.3	V	
High level input voltage	V_{IH}	2.0	—	VDD+0.3	V	
Low level input voltage	V_{IL}	–0.3	—	0.8	V	
Input clock duty cycle		45	50	55	%	

DC Electrical Characteristics

Ta = 25°C, VDD = 3.3 V

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	—	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Input current	I_I	—	—	±10	µA	V_I = 0 V or 3.465 V, VDD = 3.465 V, XIN pin
		—	—	±100		V_I = 0 V or 3.465 V, VDD = 3.465 V, SEL0, OE pins
Input capacitance	C_I	—		4	pF	SEL0, OE
Load capacitance*[1]	C_L	—	4	—	pF	Between Pin XIN and XOUT
Operating current		—	7	—	mA	XIN = 24 MHz, C_L = 0 pF, VDD = 3.3 V

Note: 1. Pin XIN and XOUT each has an 8 pF capacitance. When used with a crystal, the two capacitors combined load the crystal with 4 pF.
If driving XIN with a Reference clock signal, the load capacitance will be 8pF (typical).

DC Electrical Characteristics / SSC Clock Output

Ta = 25°C, VDD = 3.3 V

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V
Output current	I_{OH}	—	–30	—	mA	V_{OH} = 1.5 V
	I_{OL}	—	30	—		V_{OL} = 1.5 V

AC Electrical Characteristics / SSC Clock Output [Reference Value]

Ta = 25°C, VDD = 3.3 V, C_L = 15 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter [*1, 2]	t_{CCS}	—	| 250 |	| 300 |	ps	SSCCLKOUT, 24 MHz	SSC = –3.0% SELO = 1 Fig1
		—	| 250 |	| 300 |		SSCCLKOUT, 48 MHz	
Output frequency [*1, 2]		23.1	—	24.2	MHz	SSCCLKOUT, XIN = 24 MHz	SSC = –3.0% SELO = 1
		45.9	—	48.7		SSCCLKOUT, XIN = 48 MHz	
Slew rate [*1]	t_{SL}	0.8	—	—	V/ns	@48 MHz	0.4 V to 2.4 V
Clock duty cycle [*1]		45	50	55	%		
Output impedance [*1]		—	40	—	Ω		
Spread spectrum modulation frequency [*1]		—	33	—	KHz	@48 MHz SSCCLKOUT	
Input clock frequency		10	—	60	MHz		
Stabilization time [*1,3]		—	—	2	ms		
Output Enable/Disable time*[1,4]	t_{PZ}	—	—	100	ns		

Notes: 1. Parameters are target of design. Not 100% tested in production.
2. Cycle to cycle jitter and output frequency are included spread spectrum modulation.
3. Stabilization time is the time required for the integrated circuit to obtain phase lock of its input signal after power up.
4. Output Enable/Disable time is the time required for the integrated circuit to obtain output signal after the OE pin input.

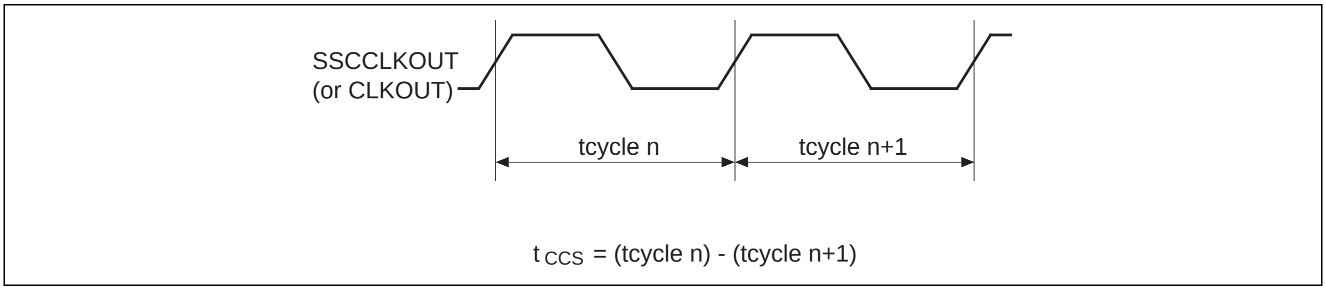


Figure 1 Cycle to cycle jitter

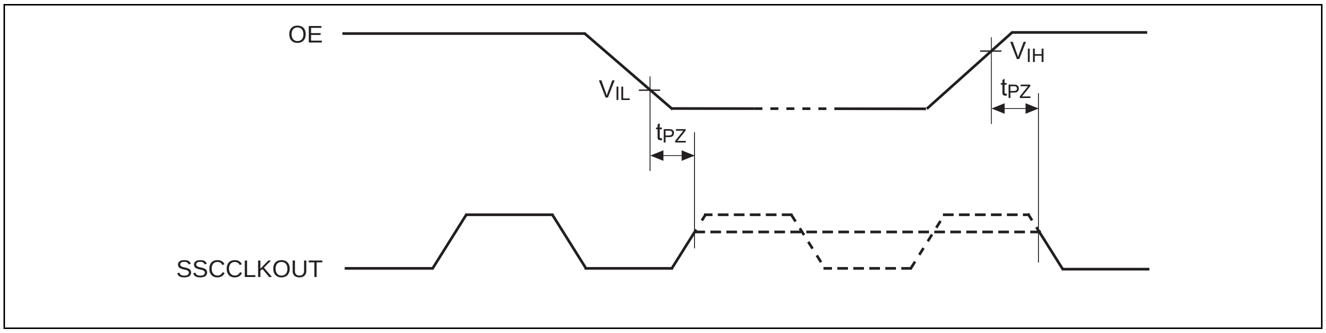


Figure 2 Output Enable/Disable time

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Application Information

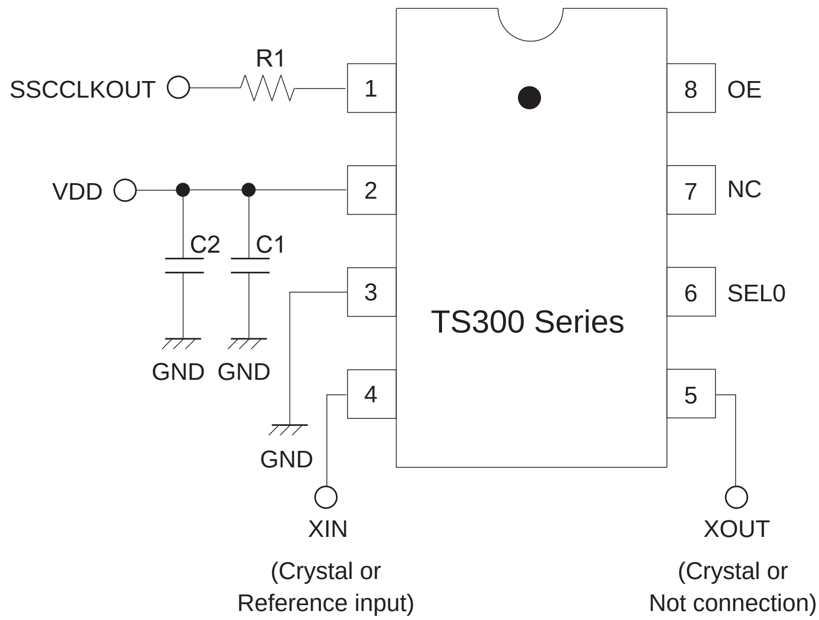
1. Recommended Circuit Configuration

The power supply circuit of the optimal performance on the application of a system should refer to Fig. 3.

VDD decoupling is important to both reduce Jitter and EMI radiation.

The C1 decoupling capacitor should be placed, as close to the VDD pin as possible, otherwise the increased trace inductance will negate its decoupling capability.

The C2 decoupling capacitor shown should be a tantalum type.



Notes: C1 = High frequency supply decoupling capacitor.
(0.1 µF recommended)
C2 = Low frequency supply decoupling capacitor.
(22 µF tantalum type recommended)
R1 = Match value to line impedance.
(22 Ω Reference value)

Figure 3 Recommended circuit configuration

2. Example Board Layout Configuration

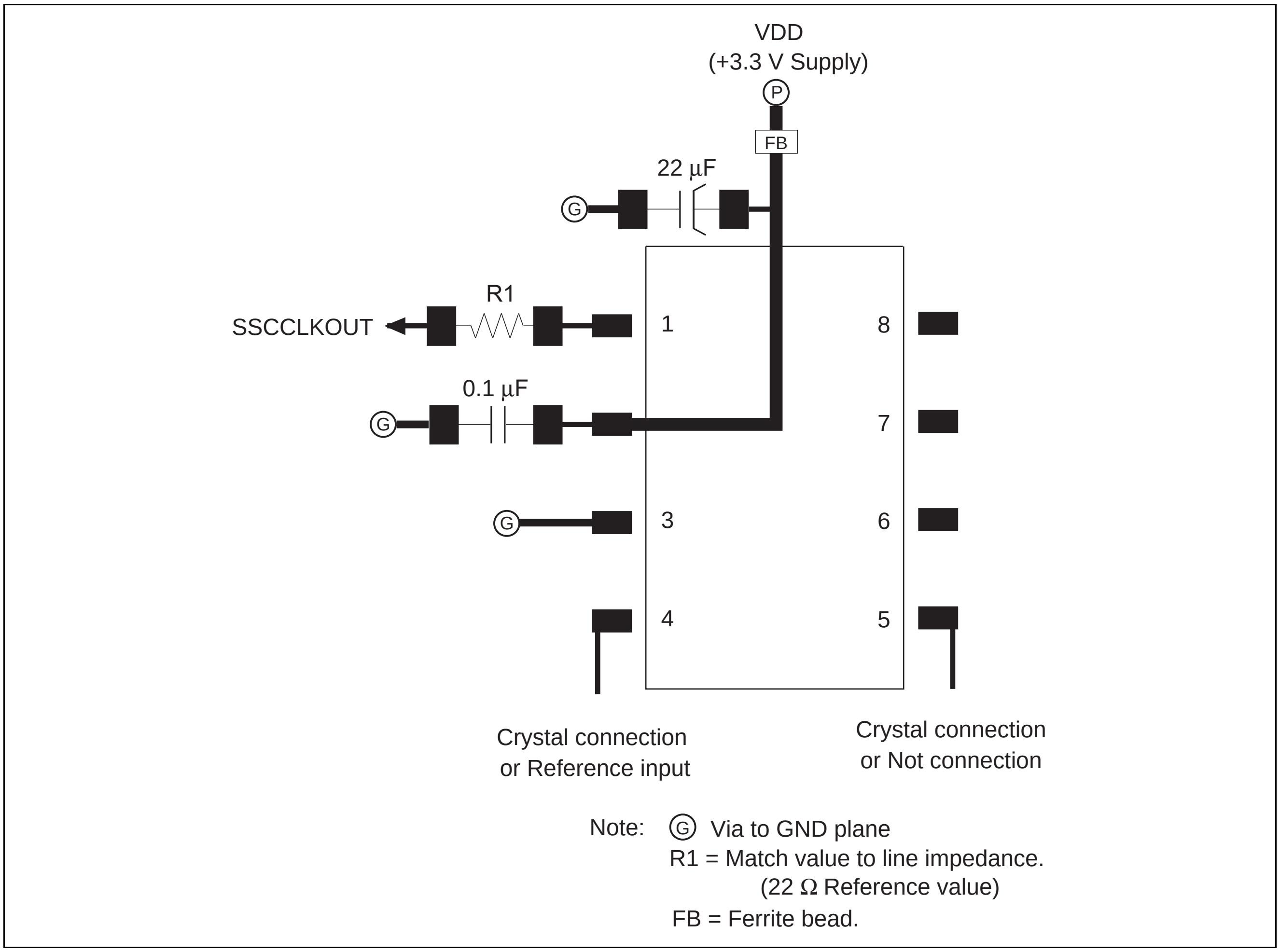


Figure 4 Example Board Layout

3. Example of TS300 EMI Solution IC's Application

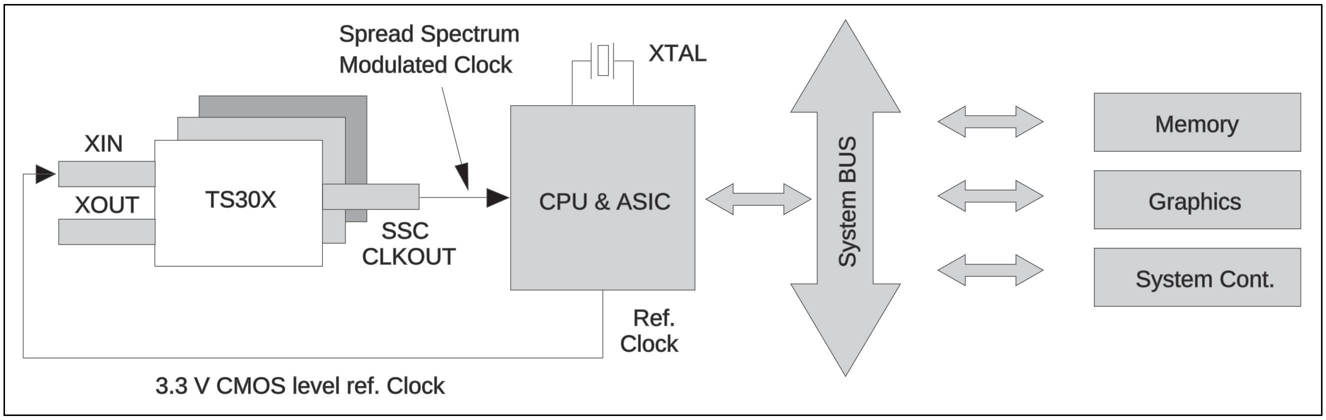


Fig 5 Ref. Clock Input Example

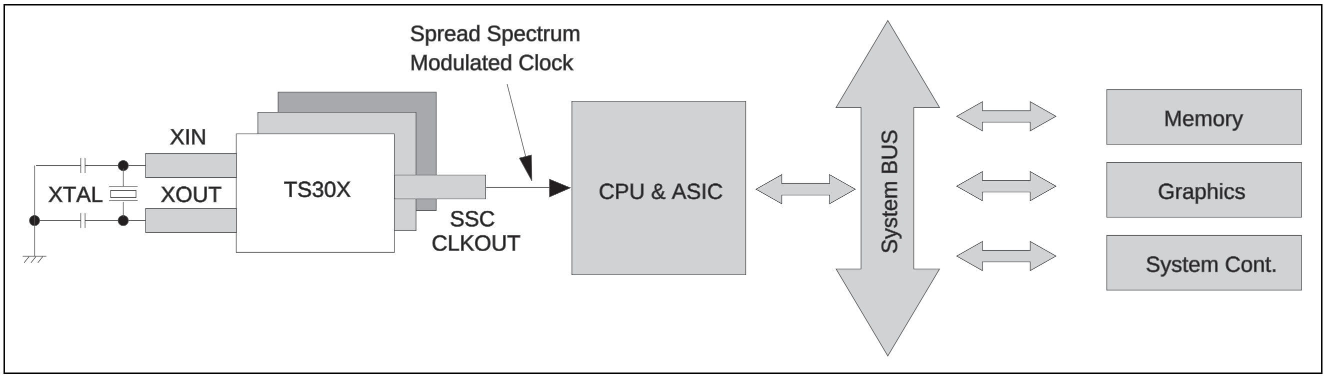


Fig 6 XTAL Ref. Clock Input Example

RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
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Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001