

Silicon Controlled Switch



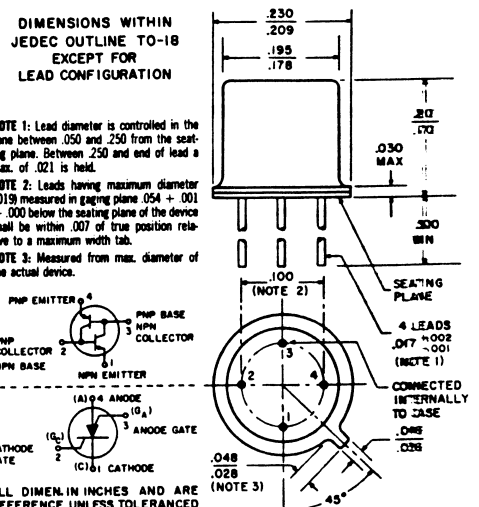
The General Electric Type 3N86 is a PLANAR PNP silicon controlled switch (SCS) offering outstanding circuit design flexibility by providing leads to all four semiconductor regions. Unique fabrication processes based on planar oxide passivation have resulted in high reliability and uniformity at low cost. The SCS is thoroughly characterized at temperature extremes to permit worst case circuit design. The 3N86 can be considered an integrated PNP-NPN transistor pair in a positive feedback configuration. As such it offers fewer connections, fewer parts, lower cost and better characterization than is available from two separate transistors. Its characterization permits it to be used as an extremely sensitive SCR, as a complementary SCR, or as a "transistor" with "latching" capabilities. Type 3N86 is intended for applications requiring extremely low holding current, high triggering sensitivity at either gate and high turn-off gain.

FEATURES:

- Completely eliminates rate effect problems
- Dynamic and static breakover voltages are identical
- Extremely high triggering sensitivity at both gates
- Low holding current
- High turn-off gain
- Design parameters specified at worst-case temperatures
- Characterized for SCR and complementary SCR type applications
- Characterized as PNP and also as transistor integrated pair
- All planar, completely oxide passivated
- Leads to all four semiconductor regions

absolute maximum ratings⁽¹⁾ (25°C) (unless otherwise specified)

Voltage			
Anode to cathode forward and reverse	65	volts	
Anode gate to anode reverse	65	volts	
Cathode gate to cathode reverse	5	volts	
Total Current			
Continuous DC forward ⁽²⁾	200	ma	
Peak recurrent forward (T _A = 100°C, 100 μsec. pulse width, 1% duty cycle)	1.0	amps	
Peak non-recurrent forward (10 μsec. pulse width)	5.0	amps	
Gate Current (Forward Bias)			
Continuous DC anode gate ⁽²⁾	100	ma	
Peak anode gate (T _A = 100°C, 100 μsec. pulse width, 1% duty cycle)	200	ma	
Peak cathode gate (T _A = 100°C, 100 μsec. pulse width, 1% duty cycle)	500	ma	
Continuous DC cathode gate	20	ma	
Dissipation			
Total power ⁽²⁾	400	mw	
Cathode gate power ⁽²⁾	100	mw	
Temperature			
Operating junction	-65 to +150	°C	
Storage	-65 to +200	°C	



NOTE 1: Symbols and nomenclature are defined below.

NOTE 2: Derate currents and power linearly to 150°C, the maximum rated temperature. The absolute maximum rating at any given temperature shall be in terms of the more conservative of the two parameters, i.e., current or power.

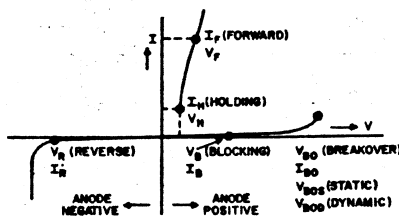


FIG. 1

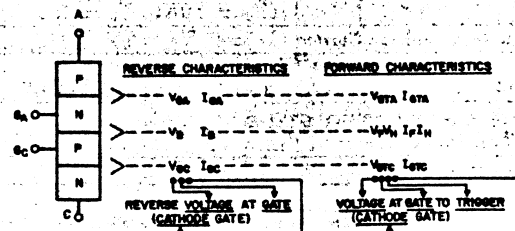


FIG. 2

DEFINITION OF TERMS USED IN SCS SPECIFICATIONS

PNPN devices available at present do not have a common nomenclature. In part, this is due to their different construction and varied applications. SCS nomenclature permits the reverse characteristics of all three junctions to be specified. The anode forward characteristic and gate triggering characteristics can also be specified fully. The principles used in assigning symbols are illustrated below and with outline drawing above.

SCS CHARACTERIZATION

CUTOFF CHARACTERISTICS

Parameter	Symbol ⁽¹⁾	Temp.	3N86	Units
Forward Blocking Current ($R_{GC} = 10K, V_{AC} = 65V$)	$I_{B\ max}$	@ 25°C @ 150°C	1.0 20	$\mu A\ max$ $\mu A\ max$
Reverse Blocking Current ($R_{GC} = 10K, V_{CA} = 65V$)	$I_{R\ max}$	@ 25°C @ 150°C	1.0 20	$\mu A\ max$ $\mu A\ max$
Cathode Gate Reverse Cutoff Current ($V_{GC} = -5V$)	I_{GC}	@ 25°C	20	$\mu A\ max$
Anode Gate Reverse Cutoff Current ($V_{GA} = -65V$)	I_{GA}	@ 25°C	1.0	$\mu A\ max$

CONDUCTING CHARACTERISTICS

Forward Voltage ($I_A = 200ma, R_{GC} = 10K$)	$V_{F\ max}$	@ 25°C @ -65°C	2.0 2.5	V max V max
Forward Voltage ($I_A = 100ma, I_{GA} = 50ma, R_{GC} = 10K$)	$V_{F\ max}$	@ 25°C	1.5	V max
Holding Current ($R_{GC} = 10K$)	$I_{H\ max}$	@ 25°C @ -65°C	0.2 0.8	ma max ma max
Holding Current ($R_{GC} = 10K, I_{GA} = 50ma$)	$I_{H\ max}$	@ 25°C @ -65°C	2.0 8.0	ma max ma max
Saturation Voltage (G_A to C) ($I_{GC} = 5ma, I_{GA} = 50ma, I_A = 0$)	$V_{CEsat\ NPN}$	@ 25°C	2.0	V max
Saturation Voltage (G_A to C) ($I_{GC} = 0, I_{GA} = 50ma, I_A = 5ma$)	$V_{CEsat\ PNP}$	@ 25°C	2.0	V max

TRIGGERING CHARACTERISTICS

Cathode Gate Current to Trigger (I_{GTC} from current source, $V_{AC} = 40V, R_A = 800\Omega$)	$I_{GTC\ max}$	@ 25°C @ -65°C	1.0 50	$\mu A\ max$ $\mu A\ max$
Cathode Gate Current to Trigger (I_{GTC} from current source, $V_{AC} = 40V, R_A = 800\Omega, I_{GA} = 50ma$)	$I_{GTC\ max}$	@ 25°C	50	$\mu A\ max$
Cathode Gate Voltage to Trigger ($V_{AC} = 40V, R_A = 800\Omega, R_{GC} = 10K, R_{GA} = \infty, I_{GTC}$ from current source)	$V_{GTC\ max}$	@ 25°C @ -65°C	.65 1.0	V max V max
Cathode Gate Voltage to Trigger ($V_{AC} = 40V, R_A = 800\Omega, R_{GC} = 10K, I_{GA} = 50ma, I_{GTC}$ from current source)	$V_{GTC\ max}$ $V_{GTC\ min}$	@ 25°C @ 25°C	0.8 0.4	V max V min
Anode Gate Current to Trigger (I_{GTA} from current source, $V_{AC} = 40V, R_C = 800\Omega, R_{GC} = 10K$)	$I_{GTA\ max}$	@ 25°C @ -65°C	0.1 0.25	ma max ma max
Anode Gate Voltage to Trigger (I_{GTA} from current source, $V_{AC} = 40V, R_C = 800\Omega, R_{GC} = 10K, R_{GA} = 1K$)	$V_{GTA\ max}$ $V_{GTA\ min}$	@ 25°C @ -65°C @ 150°C	0.8 1.0 0.4 0.2	V max V max V min V min

TRANSIENT CHARACTERISTICS

Turn-On Time ($V_{AC} = 20V, I_A = 100ma, I_{GC} = 100\mu A$) (See circuit, Figure 3)	$t_{on\ max}$	@ 25°C @ -65°C	1.5 2.0	$\mu s\ max$ $\mu s\ max$
Turn-On Time ($V_{AC} = 20V, I_A = 100ma, I_{GC} = 100\mu A, I_{GA} = 50ma$)	$t_{on\ max}$	@ 25°C	2.0	$\mu sec\ max$
Recovery Time ($V_{AC} = 20V, I_A = 100ma, R_{GC} = 10K$) (See circuit, Figure 4)	$t_{rec\ max}$	@ 25°C @ 150°C	15 25	$\mu s\ max$ $\mu s\ max$
Recovery Time ($V_{AC} = 20V, I_A = 100ma, R_{GC} = 10K, I_{GA} = 50ma$)	$t_{rec\ max}$	@ 25°C	15	$\mu sec\ max$
Collector Capacitance Voltage Gate to Gate = 20V	$C_{ob\ max}$	@ 25°C	15	pf
Rate of Rise of Forward Blocking Voltage	$dv/dt\ max$	@ 25°C	(see note 5)	V/ $\mu sec\ max$

Electrical characteristics (25°C) (unless otherwise specified)

DC CHARACTERISTICS

Parameter	PNP ¹	NPN ¹	Units
Collector to Base Breakdown Voltage ($I_C = [\pm]^{(a)} 1.0\mu A, I_B = 0$)	Min. -65	Max. 65	volts
Emitter to Base Breakdown Voltage ($I_C = 0, I_B [NPN] = 20\mu A, I_B [PNP] = -1\mu A$)	Min. -65	Max. 5	volts
Collector Saturation Voltage ($I_C = 50ma, I_B = 5ma$)			2 volts
Base Saturation Voltage ($I_C = 1ma, I_B = 5ma$)			0.9 volts
Forward Current Transfer Ratio ($V_{CB} = 0.5V, I_C = 3ma$)			20
Forward Current Transfer Ratio ($V_{CB} = -2.0V, I_C = -1ma$)			0.2

CUTOFF CHARACTERISTICS ($V_{AQ} = 65\ volts$)

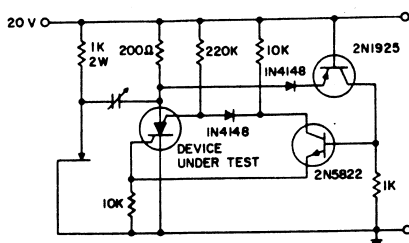
Collector to Emitter Leakage Current ($T_A = 150°C$)	I_{CEO}	-20	μA
($R_B = 10K\Omega, T_A = 150°C$)	I_{CER}	20	μA
Collector to Base Leakage Current ($I_B = 0, T_A = 150°C$)	I_{CBO}	-20	μA
Emitter to Base Leakage Current ($I_C = 0, T_A = 150°C$)	I_{EBO}	-20	μA
($V_{EB} = 5Vdc, I_C = 0$)	I_{EBO}	20	μA

TRANSIENT CHARACTERISTICS

Collector Capacitance ($I_B = 0, V_{EB} = [\pm]^{(a)} 20V$)	C_{ob}	15	15 pf
Gain Bandwidth Product	f_T	75	mc

NOTE 3: The transistor characterization is essentially a restatement of the SCS characterization and is meant to facilitate using the SCS as a complementary PNP-NPN integrated transistor pair.

NOTE 4: The $[\pm]$ sign indicates that the PNP and NPN transistors require opposite polarities as identified by the test conditions.
NOTE 5: The dv/dt rating is unlimited when the anode gate lead is returned to the anode voltage through a current limiting resistor.



RECOVERY TEST SET

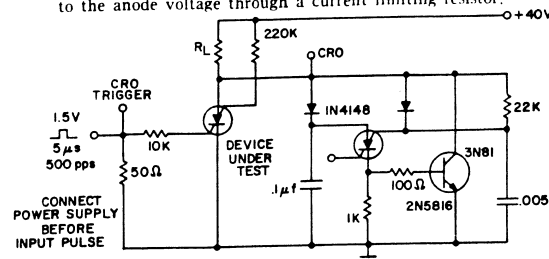
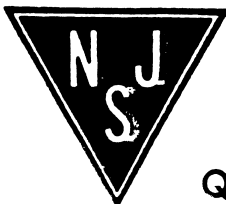


FIG. 4

TURN ON TIME TEST SET

TRANSISTOR CHARACTERIZATION



Quality Semi-Conductors