Ordering number : ENA1893

SANYO Semiconductors
DATA SHEET

LV766106F — Monolithic Linear IC For PAL/NTSC Color Television Sets VIF/SIF/Y/C/Deflection /CbCr IN Implemented in a Single Chip

Overview

The LV766106F is VIF/SIF/Y/C/D/Deflection /CbCr IN Implemented in a single chip for PAL/NTSC color television sets.(*1)

Functions

- VIF / SIF / Y / C / Deflection / CbCr IN / Implemented in a Single Chip with CPU
- I^2C Bus Control

Specifications

BIP Chip Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Allowable power dissipation	Pd max	Ta ≤65°C (*2)	1.3	W
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-55 to +150	°C
Maximum supply voltage	V62 max		6.0	V
	V4 max		6.0	V
Maximum supply current	I9 max		15	mA
	I20 max		20	mA
	I49 max		40	mA

(*1) μ-Controller Chip：LC87F3664A , F：FLASHROM=64Kbyte(Program_ROM:48Kbyte／character_ROM:16Kbyte)
(This production is produced and sold by SANYO under license of the Silicon Storage Technology Inc.)

(*2) Provided with a glass epoxy board (230×150×1.6 mm)

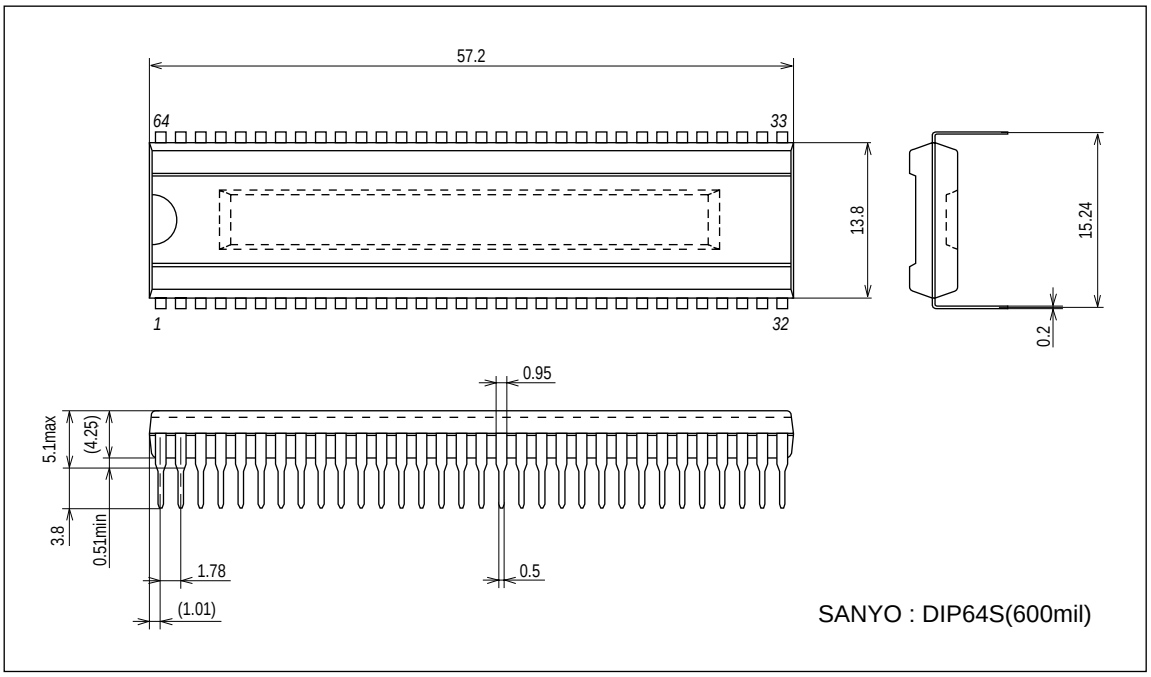
BIP Operating Conditions at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{62}		5.0	V
	V_4		5.0	V
Recommended supply current	I_9		10	mA
	I_{20}		13	mA
	I_{49}		30	mA
Operating supply voltage range	V_{62}		4.7 to 5.3	V
	V_4		4.7 to 5.3	V
Operating supply current range	I_9		7 to 13	mA
	I_{20}		11 to 15	mA
	I_{49}		28 to 35	mA

Package Dimensions

unit : mm (typ)

3300



µ-Controller Chip Absolute maximum ratings at Ta=25°C, V_{SS}=0V

Parameter		Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Maximum Supply voltage		V_{DD} max	CpuV_{DD}			-0.3	~	+6.0	V
Input voltage		V_I	XT1,RES#			-0.3	~	V_{DD}+0.3	
Output voltage		V_O1	XT2,FILT			-0.3	~	V_{DD}+0.3	
		V_O2	CpuV_{DD}2			-0.3	~	3.3V+0.3	
Input/output voltage		V_{IO}	Ports0,1			-0.3	~	V_{DD}+0.3	
High level output current	Peak output current	I_OPH	Ports04~07,1	・CMOS output ・For each pin.		-10			mA
	Mean Output current	I_OMH	Ports04~07,1	・CMOS output ・For each pin.		-1			
	Total output current	ΣI_OAH	Ports04~07,1	The total of all pins.		-25			
Low level output current	Peak output current	I_OPL	Ports0,1	For each pin				20	
	Mean output current	I_OML1	P02,P03,P06,P07 Ports1	For each pin				1	
		I_OML2	P00,P01,P04,P05	For each pin				8	
	Total output Current	ΣI_OAL1	P02,P03,P06,P07 Ports1	The total of all pins.				45	
		ΣI_OAL2	P00,P01,P04,P05	The total of all pins.				16	

µ-Conttoller Chip Recommended operating range at Ta=-10°C to +65°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions		V_{DD}[V]	Limits min.	typ.	max.	unit
Operating supply voltage range	V_{DD}	CpuV_{DD}	0.229µs≤tCYC≤200µs			4.5		5.5	V
Hold voltage	V_{HD}	CpuV_{DD}	RAMs and the registers data are kept in HOLD mode.			2.0		5.5	
High level input Voltage	V_IH1	Ports0,1, P00 port input /interrupt			4.5 to 5.5	0.3V_{DD} +0.7		V_{DD}	
	V_IH2	Port00 Watch-dog timer			4.5 to 5.5	0.9V_{DD}		V_{DD}	
	V_IH3	RES#			4.5 to 5.5	0.75V_{DD}		V_{DD}	
Low level input Voltage	V_IL1	Ports0,1, P00 port input /interrupt			4.5 to 5.5	V_{SS}		0.1V_{DD} +0.4	
	V_IL2	Port00 Watch-dog timer			4.5 to 5.5	V_{SS}		0.8V_{DD} -1.0	
	V_IL3	RES#			4.5 to 5.5	V_{SS}		0.25V_{DD}	
Operation cycle time (*3)	t_{CYC}1		All functions operating		4.5 to 5.5		0.231		µs
	t_{CYC}2		OSD and Data slicer are not operating		4.5 to 5.5	0.231		200	
Oscillation frequency range	FmV_{CO}1		Built-in VCO1 Oscillation System clock		4.5 to 5.5		13.0		MHz
	FmV_{CO}2 (*4)		Built-in VCO2 oscillation OSD clock	OCKSEL=0	4.5 to 5.5		12.5		
				OCKSEL=1			16.6		
	FmRC		Built-in RC oscillation		4.5 to 5.5	0.3	1.0	2.0	
	FsX'tal (*4)	XT1(P07), XT2(P06)	At the 32.768KHz crystal Oscillating See the figure1		4.5 to 5.5		32.768		KHz
Oscillation stabilizing time	tmsV_{CO}		・after the HOLD mode ・Power-On		4.5 to 5.5		300		mS

(Note) FLASH-ROM erase/write temperature range :Ta=25±2°C（V_{DD}=4.5 to 5.5V）

(*3) Relational expression between Tcyc and oscillation frequency;
1/1 frequency dividing: 3/FmVCO1, 1/2 frequency dividing: 6/FV_{CO}1.

(*4) OCKSEL is the selectable register for OSD clock frequency. (See the LC873600 users manual for details.)

(*5)When the base timer count of clock accuracy is necessary , use the port terminal (two ports) as the crystal oscillation.
(See the [12 µ-Controller Chip Crystal Oscillation Circuit and Sample Characteristics] for details.)

BIP Chip Electrical Characteristics at Ta=25°C, I_{CC}=I_9=10mA I_{CC}=I_{20}=13mA I_{CC}=I_{49}=30mA V_{CC}=V_{62}= V_4=5.0V

Parameter	Symbol	Conditions	min	typ	max	Unit
[Circuit voltage, current]						
Horizontal supply voltage	V_{20}	I_{20}=13mA	4.7	5.0	5.3	V
Logic supply voltage	V_9	I_9=10mA	3.0	3.3	3.6	V
RGB supply voltage	V_{49}	I_{49}=30mA	7.8	8.15	8.5	V
IF supply current	I_{62}	V_{62}=5.0V	56	65	74	mA
Video supply current	I_4	V_4=5.0V	65	77	89	mA
[VIF block]						
Maximum RFAGC voltage	VRFH	CW=80 dBμ, DAC=0	4.3	4.7	5	Vdc
Minimum RFAGC voltage	VRFL	CW=80 dBμ, DAC=63	0	0.3	0.7	Vdc
RF AGC Delay Pt (@DAC=0)	RFAGC0	DAC=0	90	–	–	dBμ
RF AGC Delay Pt (@DAC=63)	RFAGC63	DAC=63	–	–	80	dBμ
Input sensitivity	Vi	Output-3db	–	–	46	dBμ
Sync signal tip level	$V_O$tip	CW=80 dBμ	1.1	1.4	1.7	Vdc
Video output amplitude	V_O	80dBu,AM=78%,fm=15kHz	1.90	2.00	2.10	Vp_p
Video S/N	S/N	CW=80 dBμ	40	45	–	dB
C-S beat level	IC-S	V4.43MHz/V1.07MHz	35	–	–	dB
Differential gain	DG	80 dBμ, 87.5% Video MOD	–	5.0	15	%
Differential phase	DP	80 dBμ, 87.5% Video MOD	–	5.0	10.0	deg
APC pull-in range(U)	fPU		2.0	–	–	MHz
APC pull-in range(L)	fPL		1.5	–	–	MHz
NTSC Trap1(4.5MHz)	NTR1		–	–	-27	dB
BG Trap1(5.5MHz)	BTR1		–	–	-27	dB
I Trap1(6.0MHz)	ITR1		–	–	-27	dB
DK Trap1(6.5MHz)	DTR1		–	–	-27	dB
[SIF block]						
FM detection output voltage	SOADJ	FM=±50kHz	500	640	780	mVrms
FM limiting sensitivity	SLS	Output -3dB	–	–	60	dBμ
FM detection output f characteristics	SF	fm=100kHz	-1.0	0	5.0	dB
FM detection output distortion	STHD	FM=±50kHz	–	–	3.0	%
SIF S/N	SSN	D_{IN} Audio	45.0	–	–	dB
[AUDIO block]						
Volume gain (Stereo mode)	AVGT	1kHz	-3.0	0.0	+3.0	dB
Frequency characteristic (Stereo mode)	AFREQT		–	20	30	kHz
Total harmonic distortion (Stereo mode)	ATHDT	D_{IN} Audio	–	0.2	0.7	%
Output voltage noise (Stereo mode)	ANOT	D_{IN} Audio	–	-75	-70	dBV
Cross talk (Stereo mode)	ACTT	D_{IN} Audio	–	-80	-70	dB
Volume gain (Mono mode)	AVGM	1kHz	-3.0	0.0	+3.0	dB
Frequency characteristic (Mono mode)	AFREQM		–	20	30	kHz
Total harmonic distortion (Mono mode)	ATHDM	D_{IN} Audio	–	0.2	0.7	%
Output voltage noise (Mono mode)	ANOM	D_{IN} Audio	–	-75	-70	dBV
Mute	AMUTE	D_{IN} Audio	–	-80	-70	dB
L/R Balance	ABT	1kHz	-0.5	0	0.5	dB

Parameter	Symbol	Conditions	min	typ	max	Unit
[Video block]						
Video overall gain (Contrast max)	CONT127		11.0	13.5	16.0	dB
Contrast adjustment Characteristics (Normal/max)	CONT64		-7.0	-4.5	-2.0	dB
Contrast adjustment characteristics (Min/max)	CONT0		-18.0	-15.5	-11.0	dB
Video frequency Characteristics 1 NTSC	BW1	1.8MHz/100kHz , Y Filter.sys = 00	-6.0	-3.0	0.0	dB
Video frequency characteristics 2 PAL	BW2	2.2MHz/100kHz , Y Filter.sys = 01	-6.0	-3.0	0.0	dB
Video frequency characteristics 3 WIDE	BW3	2.3MHz/100kHz , Y Filter.sys = 10	-6.0	-3.0	0.0	dB
Video frequency characteristics 4 APF	BW4	3.4MHz/100kHz , Y Filter.sys = 00,Y APF=1	-6.0	-3.0	0.0	dB
Chroma trap amount PAL	CtrapP	Y Filter.sys = 01		-26.0	-20.0	dB
Chroma trap amount NTSC	CtrapN	Y Filter.sys = 00		-26.0	-20.0	dB
DC restoration rate 1	ClampG1	DC.Rest=00	95.0	100.0	105.0	%
DC restoration rate 2	ClampG2	DC.Rest=01	102.0	107.0	112.0	%
DC restoration rate 3	ClampG3	DC.Rest=10	105.0	112.0	120.0	%
DC restoration rate 4	ClampG4	DC.Rest=11	118.0	128.0	136.0	%
Y-DL TIME1	TdY1	Y Filter.Sys=00 Y Delay Ajust=0100		1.40		ns
Y-DL TIME2	TdY2	Y Filter.Sys=01 Y Delay Ajust=0100		1.20		ns
Y-DL TIME3	TdY3	Y Filter.Sys=11,Delay Test=1 Y Delay Ajust=0100		1.60		ns
Y-DL TIME4	TdY4	Y Filter.Sys=10 Y Delay Ajust=0100		1.15		ns
Y-DL TIME Ajust1	TdYa1	Y Filter.Sys=00 Y Delay Ajust=0000		1.25		ns
Y-DL TIME Ajust2	TdYa2	Y Filter.Sys=00 Y Delay Ajust=0111		1.45		ns
Black stretch gain max	BKSTmax	Blk.Str.Gain=10 ,Blk.Str.Start=01	17.0	26.0	42.0	IRE
Black stretch gain mid	BKSTmid	Blk.Str.Gain=01 ,Blk.Str.Start=01	8.0	19.0	33.0	IRE
Black stretch gain min	BKSTmin	Blk.Str.Gain=00 ,Blk.Str.Start=01	1.0	11.0	26.0	IRE
Black stretch start point max (70IRE ΔV)	BKSTTHmax	Blk.Str.Gain=01 ,Blk.Str.Start=10	-4.0	0.0	6.0	IRE
Black stretch start point mid (50IRE ΔV)	BKSTTHmid	Blk.Str.Gain=01 ,Blk.Str.Start=01	-5.0	0.0	5.0	IRE
Black stretch start point min (40IRE ΔV)	BKSTTHmin	Blk.Str.Gain=01 ,Blk.Str.Start=00	-5.0	0.0	5.0	IRE
Sharpness variability range NTSC (trap 1 mid)	Sharp32T1	F=2.2MHz,Y Filter.Sys=00, Y Gamma Start=11,C_Kill.ON=1	1.5	3.0	6.0	dB
(trap 1 max)	Sharp63T1	F=2.2MHz,Y Filter.Sys=00, Y Gamma Start=11,C_Kill.ON=1	9.0	12.0	15.0	dB
(trap 1 min)	Sharp0T1	F=2.2MHz,Y Filter.Sys=00, Y Gamma Start=11,C_Kill.ON=1	-14.0	-9.0	-7.5	dB
Sharpness variability range PAL (trap 2 mid)	Sharp32T2	F=2.7MHz,Y Filter.Sys=01, Y Gamma Start=11,C_Kill.ON=1	1.5	3.0	6.0	dB
(trap 2 max)	Sharp63T2	F=2.7MHz,Y Filter.Sys=01, Y Gamma Start=11,C_Kill.ON=1	8.5	11.5	15.0	dB
(trap 2 min)	Sharp0T2	F=2.7MHz,Y Filter.Sys=01, Y Gamma Start=11,C_Kill.ON=1	-14.0	-11.0	-8.0	dB
Sharpness variability range 6MHz TRAP (trap 4 mid)	Sharp32T4	F=3.0MHz,Y Filter.Sys=10, Y Gamma Start=11,C_Kill.ON=1	1.5	5.0	8.0	dB
(trap 4 max)	Sharp63T4	F=3.0MHz,Y Filter.Sys=10, Y Gamma Start=11,C_Kill.ON=1	10.0	13.5	17.0	dB
(trap 4 min)	Sharp0T4	F=3.0MHz,Y Filter.Sys=10, Y Gamma Start=11,C_Kill.ON=1	-14.0	-11.0	-7.0	dB

Parameter	Symbol	Conditions	min	typ	max	Unit
White peak limiter effective point1	WPL1	APL=100% WPL=00	130.0	160.0	190.0	IRE
White peak limiter effective point2	WPL2	APL=100% WPL=01	90.0	125.0	140.0	IRE
White peak limiter effective point3	WPL3	APL=100% WPL=10	70.0	105.0	130.0	IRE
White peak limiter effective point4	WPL4	APL=100% WPL=11	50.0	85.0	120.0	IRE
Y gamma Start effective point 1	YGST1	Y Gamma Start=00 Y Gamma GAIN=01		55		IRE
Y gamma Start effective point 2	YGST2	Y Gamma Start=01 Y Gamma GAIN=01		65		IRE
Y gamma Start effective point 3	YGST3	Y Gamma Start=10 Y Gamma GAIN=01		68		IRE
Y gamma gain 1	YGGA1	Y Gamma Start=01 Y Gamma GAIN=00		220		IRE
Y gamma gain 2	YGGA2	Y Gamma Start=01 Y Gamma GAIN=01		250		IRE
Y gamma gain 3	YGGA3	Y Gamma Start=01 Y Gamma GAIN=10		260		IRE
Gray Mode Level	GRAY	GLAY MODE=1, Cross B/W=10	12.5	16.0	19.5	IRE
Horizontal/vertical blanking output level	RGBBLK		0.0	0.1	0.5	V
Pre-shoot adjust1	PreShoot1	Pre-shoot adj.=00	0.92	0.97	1.02	
Pre-shoot adjust2	PreShoot2	Pre-shoot adj.=11	1.08	1.13	1.18	
Over-shoot adjust	OverShoot	Over-shoot adj.=11	1.08	1.13	1.18	
[RGB output(cutoff drive)block]						
Brightness control (Normal)	BRT64		1.8	2.3	2.7	V
Brightness control (Normal-H)	BRT64H		3.3	3.7	4.1	V
Hi brightness (max)	BRT127		40.0	50.0	60.0	IRE
Low brightness (min)	BRT0		-60.0	-50.0	-40.0	IRE
Cutoff control (min)	Vbias0		2.3	2.8	3.3	V
(Bias control) (max)	Vbias255		3.1	3.6	4.1	V
Resolution	Vbiassns		-	3.5	-	mV/Bit
Sub-bias control Resolution	Vsbiassns		—	7	—	mV/Bit
RGB Drive adjustment Maximum output	RGBout127		1.5	1.7	2.3	Vpp
RGB Output attenuation	RGBout0		5	10	13	dB
[Video SW block]						
Video signal input 1DC voltage	V_{IN}1DC	Video SW.=00	1.9	2.2	2.5	V
Video signal input 1AC voltage	V_{IN}1AC	Video SW.=00		1		Vpp
Video signal input 2DC voltage	V_{IN}2DC	Video SW.=01	1.9	2.2	2.5	V
Video signal input 2AC voltage	V_{IN}2AC	Video SW.=01		1		Vpp
Video signal input 3DC voltage	V_{IN}3DC	Video SW.=10	1.9	2.2	2.5	V
Video signal input 3AC voltage	V_{IN}3AC	Video SW.=10		1		Vpp
Video signal input 4DC voltage	V_{IN}4DC	Video SW.=11	1.9	2.2	2.5	V
Video signal input 4AC voltage	V_{IN}4AC	Video SW.=11		1		Vpp
SVO pin DC voltage	SVODC	Video SW.=01,SVO SW=1 YCMIX=0	1.6	1.9	2.2	V
SVO pin AC voltage	SVOAC	Video SW.=01,SVO SW=1 YCMIX=0	1.7	2	2.3	Vpp
SVO pin Ycmix AC Voltage	SVOYC	Video SW.=01,SVO SW=1 YCMIX=1	0.1	0.14	0.18	Vpp

Parameter	Symbol	Conditions	min	typ	max	Unit
[Chroma block]: PAL/NTSC common						
B-Y/Y amplitude ratio	CLRBY		75	100	150	%
Color control characteristics 1	CLRMN	Color MAX/CEN	1.6	2.0	2.4	ratio
Color control characteristics 2	CLRMM	Color MAX/MIN	30	40	50	dB
Color control sensitivity	CLRSE		1	2	4	%/bit
fsc output level	FSC40	a reference value		350		mVpp
Residual higher harmonic level B	E_CAR_B				300	mVpp
Residual higher harmonic level R	E_CAR_R				300	mVpp
Residual higher harmonic level G	E_CAR_G				300	mVpp
[Chroma block]: PAL						
ACC amplitude characteristics 1	ACCM1_P	Input:+6dB/0dB 0dB=40IRE	0.7	1.0	1.2	ratio
ACC amplitude characteristics 2	ACCM2_P	Input:-20dB/0dB	0.7	1.0	1.1	ratio
Demodulation output ratio R-Y/B-Y:PAL	RB_P	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle=Center	0.50	0.56	0.67	ratio
Demodulation output ratio G-Y/B-Y :PAL	GB_P	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle=Center, R-Y= no-signal	-0.24	-0.19	-0.17	ratio
Demodulation output ratio G-Y/R-Y :PAL	GR_P	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle=Center, B-Y= no-signal	-0.56	-0.51	-0.46	ratio
Demodulation angle R-Y/B-Y :PAL	ANGRB_P	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle=Center	85	90	95	°C
Killer operating point 0 (PAL)	KILLP0	0dB=40IRE	-35		-22	dB
Killer operating point 3 (PAL)	KILLP3	0dB=40IRE	-38		-24	dB
Difference between two Killer operating points (PAL)	DKILLP	KILLP0-KILLP3	0.5		6.0	dB
APC pull-in range (+)	PULIN+_P		350			Hz
APC pull-in range (-)	PULIN-_P				-350	Hz
[Chroma block]:NTSC						
ACC amplitude characteristics 1	ACCM1_N	Input:+6dB/0dB 0dB=40IRE	0.7	1.0	1.2	ratio
ACC amplitude characteristics 2	ACCM2_N	Input:-20dB/0dB	0.7	1.0	1.1	ratio
Demodulation output ratio R-Y/B-Y: NTSC	RB_N	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle =Center	0.80	0.90	1.00	ratio
Demodulation output ratio G-Y/B-Y: NTSC	GB_N	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle =Center	0.22	0.27	0.38	ratio
Demodulation angle B-Y/R-Y : NTSC	ANGBR_N	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle =Center	95	105	111	°C
Demodulation angle G-Y/B-Y : NTSC	ANGGB_N	R-Y/B-Y_GainBalance, R-Y/B-Y_Angle =Center	230	240	250	°C
Killer operating point 0 (NTSC)	KILLN0	0dB=40IRE	-40		-27	dB
Killer operating point 3 (NTSC)	KILLN3	0dB=40IRE	-43		-29	dB
Difference between two Killer operating points (NTSC)	DKILLN	KILLN0-KILLN3	0.5		6.0	dB
APC pull-in range (+)	PULIN+_N		350			Hz
APC pull-in range (-)	PULIN-_N				-350	Hz
Tint center	TINCEN		-10	0	10	deg
Tint variable range (+)	TINT+				-35	deg
Tint variable range (-)	TINT-		35			deg
Cr Output amplitude	CBCR-R	CbCr_IN=1 ,Cross B/W=01	2.5		5.0	Vpp
Cb Output amplitude	CBCR-B	CbCr_IN=1 ,Cross B/W=01	3.25		5.75	Vpp

Parameter	Symbol	Conditions	min	typ	max	Unit
[Filter block]:Chroma BPF Characteristic						
C-BPF1A (3.93MHz)	CBPF1A	Reference: 4.43MHz C.Filter.Sys=10	-7.5	-3.0	-1.0	dB
C-BPF1B (4.73/4.13MHz)	CBPF1B	Reference: 4.13MHz C.Filter.Sys=10	-2.5	1.5	5.5	dB
C-BPF1C (4.93/3.93MHz)	CBPF1C	Reference: 3.93MHz C.Filter.Sys=10	-3.5	2.0	7.5	dB
C-BPF2A (3.93MHz)	CBPF2A	Reference: 4.43MHz C.Filter.Sys=11	-6.0	-3.0	-1.0	dB
C-BPF2B (4.73/4.13MHz)	CBPF2B	Reference: 4.13MHz C.Filter.Sys=11	-4.0	0.0	4.0	dB
C-BPF2C (4.93/3.93MHz)	CBPF2C	Reference: 3.93MHz C.Filter.Sys=11	-5.5	0.0	5.5	dB
APC pull-in range (+)	PULIN+_N		350			Hz
APC pull-in range (-)	PULIN-_N				-350	Hz
Tint center	TINCEN		-10	0	10	°C
Tint variable range (+)	TINT+				-40	°C
Tint variable range (-)	TINT-		40			°C
Cr Output amplitude	CBCR-R	CbCr_IN=1 ,Cross B/W=01	1.7		3.4	Vpp
Cb Output amplitude	CBCR-B	CbCr_IN=1 ,Cross B/W=01	1.8		3.7	Vpp
[Filter block]:Chroma BPF Characteristic						
C-BPF1A (3.93MHz)	CBPF1A	Reference: 4.43MHz C.Filter.Sys=10	-6.0	-3.0	-1.0	dB
C-BPF1B (4.73/4.13MHz)	CBPF1B	Reference: 4.13MHz C.Filter.Sys=10	-2.5	1.5	5.5	dB
C-BPF1C (4.93/3.93MHz)	CBPF1C	Reference: 3.93MHz C.Filter.Sys=10	-3.5	2.0	7.5	dB
C-BPF2A (3.93MHz)	CBPF2A	Reference: 4.43MHz C.Filter.Sys=11	-6.0	-3.0	-1.0	dB
C-BPF2B (4.73/4.13MHz)	CBPF2B	Reference: 4.13MHz C.Filter.Sys=11	-4.0	0.0	4.0	dB
C-BPF2C (4.93/3.93MHz)	CBPF2C	Reference: 3.93MHz C.Filter.Sys=11	-5.5	0.0	5.5	dB
[Deflection block]						
Horizontal free-running frequency	FH		15470	15670	15870	Hz
Horizontal pull-in range	FH PULL		±400			Hz
Horizontal output pulse width	H duty		36.1	37.6	39.1	µs
Horizontal output pulse saturation voltage	V Hsat		0	0.2	0.4	V
Vertical free-running cycle 50	VFR50		312.0	312.5	313.0	H
Vertical free-running cycle 60	VFR60		262.0	262.5	263.0	H
Horizontal output pulse phase	HPHCENpal		3.8	5.8	7.8	µs
Horizontal output pulse phase	HPHCENnt		3.8	5.8	7.8	µs
Horizontal position adjustment range	HPH range	5bit		±1.8		µs
Horizontal position adjustment maximum variability width	HPH step				180.0	ns
Horizontal blanking left @0	BLKL0	H.BLK.L:000	8000	9000	10000	ns
Horizontal blanking left @7	BLKL7	H.BLK.L:111	11500	12500	13500	ns
Horizontal blanking right @0	BLKR0	H.BLK.R:000	-1600	-600	400	ns
Horizontal blanking right @7	BLKR7	H.BLK.R:111	1800	2800	3800	ns
Horizontal output stop voltage	H stop	reference	3.30	3.60	3.90	V
Horizontal phase bow correction @16	HBOW16		-0.5	0	0.5	µs
Horizontal phase bow correction @0	HBOW0		0.7	1.2	1.7	µs
Horizontal phase bow correction @31	HBOW31		-1.5	-1.0	-0.5	µs
Horizontal phase angle correction @16	HANG16		-0.5	0	0.5	µs
Horizontal phase angle correction @0	HANG0		0.4	0.9	1.4	µs
Horizontal phase angle correction @31	HANG31		-1.3	-0.8	-0.3	µs

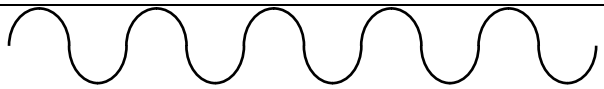
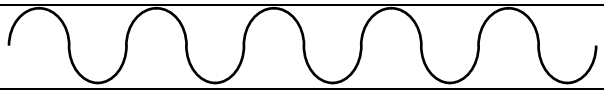
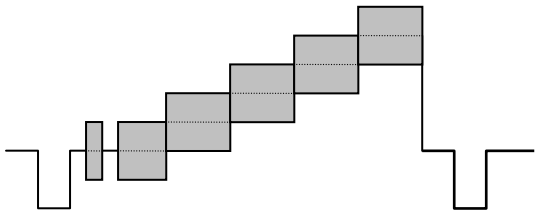
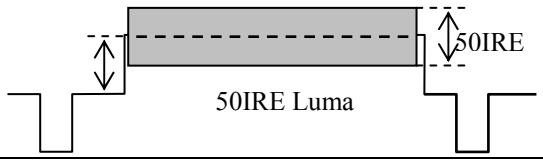
Parameter	Symbol	Conditions	min	typ	max	Unit
<Vertical screen size adjustment>						
Vertical ramp output amplitude PAL @64	Vspal64	V.SIZE:1000000	0.75	1.05	1.35	Vp-p
Vertical ramp output amplitude NTSC @64	Vsnt64	V.SIZE:1000000	0.75	1.05	1.35	Vp-p
Vertical ramp output amplitude PAL @0	Vspal0	V.SIZE:0000000	0.30	0.60	0.9	Vp-p
Vertical ramp output amplitude NTSC @0	Vsnt0	V.SIZE:0000000	0.30	0.60	0.9	Vp-p
Vertical ramp output amplitude PAL @127	Vspal127	V.SIZE:1111111	1.25	1.55	1.85	Vp-p
Vertical ramp output amplitude NTSC @127	Vsnt127	V.SIZE:1111111	1.25	1.55	1.85	Vp-p
<Vertical screen position adjustment>						
Vertical ramp DC voltage @32	Vdc32	V.DC:10000	2.10	2.40	2.70	Vdc
Vertical ramp DC voltage @0	Vdc0	V.DC:00000	1.80	2.10	2.40	Vdc
Vertical ramp DC voltage @63	Vdc63	V.DC:11111	2.55	2.85	3.15	Vdc
Vertical position @8	Vshift8	V.SHIFT:1000	500	550	600	µs
Vertical position @0	Vshift0	V.SHIFT:0000	0	50	100	µs
Vertical position @15	Vshift15	V.SHIFT:1111	950	1000	1050	µs
<High-voltage dependent vertical size correction>						
Vertical size Correction @0	Vpsizecomp	V.COMP:000	0.89	0.93	0.97	ratio
<Vertical screen linearity adjustment>						
Vertical linearity @16	Vlin16	V.LIN:10000	0.7	1.00	1.30	ratio
Vertical linearity @0	Vlin0	V.LIN:00000	1.30	1.60	1.90	ratio
Vertical linearity @31	Vlin31	V.LIN:11111	0.35	0.65	0.95	ratio
Vertical S-shaped correction @16	Vscor16	V.SC:10000	0.70	1.00	1.30	ratio
Vertical S-shaped correction @0	Vscor0	V.SC:00000	1.10	1.40	1.70	ratio
Vertical S-shaped correction @31	Vscor31	V.SC:11111	0.30	0.60	0.90	ratio
<High-voltage dependent horizontal size correction>						
Horizontal size correction @0	H size comp	H.COMP:000	0.18	0.28	0.38	V

Test Conditions at Ta=25°C, $I_{CC}=I_9$=10mA, $I_{CC}=I_{20}$=13mA, $I_{CC}=I_{49}$=30mA, $V_{CC}=V_{62}= V_4$=5.0V

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Circuit voltage,current]					
Horizontal supply voltage (pin 20)	V_{20}	20	No signal	Apply a current of 13mA to pin 20 and measure the voltage at pin 20.	Initial
Logic supply voltage (pin 9)	V_9	9	No signal	Apply a current of 11mA to pin 9 and measure the voltage at pin 9.	Initial
RGB supply voltage(pin 49)	I_{49}	49	No signal	Apply a current of 12mA to pin 49 and measure the voltage (V) at pin49.	Initial
IF supply current(pin 62)	I_{62}	62	No signal	Apply a voltage of 5.0V to pin 62 and measure the incoming DC current (mA). (IF AGC 2.5V applied)	Initial
Video / vertical supply current (pin 4)	I_4	4	No signal	Apply a voltage of 5.0V to pin 4 and measure the incoming DC current (mA).	Initial

• VIF Block Input Signals and Test Conditions

1. Input signals must be input to the PIF IN (pin 56) in the Test Circuit.
2. Input signal voltage values are the levels at the VIF IN (pin 56) in the Test Circuit.
3. Signal contents and signal levels
4. Bus control condition: VIF SYS.SW=”000”, APC.SIS.TEST="0",SVO.SW="0",VIDEO LEVEL=”ADJ

Input signal	Waveform	Conditions
SG1		38.9MHz
SG2		34.47MHz
SG3		33.4MHz
SG4		Frequency variable
SG5		38.9MHz 87.5% Video Mod. 10-stairstep wave (Subcarrier: 4.43MHz)
SG6		38.9MHz fm=15kHz,AM=78%
SG7		38.9MHz, 90dBu 87.5% Video Mod. 50IRE Luma (Carrier: variable)

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[VIF block]					
Maximum RF AGC voltage	VRFH	58	SG1 80dBμ	Measure the DC voltage at pin 58.	RF.AGC=”000000”
Minimum RF AGC voltage	VRFL	58	SG1 80dBμ	Measure the DC voltage at pin 58.	RF.AGC=”111111”
RF AGC Delay Pt (@DAC=0)	RFAGC0	58	SG1	Obtain the input level at which the DC voltage at pin 58 becomes 2.5V.	RF.AGC=”000000”
RF AGC Delay Pt (@DAC=63)	RFAGC63	58	SG1	Obtain the input level at which the DC voltage at pin 58 becomes 2.5V.	RF.AGC=”111111”
Input sensitivity	Vi	61	SG6	Using an oscilloscope, observe the level at pin 61 and obtain the input level at which the waveform's amplitude becomes 1.4Vp-p.	
Sync tip level	$V_O$tip	61	SG1 80dBμ	Measure the DC voltage at pin 61.	
Video output amplitude	V_O	61	SG6 80dBμ	Using an oscilloscope, adjust the waveform's amplitude at pin 61 to about 2Vpp and measure the waveform’s amplitude. * After this measurement, set "Video Level DAC" to the value adjusted .	
Video S/N	S/N	61	SG1 80dBμ	Measure the noise voltage (Vsn) at pin 61 with an RMS voltmeter through a 10kHz to 5.0MHz band-pass filter and calculate 20log(1.43/Vsn).	
C-S beat level	IC-S	61	SG1 SG2 SG3	Input a 80dBμ SG1 signal and measure the DC voltage (V60) at pin 60. Mix SG1=74dBμ, SG2=64dBμ, and SG3=64dBμ to enter the mixture in the VIF IN. Apply V60 to pin 60 from an external DC power supply. Using a spectrum analyzer, measure the difference between pin 61’s 4.43MHz component and 1.07MHz component.	
Differential gain	DG	61	SG5 80dBμ	Using a vector scope, measure the level at Pin 61.	
Differential phase	DP	61	SG5 80dBμ	Using a vector scope, measure the level at Pin 61.	
APC pull-in range (U),(L)	fPU, fPL	61	SG4 80dBμ	Connect an oscilloscope to pin 61 and adjust the SG4 frequency to a frequency higher than 38.9MHz to bring the PLL into unlocked mode. (A beat signal appears.) Lower the SG4 frequency and measure the frequency at which the PLL locks again. In the same manner, adjust the SG4 frequency to a lower frequency to bring the PLL into unlocked mode. Higher the SG4 frequency and measure the frequency at which the PLL locks again.	
NT Trap1 (4.5MHz)	NTR1	61	SG7	Determine the output level difference between carrier frequencies of 1MHz and 4.5MHz.(Reference:1MHz)	SIF.SYS=”00”
BG Trap 1 (5.5MHz)	BTR1	61	SG7	Determine the output level difference between carrier frequencies of 1MHz and 5.5MHz.(Reference:1MHz)	SIF.SYS=”01”
I Trap1 (6.0MHz)	ITR1	61	SG7	Determine the output level difference between carrier frequencies of 1MHz and 6.0MHz.(Reference:1MHz)	SIF.SYS=”10”
DK Trap1 (6.5MHz)	DTR1	61	SG7	Determine the output level difference between carrier frequencies of 1MHz and 6.5MHz.(Reference:1MHz)	SIF.SYS=”11”

•SIF Block (FM block) Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. Bus control condition: IF.AGC.SW="1", SIF.SYS="01",DEEM-TC="0",FM.GAIN="0"
2. SW: IF1="ON", pin 19=5V
3. Input signals are input to pin 52 and the carrier frequency is 5.5MHz.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
FM detection output voltage	SOADJ	64	90dBμ, fm=400Hz, FM=±50kHz	Measure the 400 Hz component (SV1:mVrms) of the FM detection output at pin 64.	
FM limiting sensitivity	SLS	64	fm=400Hz, FM=±50kHz	Measure the input level (dBμ) at which the 400Hz component of the FM detection output at pin 64 becomes -3dB relative to SV1.	
FM detection output f characteristics (fm=100kHz)	SF	64	90dBμ, fm=100kHz FM=±50kHz	Set SW: IF1="OFF". Measure (SV2: mVrms) the FM detection output of pin 64. Calculate as follows: SF=20log(SV1/SV2) [dB]	
FM detection output distortion	STHD	64	90dBμ, fm=400Hz, FM=±50kHz	Measure the distortion factor of the 400Hz component of the FM detection output at pin 64.	
SIF.S/N	SSN	64	90dBμ, CW	Measure the noise level (DIN AUDIO, SV4:mVrms) at pin 64. Calculate as follows: SSN=20log(SV1/SV4) [dB]	

•Audio Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

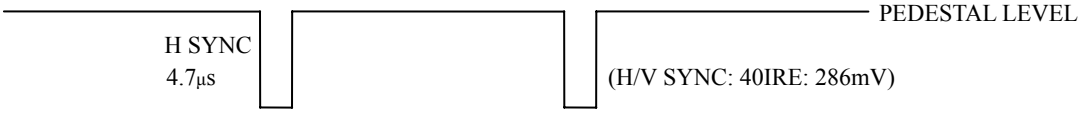
1. Bus control condition:
   Audio Mute ="0", A.MONI.SW="1", FM MUTE="1", Audio SW ="00",
   VOL FIL="0", IF AGC="1"MONO Mode="0", Volume (L/MONO) ="0000000"
2. Enter an input signal EXT1/EXT2-LIN from pin 2/pin8.
3. Enter an input signal EXT1/EXT2-RIN from pin 1/pin7.
4. Output signal LOUT is output to pin 50.
5. Output signal ROUT is output to pin 51.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[AUDIO block]					
Volume gain (Stereo mode)	AVGT	50	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz,300mVrms	Measure the 1kHz component (V1:mVrms) at the LOUT(50PIN) and calculate as follows: AVGT=20log(V1/300) [dB]	
Maximum output voltage (Stereo mode)	AVOT	2	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz	When the distortion (DIN.AUDIO) of the LOUT(pin50) is 1%, Measure the voltage level at the EXT-LIN (pin 2).	
Frequency characteristic (Stereo mode)	AFREQT	2	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =300mVrms	Measure the voltage level (V2:mVrms) at the LOUT(pin50) and calculate as follows: AFT=20log(V2/300) [dB] When the AFT is –3dB, Measure the frequency at the EXT-LIN (pin 2).	
Total harmonic distortion (Stereo mode)	ATHDT	50	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz,300mVrms	Measure the distortion (DIN.AUDIO) of the 1kHz component at the LOUT (50PIN).	
Output voltage noise (Stereo mode)	ANOT	50	No signal	Measure the noise level (DIN AUDIO) at the LOUT (pin50).	
Cross talk (Stereo mode)	ACTT	51	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz,300mVrms	Measure the 1kHz component (V3:mVrms) at the ROUT (pin51) and calculate as follows: ACTT=20log(V3/300) [dB]	
Volume gain (Mono mode)	AVGM	50	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz,300mVrms	Measure the 1kHz component (V4:mVrms) at the LOUT (pin50) and calculate as follows: AVGM=20log(V4/300) [dB]	Audio SW=10 Mono Mode=1
Maximum output voltage (Mono mode)	AVOM	2	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz	When the distortion (DIN.AUDIO) of the LOUT(pin50) is 1%, Measure the voltage level at the EXT-LIN (PIN 2).	Audio SW=10 Mono Mode=1
Frequency characteristic (Mono mode)	AFREQM	2	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =300mVrms	Measure the voltage level (V5:mVrms) at the LOUT (pin50) and calculate as follows: AFM=20log(V5/300) [dB] When the AFM is –3dB, Measure the frequency at the EXT-LIN (PIN 2).	Audio SW=10 Mono Mode=1
Total harmonic distortion (Mono mode)	ATHDM	50	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz,300mVrms	Measure the distortion (DIN.AUDIO) of the 1kHz component at the LOUT (pin50).	Audio SW=10 Mono Mode=1
Output voltage noise (Mono mode)	ANOM	50	No signal	Measure the noise level (DIN AUDIO) at the LOUT (50PIN).	Mono Mode=1
Mute	AMUTE	50	EXT1-LIN(2PIN) EXT2-LIN(8PIN) =1kHz,300mVrms	Measure the 1kHz component (V8:mVrms) at the LOUT (PIN50) and calculate as follows: AMUTE =20log(V8/300) [dB]	Audio.mute =1
L/R Balance	ABT	51	EXT1-LIN(2PIN) EXT1-RIN(1PIN) EXT2-LIN(8PIN) EXT2-RIN(7PIN) =1KHz,300mVrms	Measure the 1KHz component(V9:mVrms) at the ROUT (PIN51) and calculate as follows: ABT=20Log(V1/V9) [dB]	

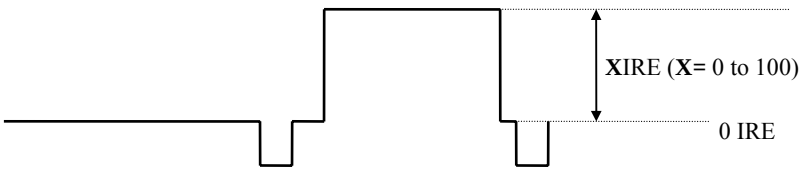
• Video Block Input Signals and Test Conditions

1, C IN Input*chroma burst signal: 40 IRE
2. Y IN input signal 100IRE:714mV
3, Bus control bit conditions: Initial test state

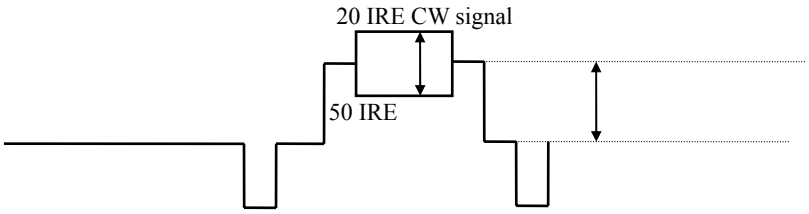
·10IRE signal (L-0): NTSC standard sync signal



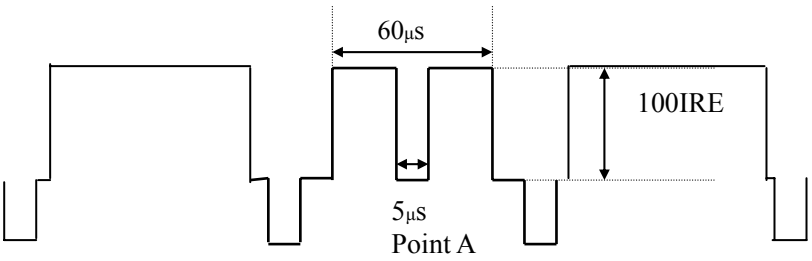
· XIRE signal (L-X)



· CW signal (L-CW)



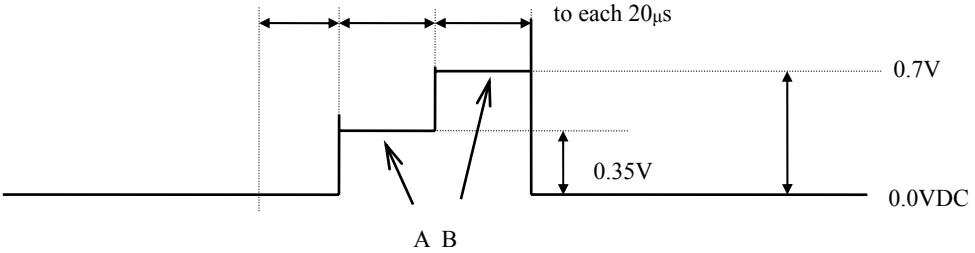
· BLACK STRETCH A point (0IRE to 99IRE) signal (L-BK)



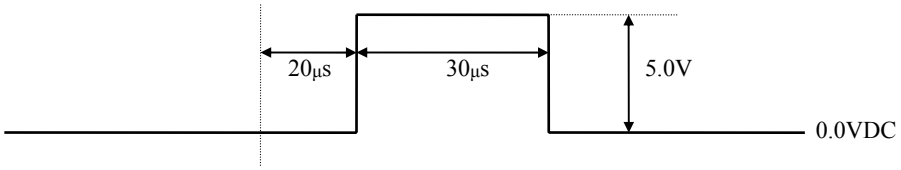
…100IRE white signal as other H …

· R/G/B IN Input signal

· RGB Input signal 1 (0-1)



· RGB Input signal 2 (0-2)



Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Video block]					
Video overall gain (Contrast max)	CONT127	46	L-50	Measure the output signal's 50IRE amplitude (CNTHB Vp-p) and calculate CONT127= 20log (CNTHB/0.357).	CONTRAST:1111111 Y Gamma Start=11
Contrast adjustment characteristics (normal/max)	CONT64	46	L-50	Measure the output signal's 50IRE amplitude (CNTCB Vp-p) and calculate CONT63= 20log (CNTCB/CNTHB).	CONTRAST:1000000 Y Gamma Start=11
Contrast adjustment characteristics (min/max)	CONT0	46	L-50	Measure the output signal's 50IRE amplitude (CNTLB Vp-p) and calculate CONT0=20log (CNTLB/CNTHB).	CONTRAST:0000000 Y Gamma Start=11
Video frequency Characteristics 1 (NTSC)	BW1	46	L-CW	With the input signal's continuous wave=100kHz, measure the output signal's continuous wave amplitude (PEAKDC Vpp). With the input signal's continuous wave=1.8MHz, measure the output signal's continuous wave amplitude (CW1.8 Vpp). Calculate BW1=20Log (CW1.8/PEAKDC).	Y Filter.sys:00 SHARPNESS: 001010 Y Gamma Start=11
Video frequency Characteristics 2 (PAL)	BW2	46	L-CW	With the input signal's continuous wave=2.2MHz, measure the output signal's continuous wave amplitude (CW2.2 Vp-p). Calculate BW2=20Log (CW2.2/PEAKDC).	Y Filter.sys:01 SHARPNESS: 001010 Y Gamma Start=11
Video frequency Characteristics 3 (6MHz TRAP)	BW3	46	L-CW	With the input signal's continuous wave=2.3MHz, measure the output signal's continuous wave amplitude (CW2.3 Vp-p). Calculate BW3=20Log (CW2.3/PEAKDC).	Y Filter.sys:10 SHARPNESS: 001010 Y Gamma Start=11
Video frequency Characteristics 4 (APF)	BW4	46	L-CW	With the input signal's continuous wave=3.4MHz, measure the output signal's continuous wave amplitude (CW3.4 Vp-p). Calculate BW3=20Log (CW3.4/PEAKDC).	Y Filter.sys:00 SHARPNESS: 001010 Y APF:1 Y Gamma Start=11
Chroma trap amount PAL	CtraPP	46	L-CW	With the input signal's continuous wave=4.43MHz, measure the output signal's continuous wave amplitude (F0P Vp-p). Calculate CtraP=20Log (F0P/PEAKDC).	Y Filter.sys:01 Sharpness: 000000 Y Gamma Start=11
Chroma trap amount NTSC	CtraPN	46	L-CW	With the input signal's continuous wave=3.58MHz, measure the output signal's continuous wave amplitude (F0N Vp-p). Calculate CtraN=20Log (F0N/PEAKDC).	Y Filter.sys:00 Sharpness: 000000 Y Gamma Start=11
DC restoration rate 1	ClampG1	46	L-0	Measure the output signal's 0IRE DC level (BRTPL V).	Sub.Bais:1111111 CONTRAST:0111111
			L-100	Measure the output signal's 0IRE DC level(DRVPH V) and 100IRE amplitude (DRVH Vp-p) and calculate ClampG=100×(1+(DRVPH-BRTPL)/DRVH).	Sub.Bais:1111111 Contrast:0111111 DCREST=00 BLK.STR.START=11 WPL=0
DC restoration rate 2	ClampG2	46	L-100	With DCREST = 01, carry out measurement similarly to the case of the DC restoration rate 1.	DCREST =01
DC restoration rate 3	ClampG3	46	L-100	With DCREST = 10, carry out measurement similarly to the case of the DC restoration rate 1.	DCREST =10
DC restoration rate 4	ClampG4	46	L-100	With DCREST = 11, carry out measurement similarly to the case of the DC restoration rate 1.	DCREST =11
Y-DL TIME1 (NTSC)	TdY1	46	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	Y Filter.sys:00 YDELAY Ajust:100
Y-DL TIME2 (PAL)	TdY2	46	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	Y Filter.sys:01 YDELAY Ajust:100
Y-DL TIME3	TdY3	46	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	Y Filter.sys:11 YDELAY Ajust:100 Delay Test:1
Y-DL TIME4 (6MHz TRAP)	TdY4	46	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	Y Filter.sys:10 YDELAY Ajust:100
Y-DL TIME Ajust1	TdYa1	46	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	Y Filter.sys:00 Y Delay Ajust:000

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Y-DL TIME Ajust2	TdYa2	46	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	Y Filter.sys:00 Y Delay Ajust:111
Black stretch gain (MAX)	BKST max	46	L-BK (A=0IRE)	Measure the 0IRE DC level(BKST1 V) at point A of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode	Blk.str.start=11 Y Filter.sys:10
				Measure the 0IRE DC level(BKST2 V) at point A of the output signal in the Black Stretch ON mode. Calculate BKST max=50□ (BKST1-BKST2)/CNTHB.	Blk.str.gain=10 Blk.str.start=01 Y Filter.sys:10
Black stretch gain (MID)	BKST mid	46	L-BK (A=0IRE)	With Blk.str.gain = 01, carry out the same measurement as for the case of black stretch gain (MAX).	Blk.str.gain=01 Blk.str.start=01 Y Filter.sys:10
Black stretch gain (MIN)	BKST min	46	L-BK (A=0IRE)	With Blk.str.gain = 00, carry out the same measurement as for the case of black stretch gain (max).	Blk.str.gain=00 Blk.str.start=01 Y Filter.sys:10
Black stretch start max (60IRE ΔBlack)	BKSTTH max	46	L-BK (A=60IRE)	Measure the 60IRE DC level(BKST3 V) at point A of the output signal in the Black Stretch ON mode.	Blk.str.gain=01 Blk.str.start=10 Y Filter.sys:10
				Measure the 60IRE DC level(BKST4 V) at point A of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode. Calculate BKSTTHmax=50□(BKST4-BKST3)/CNTHB.	Blk.str.gain=00 Blk.str.start=11 Y Filter.sys:10
Black stretch start mid (50IRE ΔBlack)	BKSTTH mid	46	L-BK (A=50IRE)	Measure the 50IRE DC level(BKST5 V) at point A of the output signal in the Black Stretch Defeat ON mode.	Blk.str.gain=01 Blk.str.start=01 Y Filter.sys:10
				Calculate BKSTTHmid=50□ BKST6-BKST5)/CNTHB.	Blk.str.gain=00 Blk.str.start=11 Y Filter.sys:10
Black stretch start min (40IRE ΔBlack)	BKSTTH min	46	L-BK (A=40IRE)	Measure the 40IRE DC level(BKST7 V) at point A of the output signal in the Black Stretch Defeat ON mode.	Blk.str.gain=01 Blk.str.start=00 Y Filter.sys:10
				Measure the 40IRE DC level(BKST8 V) at point A of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode. Calculate BKSTTHmin=50□(BKST8-BKST7)/CNTHB.	Blk.str.gain=00 Blk.str.start=11 Y Filter.sys:10
Sharpness variable range (NTSC)	Sharp32T1	46	L-CW	With the input signal's continuous wave=2.2MHz, measure the output signal's continuous wave amplitude (F01S32 Vp-p). Calculate Sharp32T1=20Log (F01S32/PEAKDC).	Y Filter.sys:00 Sharpness: 100000 Y Gamma Start=11 C_Kill.ON=1
(max)	Sharp63T1	46	L-CW	With the input signal's continuous wave=2.2MHz, measure the output signal's continuous wave amplitude (F01S63 Vpp). Calculate Sharp63T1=20Log (F01S63/PEAKDC).	Y Filter.sys:00 Sharpness: 111111 Y Gamma Start=11 C_Kill.ON=1
(min)	Sharp0T1	46	L-CW	With the input signal's continuous wave=2.2MHz, measure the output signal's continuous wave amplitude (F01S0 Vpp). Calculate Sharp0T1=20Log (F01S0/PEAKDC).	Y Filter.sys:00 Sharpness: 000000 Y Gamma Start=11 C_Kill.ON=1
Sharpness variable range (PAL)	Sharp32T2	46	L-CW	With the input signal's continuous wave=2.7MHz, measure the output signal's continuous wave amplitude (F02S32 Vpp). Calculate Sharp32T3=20Log (F02S32/PEAKDC).	Y Filter.sys:01 Sharpness: 100000 Y Gamma Start=11 C_Kill.ON=1
(max)	Sharp63T2	46	L-CW	With the input signal's continuous wave=2.7MHz, measure the output signal's continuous wave amplitude (F02S63 Vpp). Calculate harp63T2=20Log (F02S63/PEAKDC).	Y Filter.sys:01 Sharpness: 111111 Y Gamma Start=11 C_Kill.ON=1
(min)	Sharp0T2	46	L-CW	With the input signal's continuous wave=2.7MHz, measure the output signal's continuous wave amplitude (F02S0 Vpp). Calculate Sharp0T2=20Log (F02S0/PEAKDC).	Y Filter.sys:01 Sharpness: 000000 Y Gamma Start=11 C_Kill.ON=1

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Sharpness variable range (6MHz TRAP)	Sharp32T4	46	L-CW	With the input signal's continuous wave=3.0MHz, measure the output signal's continuous wave amplitude (F04S32 Vpp). Calculate Sharp32T4=20Log (F04S32/PEAKDC).	Y Filter.sys:10 Sharpness: 100000 Y Gamma Start=11 C_Kill.ON=1
(max)	Sharp63T4	46	L-CW	With the input signal's continuous wave=3.0MHz, measure the output signal's continuous wave amplitude (F04S63 Vpp). Calculate Sharp63T4=20Log (F04S63/PEAKDC).	Y Filter.sys:10 Sharpness: 111111 Y Gamma Start=11 C_Kill.ON=1
(min)	Sharp0T4	46	L-CW	With the input signal's continuous wave=3.0MHz, measure the output signal's continuous wave amplitude (F04S0 Vpp). Calculate Sharp0T4=20Log (F04S0/PEAKDC).	Y Filter.sys:10 Sharpness: 000000 Y Gamma Start=11 C_Kill.ON=1
White peak limiter operating point 1	WPL1	46	L-100	Measure the ampritude(from pedestal to white) of the output signal with WPL=00. (PIN 45: 5V) Bigger the input signal and measure the amplitude (from pedestal to white) of the output signal at which the output signal is clipped. (WP1) WPL1=WP1/CNTCB1*100	WPL=00 Y Gamma Start=11
White peak limiter operating point 2	WPL2	46	L-100	Bigger the input signal and measure the amplitude(from pedestal to white) of the output signal at which the output signal is clipped with WPL=01. (WP2) WPL2=WP2/CNTCB1*100	WPL=01 Y Gamma Start=11
White peak limiter operating point 3	WPL3	46	L-100	Bigger the input signal and measure the amplitude(from pedestal to white) of the output signal at which the output signal is clipped with WPL=10. (WP3) WPL3=WP3/CNTCB1*100	WPL=10 Y Gamma Start=11
White peak limiter operating point 4	WPL4	46	L-100	Bigger the input signal and measure the amplitude(from pedestal to white) of the output signal at which the output signal is clipped with WPL=11. (WP4) WPL4=WP4/CNTCB1*100	WPL=11 Y Gamma Start=11
Y gamma start effective point1	YGST1	46	L-100	Measure the amplitude of the output signal (0 to 100IRE) with Y GAMMA START=3.Y GAMMA GAIN=0. (GAM0)	Y Gamma GAIN=00 Y Gamma Start=11
			L-50	Next measure the amplitude the output signal (0 to 50IRE) with Y GAMMA START=1. Y GAMMA GAIN=1(GAM1) and calculate YGS1= GAM1/GAM0*100	Y Gamma GAIN=01 Y Gamma Start=00
Y gamma start effective point12	YGST2	46	L-50	Measure the amplitude of the output signal (0 to 50IRE) with Y GAMMA START=1. Y GAMMA GAIN=1 (GAM2) and calculate YGS2= GAM2/GAM0*100	Y Gamma GAIN=01 Y Gamma Start=01
Y gamma start effective point1	YGST3	46	L-50	Measure the amplitude of the output signal (0 to 50IRE) (GAM3) and calculate YGS3= GAM3/GAM0*100	Y Gamma GAIN=01 Y Gamma Start=10
Y gamma gain 1	YGGA1	46	L-50	Measure the amplitude of the output signal (0 to 50IRE).(GGAM1)	Y Gamma Start =01 Y Gamma GAIN=00
			L-100	Measure the amplitude of the output signal (0 to 100IRE).(GGAM2) Calculate YGG1=100*GGAM1/(GGAM2-GGAM1)	
Y gamma gain 2	YGGA2	46	L-50	Measure the amplitude of the output signal (0 to 50IRE).(GGAM3)	Y Gamma Start =01 Y Gamma GAIN=01
			L-100	Measure the amplitude of the output signal (0 to 100IRE).(GGAM4) Calculate YGG2=100*GGAM3/(GGAM4-GGAM3)	
Y gamma gain 3	YGGA3	46	L-50	Measure the amplitude of the output signal (0 to 50IRE) .(GGAM5)	Y Gamma Start =01 Y Gamma GAIN=10
			L-100	Measure the amplitude of the output signal (0 to 100IRE).(GGAM6) Calculate YGG3=100*GGAM5/(GGAM6-GGAM5)	
GRAY MODE LEVEL	GRAY	46		Measure the DC level(deviation from pedestal)of pin46, and transfer IRE.	CROSS B/W:10 GRAY MODE:1
Horizontal/vertical blanking output level	RGBBLK	46	L-100	Measure the DC level (RGBBLK V) for the output signal's blanking period.	
Pre-shoot adjust1	PreShoot1	46	L-100	Measure the pre-shoot width (Tpre) and over-shoot width (Tover) at rise of 100IRE amplitude of the output signal, and calculate PreShoot = Tpre / Tover.	Pre-shoot adj.=00 Y Filter.sys:00 Sharpness=111111
Pre-shoot adjust2	PreShoot2	46	L-100	With Pre-shoot adj. = 11, carry out the same measurement as for the case of Pre-Shoot 1.	Pre-shoot adj.=11 Y Filter.sys:00 Sharpness=111111

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Over-shoot adjust	OverShoot	46	L-100	With Over-shoot adj. = 11Measure the pre-shoot width (Tpre) and over-shoot width (Tover) at rise of 100IRE amplitude of the output signal, and calculate OverShoot = Tover/Tpre	Over-shoot adj.=11 Y Filter.sys:00 Sharpness=111111
[RGB output block] (Cutoff, drive block)				Bus control bit conditions: Contrast=127	Contrast:1111111
Brightness control (normal)	BRT64	48 47 46	L-0	Measure the 0IRE DC levels of the respective output signals of R output (48), G output (47), and B output (46). Assign the measured values to BRTPCR, BRTPCG, and BRTPCB V, respectively. Calculate BRT63=(BRTPCR+BRTPCG+BRTPCB)/3	Bright: 1000000
Brightness control (normal-H)	BRT64H	46	L-0	Measure the 0IRE DC level of the output signal of B output (46) and assign the measured value to BRTPCBH.	Bright: 1000000 B.BIAS: 11111111 Sub Bias: 1111111
Brightness control (max)	BRT127	46	L-0	Measure the 0IRE DC level of the output signal of B output (46) and assign the measured value to BRTPHB. Calculate BRT127=50×(BRTPHBH-BRTPCB)/CNTHB.	Bright: 1111111 B.BIAS: 11111111 Sub Bias: 1111111
Brightness control (min)	BRT0	46	L-0	Measure the 0IRE DC level of the output signal of B output (46) and assign the measured value to BRTPLB. Calculate BRT0=50□(BRTPLB-BRTPCBH)/CNTHB.	Bright: 0000000 B.BIAS: 11111111 Sub Bias: 1111111
Bias (cutoff) control (min)	Vbias0	48 47 46	L-50	Measure the 0IRE DC levels (Vbias0χV)of the respective output signals of R output (48), G output (47), and B output (46). (χ: R, G, and B)	Sub.Bias: 1111111
Bias (cutoff) control (max)	Vbias255	48 47 46	L-50	Measure the 0IRE DC levels (Vbias255χV)of the respective output signals of R output (48), G output (47), and B output (46). (χ: R, G, and B)	Sub.Bias: 1111111 R/G/B.BIAS:11111111
Bias (cutoff) control resolution	Vbiassns	48 47 46	L-50	Measure the 0IRE DC levels (BAS80χV) of the respective output signals of R output (48), G output (47), and B output (46). (χ: R, G, and B) Measure the 0IRE DC levels (BAS48χV)of the respective output signals of R output (48), G output (47), and B output (46). Calculate Vbiassnsχ= (BAS80χ-BAS48χ)/32	R/G/B.BIAS:01010000 Sub.Bias: 1111111 R/G/B.BIAS:00110000 Sub.Bias: 1111111
Sub-bias control resolution	Vsbiassns	48 47 46	L-50	Set Sub.Bias 64 and measure the 0IRE DC levels (SB64χV) of the respective output signals of R output (48),G output(47), and B output(46).and next,set Sub.Bias 42,then measure the same as before. Calculate Vsbiassnsχ-(SB64χ-SB42χ)/22	Sub.Bias: 1000000/0101010 Contrast: 0111111 R/G/B.BIAS:11111111
Drive adjustment maximum output	RGBout127	48 47 46	L-100	Measure the 100IRE amplitudes (DRVHχVp-p)of the respective output signals of R output (48),G output(47) and B output (46). (χ: R, G and B)	Bright: 0000000 R/G/B DRIVE: 1111111 Contrast: 1000000
Output attenuation	RGBout0	48 47 46	L-100	Measure the 100IRE amplitudes (DRVLχVp-p) of the respective output signals of R output (48), G output (47), and B output (46). (χ: R, G and B) Calculate RGBout0χ=20log(DRVHχ/DRVLχ)	Bright: 0000000 R/G/B DRIVE: 0000000 Contrast: 1000000

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[VIDEO SW [Block]					
Video signal input 1DC voltage	VIN1DC	5	L-100	Input signals to pin 5 and measure the voltage of the pedestal.	Video SW:01
Video signal input 1 AC voltage	VIN1AC	5		Pin 5 recommended input level	Video SW:01
Video signal input 2DC voltage	VIN2DC	3	L-100	Input signals to pin 3 and measure the voltage of the pedestal.	Video SW:00
Video signal input 2 AC voltage	VIN2AC	3		Pin 3 recommended input level	Video SW:00
Video signal input 3DC voltage	VIN3DC	10		Input signals to pin 10 and measure the voltage of the pedestal.	Video SW:10
Video signal input 3AC voltage	VIN3AC	10		Pin 10 recommended input level	Video SW:10
Video signal input 4DC voltage	VIN4DC	7		Input signals to pin 7 and measure the voltage of the pedestal.	Video SW:11
Video signal input 4AC voltage	VIN4AC	7		Pin 7 recommended input level	Video SW:11
SVO terminal DC voltage	SVODC	61	L-100	Input signals to pin 5 and measure the voltage of the pedestal at pin 61.	Video SW:01 SVO SW:1 YCMIX:0
SVO terminal AC voltage	SVOAC	61	L-100	The signal is input to 5PIN, and the amplitude of the signal of 61PIN is measured.	VIDE0 SW:01 SVO SW:1 YCMIX:0
SVO terminal Ycmix AC Voltage	SVOYC	61	L-0 L-CW	Y signal is input to 7PIN, and C signal of 8PIN is input, and the amplitude of 61PIN (SVO) is measured.	VIDE0 SW:11 SVO SW:1 YCMIX:1

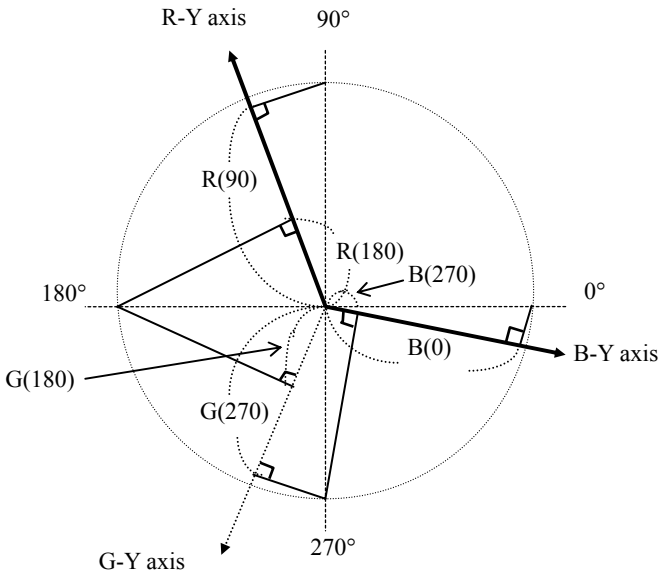
•Chroma Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. VIF, SIF blocks: No signal
2. Deflection Block: Horizontal/vertical composite sync signals are input and the deflection block must be locked into the sync signals (Refer to the Deflection Block Input Signals and the Test Conditions).
3. Bus control conditions: Set the following conditions unless otherwise specified.
   Y Input is 7 Pin (YC-Y),
   C Input is 8 Pin (YC-C)
   (Video SW=3, C. Ext=1)
   Other DAC except the above-mentioned conditions is all initial conditions.
4. Y Input condition: No signal unless otherwise specified.
   (Sync is necessary to obtain synchronization).
5. How to calculate the demodulation ratio and angle:

B-Y axis angle=tan-1(B (0) / B (270))+270°
R-Y axis angle=tan-1(R (180) / R (90))+90°
G-Y axis angle=tan-1(G (270) / G (180))+180°

B-Y axis amplitude Vb=SQRT(B(0)*B(0)+B(270)*B(270))
R-Y axis amplitude Vr=SQRT(R(180)*R(180)+R(90)*R(90))
G-Y axis amplitude Vg=SQRT(G(180)*G(180)+G(270)*G(270))



6. Chroma input signal

As for the PAL signal, the burst swings such as 135° and 225° every horizontal period.
Chroma describes the phase caused when the burst occurs at 135°.
As for the NTSC signal, the burst occurs constantly at 180°.

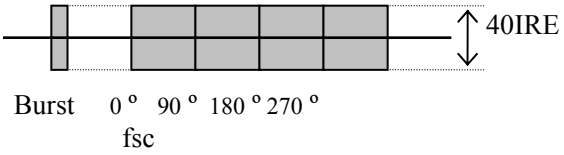
The figures below are based on the phase of NTSC. When a PAL signal is generated, adjust the phase and then enter signals.

The item common to both PAL and NTSC is the PAL signal. For those other than this, the measurement must be performed for each individual signals.

The condition of fsc: Set the following conditions unless otherwise specified.

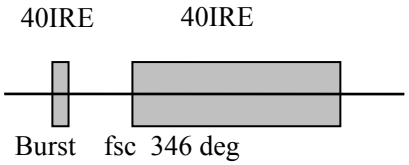
PAL =4.433619MHz
NTSC =3.579545MHz

C-1

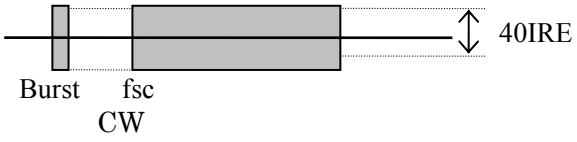


X IRE signal (L-X)

C-2

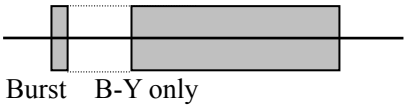


C-3

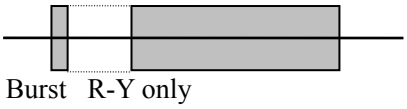


(Note: fsc±N*fh when the frequency is specified.
N should be a natural number and the nearest value should be used.)

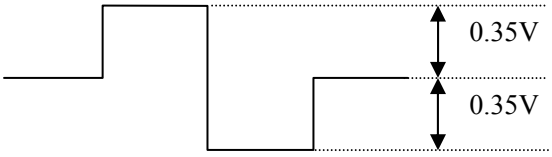
C-4



C-5



C-6



*There is no signal for H, V blanking period.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Chroma block]: PAL/NTSC common					
B-Y/Y amplitude ratio	CLRBY	46	YIN:L_{77} CIN: No signal	Measure the Y system's output level. V_1	
			C-2	Input a signal to the C_{IN} (only sync Signal to the YIN) and measure the output level to calculate as follows: CLRBY=100×(V2/V1)	Color:1000000
Color control Characteristics 1	CLRMN	46	C-1	Measure the output amplitude V_1 at color Control MAX mode and output amplitude V2 at color control CEN mode and, Calculate as follows: CLRMN=V_1/V_2	Color:1111111 Color:1000000
Color control Characteristics 2	CLRMM	46	C-1	Measure the output amplitude V_3 at color Control MIN mode to calculate as follows: CLRMM=20log (V_1/V_3)	Color:0000000
Color control sensitivity	CLRSE	46	C-1	Measure the output amplitude V4 at color Control 90 mode and output amplitude V5 at color control 38 mode to calculate as follows: CLRSE=100×(V_4− V_5)/(V_2×52)	Color:1011010 Color:0100110
Residual higher harmonic level B	E_CAR_B	46	C-1 Burst only	Measure the 8.86MHz component output amplitude at pin 46.	
Residual higher harmonic level G	E_CAR_G	47	C-1 Burst only	Measure the 8.86MHz component output amplitude at pin 47.	
Residual higher harmonic level R	E_CAR_R	48	Burst only	Measure the 8.86MHz component output amplitude at pin 48.	
[Chroma block]: PAL					
ACC amplitude characteristics 1	ACCM1_P	46	C-1 0dB +6dB	Measure the output amplitude when 0dB is applied to the chroma inputand when +6dB is applied to the chroma input. And calculate the ratio between them. ACCM1_P=20log(+6dBdata/0dBdata)	Color:1000000
ACC amplitude characteristics 2	ACCM2_P	46	C-1 -20dB	Measure the output amplitude when –20dB is applied to the chroma input and calculate the ratio between them. ACCM2_P=20log(-20dBdata/0dBdata)	Color:1000000
Demodulation output ratio R-Y/B-Y:PAL	RB_P	46 48	C-1	Refer to 5. and measure Bout output amplitude Vb and R_{OUT} output amplitude Vr. And calculate RB_P=Vr/Vb.	Color:1000000
Demodulation output ratio G-Y/B-Y:PAL	GB_P	46 47	C-4	Measure Bout output amplitude Vbp and G_{OUT} output amplitude Vgbp. And calculate GB_P=Vgbp/Vbp.	Color:1000000
Demodulation output ratio G-Y/R-Y:PAL	GR_P	47 48	C-5	Measure R_{OUT} output amplitude Vrp and G_{OUT} output amplitude Vgbp. And calculate GR_P=Vgrp/Vrp.	Color:1000000
Demodulation angle R-Y/B-Y:PAL	ANGRB_P	46 48	C-1	Refer to 5. and measure the B-Y and R-Y demodulation angle and calculate.	Color:1000000
Killer operating point 0 (PAL)	KILLP0	46	C-1	Reduce the input signal until the output Level becomes 75mVp-p or less. Measure the input level at that moment.	Color Killer Ope.:00
Killer operating point 3 (PAL)	KILLP3	46	C-1	Reduce the input signal until the output Level becomes 75mVp-p or less. Measure the input level at that moment.	Color Killer Ope.:11
Difference between two Killer operating points (PAL)	DKILLP			Calculate as follows, DKILLP=KILLP0-KILLP3	
APC pull-in range(+)	PULIN+_P	46	C-1	Decrease the chroma fsc frequency from 4.433619MHz+1000Hz and measure the frequency at which the V_{CO} locks.	
APC pull-in range(-)	PULIN-_P	46	C-1	Increase the chroma fsc frequency from 4.433619MHz-1000Hz and measure the frequency at which the V_{CO} locks.	

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Chroma block]: NTSC					
ACC amplitude characteristics 1	ACCM1_N	46	C-1 0dB +6dB	Measure the output amplitude when 0dB is applied to the chroma input and when +6dB is applied to the chroma input. And calculate the ratio between them. ACCM1_N=20log(+6dBdata/0dBdata)	
ACC amplitude characteristics 2	ACCM2_N	46	C-1 -20dB	Measure the output amplitude when 20dB is applied to the chroma input and calculate the ratio between them. ACCM2_N=20log(-20dBdata/0dBdata)	
Demodulation output ratio R-Y/B-Y:NTSC	RB_N	46 48	C-1	Refer to 5. And measure Bout output amplitude Vb and ROUT output amplitude Vr. And calculate RB_N=Vr/Vb.	Color:1000000
Demodulation output ratio G-Y/B-Y:NTSC	GB_N	47	C-1	Refer to 5. and measure G_{OUT} output amplitude Vg. And calculate GB_N=Vg/Vb.	Color:1000000
Demodulation angle B-Y/R-Y: NTSC	ANGBR_N	46 48	C-1	Refer to 5. and measure the B-Y and R-Y demodulation angle and calculate. Reference: B-Y angle	Color:1000000
Demodulation angle G-Y/B-Y: NTSC	ANGGB_N	46 47	C-1	Refer to 5. and measure the B-Y and G-Y demodulation angle and calculate. Reference: B-Y angle	Color:1000000
Killer operating point 0 (NTSC)	KILLN0	46	C-1	Reduce the input signal until the output Level becomes 75mVp-p or less. Measure the input level at that moment.	Color Killer Ope.:00
Killer operating point 3 (NTSC)	KILLN3	46	C-1	Reduce the input signal until the output Level becomes 75mVp-p or less. Measure the input level at that moment.	Color Killer Ope.:11
Difference between two Killer operating points (NTSC)	DKILLN			Calculate as follows, DKILLN=KILLN0-KILLN3	
APC pull-in range(+)	PULIN+_N	46	C-1	Decrease the chroma fsc frequency from 3.579545MHz+1000Hz and measure the frequency at which the V_{CO} locks.	
APC pull-in range(-)	PULIN-_N	46	C-1	Increase the chroma fsc frequency from 3.579545MHz-1000Hz and measure the frequency at which the V_{CO} locks.	
Tint center	TINCEN	46	C-1	Measure each part of the output level and calculate the B-Y axis angle.	TINT:1000000
Tint variable range (+)	TINT+	46	C-1	Measure each part of the output level and calculate the B-Y axis angle. TINT+ =B-Y axis angle –TINCEN	TINT:1111111
Tint variable range (-)	TINT-	46	C-1	Measure each part of the output level and calculate the B-Y axis angle. TINT- =B-Y axis angle –TINCEN	TINT:0000000
Cr output Amplitude	CBCR-R	48	R-Y IN:C-6	Measure the output amplitude. (B-Y IN:no signal)	CbCr IN: 1 Color Sys:101 Cross B/W: 01
Cb output Amplitude	CBCR-B	46	B-Y IN:C-6	Measure the output amplitude. (R-Y IN:no signal)	CbCr IN: 1 Color Sys: 101 Cross B/W: 01
[Filter Block]:Chroma BPF Characteristic					
C-BPF1A Peaker amplitude characteristic 3.93MHz	CBPF1A	46	C-3 PAL signal	Set the chroma frequency (CW) to 4.433619MHz-100kHz and measure V_0 output amplitude. And then, set the chroma frequency (CW) to 3.93MHz and measure V_1 output amplitude to calculate as follows: CBPF1A=20log(V_1/V_0)	C.Filter.Sys:10 C.BYPASS:0
C-BPF1B Peaker amplitude characteristic 4.73/4.13MHz	CBPF1B	46	C-3 PAL signal	Measure V_2 output amplitude when the chroma frequency (CW) is 4.13MHz and V_3 output amplitude when it (CW) is 4.73MHz to calculate as follows: CBPF1B =20log(V_3/V_2)	C.Filter.Sys:10 C.BYPASS:0
C-BPF1C Peaker amplitude characteristic 4.93/3.93MHz	CBPF1C	46	C-3 PAL signal	Set the chroma frequency (CW) to 4.93MHz and measure V_4 output amplitude to calculate as follows: CBPF1C =20log(V_4/V_1)	C.Filter.Sys:10 C.BYPASS:0
C-BPF2A BandPass amplitude characteristic 3.93MHz	CBPF2A	46	C-3 PAL signal	Set the chroma frequency (CW) to 4.433619MHz-100MHz and measure V_{00} output amplitude. And then, set the chroma frequency (CW) to 3.93MHz and measure V_{10} output amplitude to calculate as follows: CBPF2A=20log(V_{10}/V_{00})	C.Filter.Sys:11 C.BYPASS:0
C-BPF2B BandPass amplitude characteristic 4.73/4.13MHz	CBPF2B	46	C-3 PAL signal	Measure V_{20} output amplitude when the chroma frequency (CW) is 4.13MHz and V_{30} output amplitude when it (CW) is 4.73MHz to calculate as follows: CBPF2B =20log(V_{30}/V_{20})	C.Filter.Sys:11 C.BYPASS:0
C-BPF2C BandPass amplitude characteristic 4.93/3.93MHz	CBPF2C	46	C-3 PAL signal	Set the chroma frequency (CW) to 4.93MHz and measure V_{40} output amplitude to calculate as follows: CBPF2C =20log(V_{40}/V_{10})	C.Filter.Sys:11 C.BYPASS:0

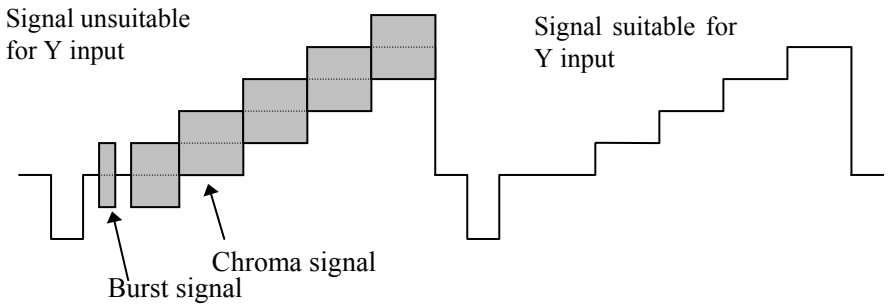
•Deflection Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

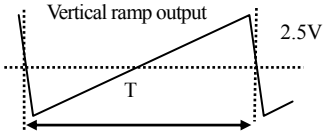
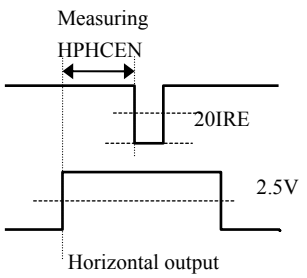
1. VIF, SIF blocks: No signal
2. C input: No. signal
3. Sync input: A horizontal/vertical composite sync signal

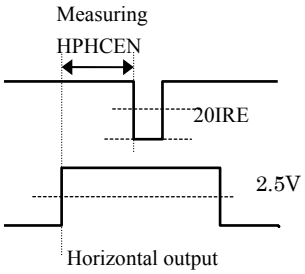
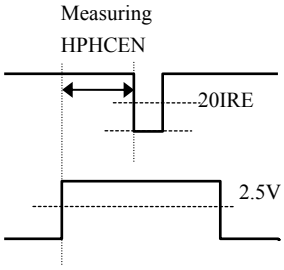
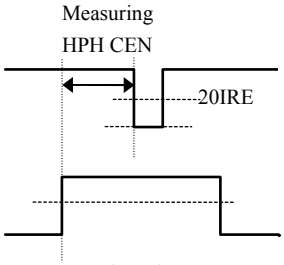
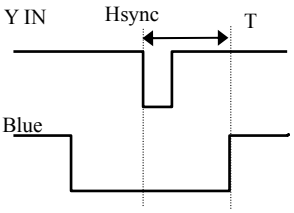
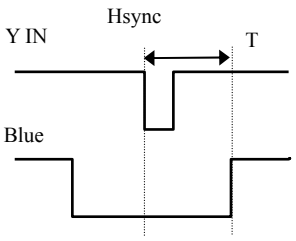
PAL: 43IRE, horizontal sync signal (15.625kHz) and vertical sync signal (50kHz)
NTSC: 40IRE, horizontal sync signal (15.734264kHz) and vertical sync signal (59.94kHz)

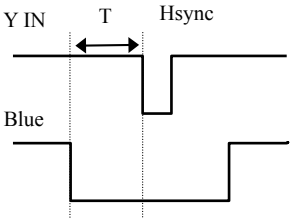
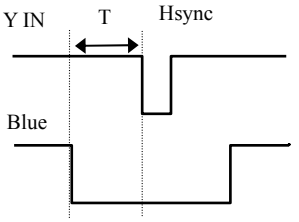
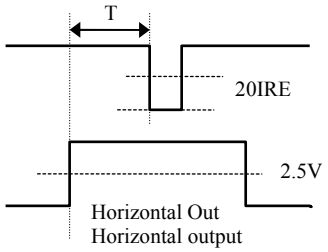
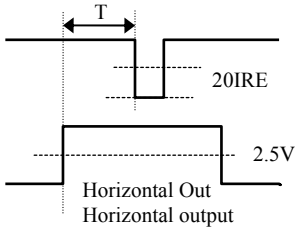
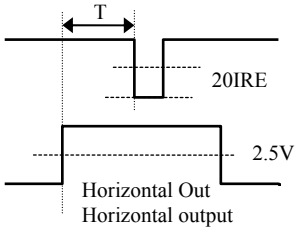
Note: No burst signal, chroma signal shall exist below the pedestal level.

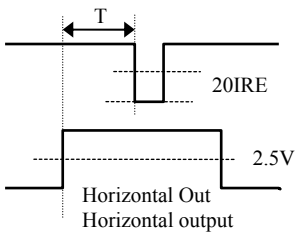
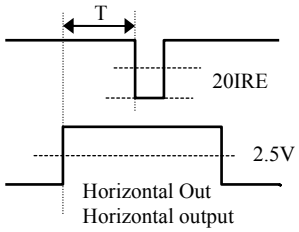
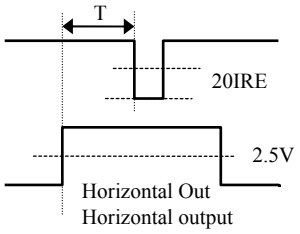
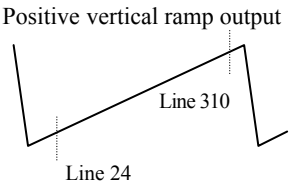
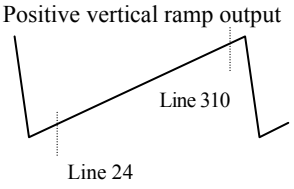
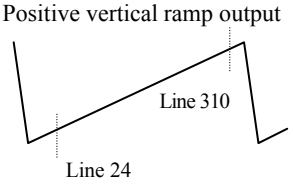


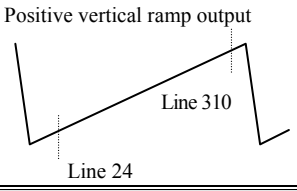
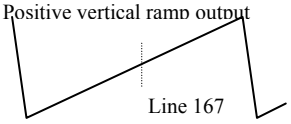
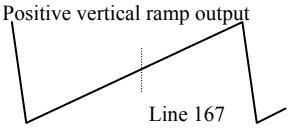
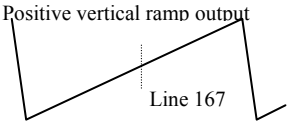
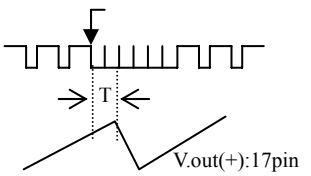
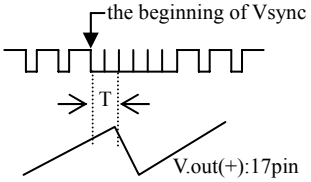
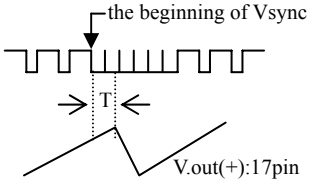
4. Bus control conditions: Initial conditions unless otherwise specified.
5. The delay time from the rise of the horizontal output (pin 22 output) to the fall of the FBP IN (pin 23 input) is 7μs.
6. Pin 15 (vertical size correction circuit input terminal) is connected to V_{CC} (5.0V).

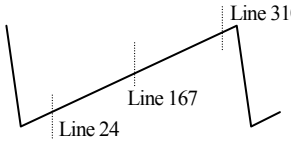
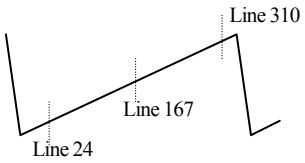
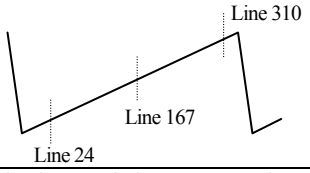
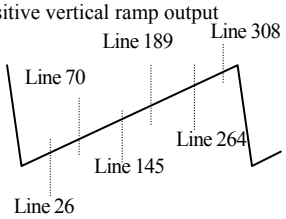
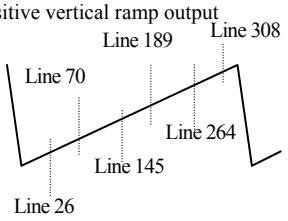
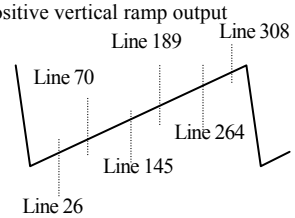
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Deflection block]					
Horizontal free-running frequency	fH	22	YIN: No signal	Connect a frequency counter to the output of pin 22 (H out) and measure the horizontal free-running frequency.	
Horizontal pull-in range	fH PULL	22 5	YIN: Horizontal /vertical sync signal PAL	Using an oscilloscope, monitor the horizontal sync signal which is input to the Y IN (pin 5) and the pin 22 output (H out) and vary the horizontal signal frequency to measure the pull-in range.	
Horizontal output pulse length	Hduty	22	YIN: Horizontal /vertical sync signal PAL	Measure the voltage for the pin 22 horizontal output pulse's low-level period.	
Horizontal output pulse saturation voltage	V Hsat	22	YIN: Horizontal /vertical sync signal PAL	Measure the voltage for the pin 22 horizontal output pulse's low-level period.	
Vertical free-running period 50(PAL) Vertical free-running period 60(NTSC)	VFR50 VFR60	17	YIN: No signal	Measure the vertical output period T at pin 17. T × 15.625kHz (PAL) T × 15.734kHz (NTSC) 	CDMODE:001 (PAL) CDMODE:010 (NTSC)
Horizontal output pulse (PAL)(NTSC)	HPHCEN (PAL) (NTSC)	22 5	Y IN: Horizontal /vertical sync signal PAL NTSC	Measure the delay time from to the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal. 	

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal position adjustment range	HPHrange	22 5	Y IN: Horizontal /vertical sync signal PAL	With H.PHASE: 0 and 31, measure the delay time from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the difference from H PHCEN. 	H.PHASE:00000 to H.PHASE:11111
Horizontal position adjustment maximum variable width	HPHstep	22 5	Y IN: Horizontal /vertical sync signal PAL	With H.PHASE: 0 to 31 varied, measure the delay time from to the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the variation at each step. Retrieve data for maximum variation. 	H.PHASE:00000 to H.PHASE:11111
Horizontal position adjustment maximum variable width	HPHstep	22 5	Y IN: Horizontal /vertical sync signal PAL	With H.PHASE: 0 to 31 varied, measure the delay time from to the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the variation at each step. Retrieve data for maximum variation. 	H.PHASE:00000 to H.PHASE:11111
Horizontal blanking left variable range@0	BLKL0	46 5	Y IN: Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 5 Y IN to the right end of blanking period at pin 46 BlueOUT with H.BLK.L = 000. 	H.BLK.L:000
Horizontal blanking left variable range@7	BLKL7	46 5	Y IN: Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 5 Y IN to the right end of blanking period at pin 46 BlueOUT with H.BLK.L = 111. 	H.BLK.L:111

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal blanking right variable range@0	BLKR0	46 5	Y IN: Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 5 Y IN to the left end of blanking period at pin 46 BlueOUT with H.BLK.R = 000. 	H.BLK.R:000
Horizontal blanking right variable range@7	BLKR7	46 5	Y IN: Horizontal /vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 5 Y IN to the left end of blanking period at pin 46 BlueOUT with H.BLK.R = 111. 	H.BLK.R:111
Horizontal output stop voltage	Hstop	20 22	Y IN: Horizontal /vertical sync signal	Decrease the current from a source connected to pin 20 and measure the pin 20 voltage at which HOUT(PIN22) stops.	
H Phase BOW@16	HBOW16	22 5	Y IN: Horizontal /vertical sync signal	Measure the delay time T from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal with line 24(NTSC:22) and 167(NTSC:142). Caluculat as follow with each value of T is as T1 and T2. HBOW16=T2-T1 	
H Phase BOW@0	HBOW0	22 5	Y IN: Horizontal /vertical sync signal	Measure the delay time T from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal with line 24(NTSC:22) and 167(NTSC:142). Caluculat as follow with each value of T is as T1 and T2. HBOW0=T2-T1 	H Phase Bow: 00000
H Phase BOW@31	HBOW31	22 5	Y IN: Horizontal /vertical sync signal	Measure the delay time T from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal with line 24(NTSC:22) and 167(NTSC:142). Caluculat as follow with each value of T is as T1 and T2. HBOW31=T2-T1 	H Phase Bow: 11111

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
H Phase ANGLE@16	HANG16	22 5	Y IN: Horizontal /vertical sync signal	Measure the delay time T from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal with line 24(NTSC:22) and 167(NTSC:142).Caluculat as follow with each value of T is as T1 and T2. HANG16=T2-T1  	
H Phase ANGLE@0	HANG0	22 5	Y IN: Horizontal /vertical sync signal	Measure the delay time T from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal with line 24(NTSC:22) and 167(NTSC:142).Caluculat as follow with each value of T is as T1 and T2. HANG0=T2-T1  	H Phase Angle: 00000
H Phase ANGLE@31	HANG31	22 5	Y IN: Horizontal /vertical sync signal	Measure the delay time T from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal with line 24(NTSC:22) and 167(NTSC:142). Caluculat as follow with each value of T is as T1 and T2. HANG31=T2-T1  	H Phase Angle: 11111
<Vertical screen size correction>					
vertical ramp output amplitude @64	Vsize64	17	Y IN: Horizontal /vertical sync signal PAL NTSC	Monitor the pin 17 vertical ramp output and measure the voltage at line 24 (22:NTSC) and line 310 (262:NTSC). Calculate as follows:Vsize64=Vline310(262:NTSC)-Vline24(22:NTSC)  	
vertical ramp output amplitude @0	Vsize0	17	Y IN: Horizontal /vertical sync signal PAL NTSC	Monitor the pin 17 vertical ramp output and measure the voltage at line 24 (22:NTSC) and line 310 (262:NTSC). Calculate as follows: Vsize0=Vline310(262:NTSC)-Vline24(22:NTSC)  	VSIZE: 0000000
vertical ramp output amplitude @127	Vsize127	17	Y IN: Horizontal /vertical sync signal PAL NTSC	Monitor the pin 17 vertical ramp output and measure the voltage at line 24 (22: NTSC) and line 310 (262:NTSC). Calculate as follows: Vsize127=Vline310(262:NTSC)-Vline24(22:NTSC)  	VSIZE: 1111111

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
<High-voltage dependent vertical size correction>					
Vertical size correction @0	Vsizecomp	17	Y IN: Horizontal /vertical sync signal PAL	Monitor the pin 17 vertical ramp output and measure the voltage at the line 24 and line 310 with VCOMP = 000. Calculate as follows: Va=Vline310-Vline24 Apply 4.0V to pin 15 and measure the voltage at the line 24 and line 310 again. Calculate as follows: Va=Vline310-Vline24 Calculate as follows: Vsizecomp=Vb/Va 	VCOMP:000 FSCorEHT=1
<Vertical screen position adjustment>					
Vertical ramp DC voltage @32	Vdc32	17	Y IN: Horizontal /vertical sync signal PAL NTSC	Monitor the pin 17 vertical ramp output and measure the voltage at line 167(142: NTSC). 	
Vertical ramp DC voltage @0	Vdc0	17	Y IN: Horizontal /vertical sync signal PAL NTSC	Monitor the pin 17 vertical ramp output and measure the voltage at line 167(142: NTSC). 	VDC:000000
Vertical ramp DC voltage @63	Vdc63	17	Y IN: Horizontal /vertical sync signal PAL NTSC	Monitor the pin 17 vertical ramp output and measure the voltage at line 167(142: NTSC). 	VDC:111111
Verticalposition @8	Vshift8	17 5	Y IN: Horizontal /vertical sync signal	Measure the time T from the beginning of Vsync at pin 5 Y IN to the fall of the pin 17. 	V.SHIFT:1000
Vertical position @0	Vshift0	17 5	Y IN: Horizontal /vertical sync signal	Measure the time T from the beginning of Vsync at pin 5 Y IN to the fall of the pin 17. 	V.SHIFT:0000
Vertical position @15	Vshift15	17 5	Y IN: Horizontal /vertical sync signal	Measure the time T from the beginning of Vsync at pin 5 Y IN to the Rise of the pin 17. 	V.SHIFT:1111

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical linearity@16	Vlin16	17	Y IN: Horizontal /vertical sync signal PAL	Monitor the pin 17 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin16=(Vb-Va)/(Vc-Vb) Positive vertical ramp output 	
Vertical linearity@0	Vlin0	17	Y IN: Horizontal /vertical sync signal PAL	Monitor the pin 17 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin0=(Vb-Va)/(Vc-Vb) Positive vertical ramp output 	VLIN:00000
Vertical linearity@31	Vlin31	17	Y IN: Horizontal /vertical sync signal PAL	Monitor the pin 17 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin31=(Vb-Va)/(Vc-Vb) Positive vertical ramp output 	VLIN:11111
Vertical S-shaped correction @16	Vscor16	17	Y IN: Horizontal /vertical sync signal PA L	Monitor the pin 17 vertical ramp output and measure the voltage at line 26, line 70, line 145, line 189, line 264 and 308. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows: Vscor16=0.5((Vb-Va)+(Vf-Ve))/ (Vd-Vc) Positive vertical ramp output 	
Vertical S-shaped correction @0	Vscor0	17	Y IN: Horizontal /vertical sync signal PAL	Monitor the pin 17 vertical ramp output and measure the voltage at line 26, line 70, line 145, line 189, line 264 and 308. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows: Vscor0=0.5((Vb-Va)+(Vf-Ve))/ (Vd-Vc) Positive vertical ramp output 	VSC:10000
Vertical S-shaped correction @31	Vscor31	17	Y IN: Horizontal /vertical sync signal PAL	Monitor the pin 17 vertical ramp output and measure the voltage at line 26, line 70, line 145, line 189, line 284 and 308. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows: Vscor31=0.5((Vb-Va)+(Vf-Ve))/ (Vd-Vc) Positive vertical ramp output 	VSC:11111

μ-Controller Chip (LC87F3664A)

Internal 64K-byte FROM (ROM/CGROM), 640-byte RAM And 352x9-bit CRT Display RAM 8-bit Single-chip Microcontroller.

1. Features

■Flash ROM

64K bytes

- 48K-byte program ROM
- 16K-byte character generator ROM
- Runs on a 5V single source and permits onboard programming.
- Block erasable in 128 byte units.
- Permits 100 programming operations.

■Internal RAM

- General-purpose RAM: 640 bytes
- CRT display RAM: 352 × 9 bits
- ROM correction RAM: 128 bytes

■Minimum bus cycle time

- 77 ns (13.0 MHz)

Note: The bus cycle time here refers to the ROM read speed.

■Minimum instruction cycle time

- 231 ns (13.0MHz)

■OSD

- Screen display: 36 characters × 8 lines
- Display RAM : 352 words (1 word=9 bits)

Display area: 36 words × 8 lines

Control area: 8 words × 8 lines

- Font types: 16×32 font, 256 types (including 5 fixed fonts)

An arbitrary number of characters can be generated as 16×17 or 8×9 font characters.

- Display colors: 512 colors (Analog output)

Character text, background, borders, and full background can be displayed.

A maximum 16 colors displayable on a line.

- Display mode specifiable on a line basis.

OSD mode1, OSD mode 2(Quarter size), OSD mode 3(Simplified graphic), caption/text mode

- Vertical display start line and horizontal display start position specifiable on a line basis.
- Shutter function (specifying the display start or stop line) and scroll functions specifiable on a line basis.
- Horizontal character spacing (9 to 16 dots) (*6) and vertical character spacing (1 to 32 dots) specifiable on a line basis.
- Character size selectable from 10 character sizes on a line basis. (*6)

(Horizontal×Vertical) = (1×1), (1×2), (2×2), (2×4), (1.5×1), (1.5×2), (3×2), (3×4), (0.5×0.5), (0.75×0.5)

- Simplified graphic display (One character (16×16 font) can be painted in 4 or 8 colors.)
- The half tone control of the TV picture in the background of the character is possible.
- Built-in the oscillation circuit for display

(*6)The supported range varies depending on the active display mode. Refer to the user's guide for details.

■Data slicer function(closed caption format)

- Extracts closed caption data and XDS data.
- NTSC/PAL selectable and line specifiable.

■Ports

- Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1 bit units: 10 (P1n, P3n)

Ports whose I/O direction can be designated in 4 bit units: 8 (P0n)

*If X'tal oscillator is to be used for time-of-day clock, the number of available Port 0 is 6.

Note: Threee of the available ports are internally connected to the companion signal processing IC.

■Timers

- Timer 0: 16-bit timer/counter with a capture register.
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
- Base timer

■SIO

- SIO0: 8-bit synchronous serial interface
- SIO1: 8-bit asynchronous/synchronous serial interface (bus mode 1 system)

Input and output is possible from the terminal of two systems in bus mode.

The two data lines and clock lines can be connected.

■AD converter: 6 bits ×5 channels

Note: One channel is connected internally to the signal processing IC.

■PWM: 14-bit PWM×1 channel

■Digital AFT
- It supports 38MHz , 38.9MHz , 39.5MHz and 45.75MHz as the IF frequencies.

■Remote controller receiver circuit (sharing with P03 and INT3 pins)
- Noise rejection function (noise filter time constant selectable from 1 Tcyc,32 Tcyc,and 128Tcyc)

■Watchdog timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■High-speed multiplication/division instructions
- 16 bits×8 bits (Execution time: 5 Tcyc)
- 24 bits×16 bits (Execution time: 12 Tcyc)
- 16 bits÷8 bits (Execution time: 8 Tcyc)
- 24 bits÷16 bits (Execution time: 12 Tcyc)

■Interrupts
- 15 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1/data slicer
9	00043H	H or L	vertical sync (VS#)/scan line
10	0004BH	H or L	Port 0

- Priority levels X > H > L
- If interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine stack levels: 320 levels maximum (the stack is allocated in RAM.)

■Oscillation circuits
- RC oscillation circuit (internal): For system clock
- VCO oscillation circuit (internal): For system clock generation and CRT display
- Crystal oscillation circuit: For base timer

Note:When the base timer count of clock accuracy is necessary , use the port terminal (two ports) as the crystal oscillation. (See the [12 μ-Controller Chip Crystal Oscillation Circuit and Sample Characteristics] for details.)

■Standby function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.

1) Oscillation is not halted automatically.
2) There are three ways of resetting HALT mode.
(1) Setting the reset pin to lower level.
(2) Generation of reset with the watchdog timer.
(3) Setting at least one of the INT0 and INT1 pins to the specified level.

- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.

1) The VCO and RC oscillators automatically stop operation.
2) There are four ways of resetting the HOLD mode.
(1) Setting the reset pin to the lower level.
(2) Generation of reset with the watchdog timer.
(3) Setting at least one of the INT0 and INT1 pins to the specified level.
(4) Having an interrupt source established at port 0.

■ROM correction function
- Executes the correction program on detection of a match with the program counter value.
- Correction program area size: 128 bytes (4 vector addresses)

■Development tools
- Emulater: TCB87 (Type B or Typ C) (onchip debugger interface board)
+ ECB873600A (evaluation chip board + LC873600EVA)
+ POD36-JCT (connecter between evaluation chip board and POD)
+ POD76600 (POD + LV766xxEVA)

■Flash Programming Board : W76200D

When using the Flash Programming Board, all of the jumper SW must be set to the OFF position.
If set to the ON position, read/write operations will not perform correctly.

Pin 1 of the conversion board should be located as indicated below.
When viewing from the edge closest to jumper SW, pin 1 is located on the lower right of both the chip and conversion board.

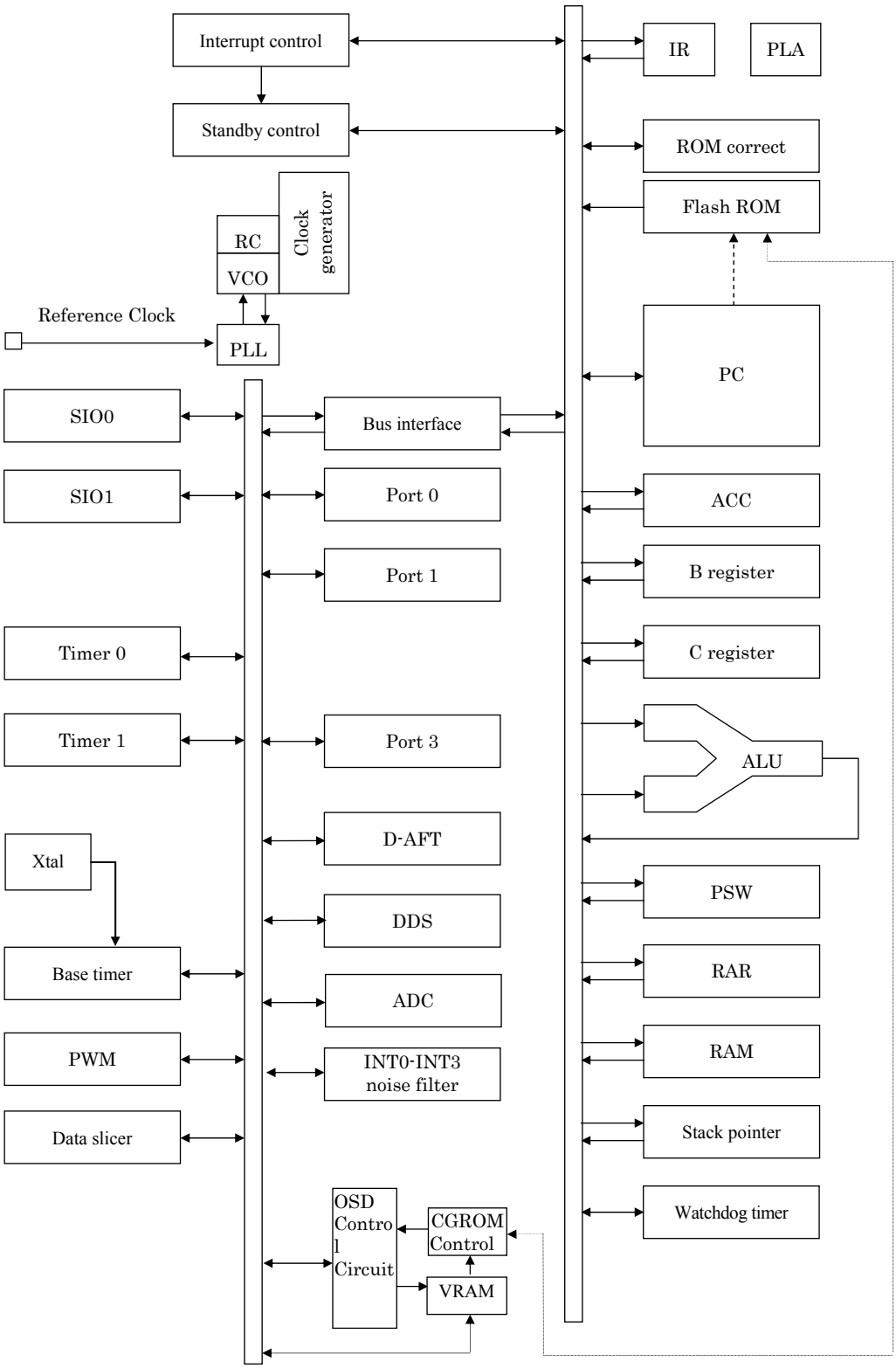
W76200D

■Flash ROM Programmer

Maker	Model	Support Version (Note)	Device
Flash Support Group,Inc. (Single)	AF9708/AF9709/AF9709B (including models manufactured by Ando Electric Co.,Ltd)	Rev02.72	LC87F3264A (3B231)
Flash Support Group,Inc. (Gang)	AF9723(main unit) (including models manufactured by Ando Electric Co.,Ltd)	(*7)	LC87F3264A
	AF9833(unit) (including models manufactured by Ando Electric Co.,Ltd)	(*7)	
SANYO	SKK/SKK TypeB	Application Version 1.04 Chip Data Version 2.21	LC87F3664

Note: Check for the latest version.
The LC87F3664A does not support a silicon signature feature.
(*7) We have a schedule to request the registration

2. μ-Controller Chip System Block Diagram



3. μ-Controller Chip Pin Function Chart

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>CpuGND</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>CpuV_{DD}</td><td>-</td><td>＋ power supply pin</td><td>No</td></tr>
<tr><td>CpuV_{DD}2</td><td>-</td><td>＋ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>・8-bit I/O port
・I/O specifiable in 4 bit units
・Pull-up resistors can be turned on and off in 4 bit units.
・HOLD reset input
・Port 0 interrupt input
・Pin functions
P00: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output/ SIO0 data output
P01: INT1 input/HOLD reset input/timer 0H capture input/SIO0 data input/bus I/O
P02: SIO0 clock I/O
P03: INT3 input (with noise filter input)/timer 0 event input/ timer 0H capture input
P04: AD conversion input terminal (AN4)
P05: AD conversion input terminal (AN5)
P06: AD conversion input terminal (AN6)/Output terminal for 32.768kHz crystal oscillation (XT2)
P07: AD conversion input terminal (AN7)/Input terminal for 32.768kHz crystal oscillation (XT1)
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT0</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr>
<tr><td>INT1</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr>
<tr><td>INT3</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table>
The two terminal of P00, P01, P04 and P05 can be used as LED driver.</td><td>P00-P03: No
P04-P07: Yes</td></tr>
<tr><td>Port 1
P11 to P17</td><td>I/O</td><td>・7-bit I/O port
・I/O specifiable in 1 bit units
・Pull-up resistors can be turned on and off in 1 bit units.
・Pin functions
P13: TVPWMD output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: SIO1 data input / bus I/O / data output
P17: SIO1 clock I/O /T1PWML output</td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P32</td><td>I/O</td><td>・3-bit I/O port (Internal connected terminal)
・I/O specifiable in 1 bit units
・ Pin functions
P30,P31: Internal communication interface terminal:
P32 : INT2 input / timer 0 event input/ timer 0L capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT2</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>No</td></tr>
<tr><td>RES#</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>FILT</td><td>Output</td><td>Internal PLL filter pin for system clock</td><td>No</td></tr>
<tr><td>$V_{DD}i1$</td><td>-</td><td>＋ power supply pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>$V_{DD}i2$</td><td>-</td><td>＋ power supply pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>RESi#</td><td>Input</td><td>Reset pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>XTIN</td><td>Input</td><td>Reference clock input (Internal connected terminal)</td><td>No</td></tr>
<tr><td>CVIN</td><td>Input</td><td>Video input pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>PEOUT</td><td>Output</td><td>Pedestal level output (Internal connected terminal)</td><td>No</td></tr>
<tr><td>VS#</td><td>Input</td><td>Vertical sync input pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>HS#</td><td>Input</td><td>Horizontal sync input pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>R</td><td>Output</td><td>Red (R) RGB video output pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>G</td><td>Output</td><td>Green (G) RGB video output pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>B</td><td>Output</td><td>Blue (B) RGB video output pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>BL1</td><td>Output</td><td>Fast blanking 1 control output pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>BL2</td><td>Output</td><td>Fast blanking 2 control output pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>DDSOUT</td><td>Output</td><td>DDS color sub-carrier output pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>DDSYS</td><td>Input</td><td>DDS color system selection pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>DDSIN</td><td>Input</td><td>DDS clock input pin (Internal connected terminal)</td><td>No</td></tr>
<tr><td>DAFTIN</td><td>Input</td><td>IF carrier input pin (Internal connected terminal)</td><td>No</td></tr>
</table>

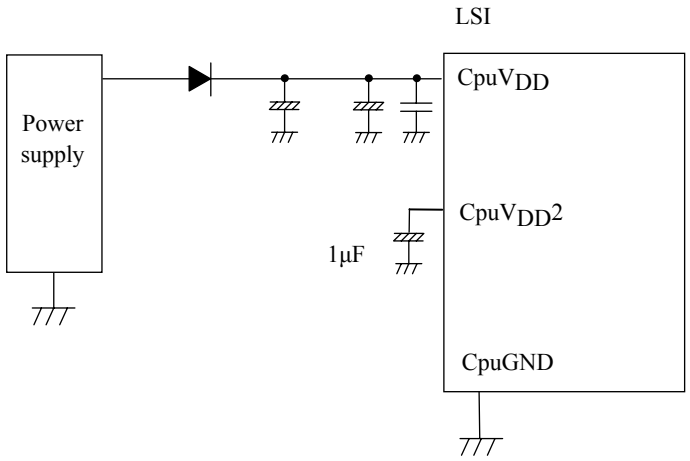
4. μ-Controller Chip Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P03	-	No	Nch-open drain	No
P04 to P07	1 bit	1	CMOS	Programmable (*8)
		2	Nch-open drain	No
P11 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	-	No	Nch-open drain	Yes
P32	-	No	Nch-open drain	No

(*8) Programmable pull-up resistors for port 0 are controlled in 4 bit units (P04 to P07).

*Connect the IC as shown below to minimize the noise input to the $CpuV_{DD}$ pin.



5. μ-Controller Chip On-board writing system

The LC87F3664A has the On-board writing system. The program is renewable by using SANYO Flash On-board System after the LSI has been installed on the application board.
This system has to connect the 6 pins (communication (CLK, DATA × 2), power supply ($CpuV_{DD}$, CpuGND) and RES#, pins) with the interface board of SANYO Flash On-board System.
It is necessary that the pins to be used for the rewriting system should be able to be separated from the application board properly.

Please ask to our sales persons before using On-board writing system.

6. µ-Controller Chip Electrical characteristics／Ta=-10deg to +65deg, V_{SS}=0V

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
High level input current	IIH(1)	Ports0,1	・Output disable ・Pull-up MOS Tr.OFF ・$V_{IN}=V_{DD}$ (including the off-leak current of the output Tr.)	4.5 to 5.5			1	µA
	IIH(2)	RES#	$V_{IN}=V_{DD}$	4.5 to 5.5			1	
Low level input current	IIL(1)	Ports0,1	・Output disable ・Pull-up MOS Tr.OFF ・$V_{IN}=V_{SS}$ (including the off-leak current of the output Tr.)	4.5 to 5.5	-1			
	IIL(2)	RES#	$V_{IN}=V_{SS}$	4.5 to 5.5	-1			
High level output voltage	$V_{O}H$	Ports04-07, Ports1	$I_{O}H$=-1.0mA	4.5 to 5.5	V_{DD}-1			V
Low level output voltage	$V_{O}L(1)$	Ports02,03 Ports06,07 Ports1	$I_{O}L$=10mA	4.5 to 5.5			1.5	
			$I_{O}L$=1.6mA	4.5 to 5.5			0.4	
	$V_{O}L(2)$	Ports00,01, Ports04,05	$I_{O}L$=8.0mA	4.5 to 5.5			0.4	
Pull-up MOS Tr. Resistance	Rpu	Ports04-07,1	$V_{O}H=0.9V_{DD}$	4.5 to 5.5	15	40	70	kΩ
Bus terminal short circuit resistance for internal communication	RBS	・P14-P30 ・P15-P31 ・P14-P16 ・P15-P17		4.5 to 5.5		130	300	Ω
Hysteresis voltage	VHIS	Ports00-03,1 ・RES#		4.5 to 5.5		0.35		V

7. µ-Controller Chip SIO0 Characteristics(*9) ／Ta=-10deg to +65deg, V_{SS}=0V

Parameter			Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Serial Clock	Input Clock	Cycle	tSCK(1)	SCK0(P02)	See the figure 4.	4.5 to 5.5	2			tCYC
		Low level pulse-width	tSCKL(1)				1			
		High level Pulse-width	tSCKH(1)				1			
			tSCKHA(1a)		・Continuous data transmitting and receiving mode ・See the figure 4. (*10)		4			
	Output Clock	Cycle	tSCK(2)	SCK0(P02)	・At the CMOS output selection ・See the figure 4.	4.5 to 5.5	4/3			
		Low level pulse-width	tSCKL(2)				1/2			tSCK
		Low level pulse-width	tSCKH(2)				1/2			
			tSCKHA(2a)		・At the CMOS output ・Continuous data transmitting and receiving mode ・See the figure 4.		tSCKH(2) + 2tCYC		tSCKH(2)+ (10/3)tCYC	tCYC
Serial Input	Data setup time		tsDI(1)	SI0(P01) SB0(P01)	・Define for rising of SIOCLK. ・See the figure 4.	4.5 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial Outpu	Input Clock	Output delay time	tdDO(1)	SO0(P00) SB0(P01)	・Continuous data transmitting and receiving mode (*11)	4.5 to 5.5			(1/3)tCYC +0.05	
			tdDO(2)		・Synchronous 8-bit mode (*11)				1tCYC +0.05	
	Output Clock		tdDO(3)		(*11)				(1/3)tCYC +0.05	

(*9) This limited value is theoretical figure. Be sure to ensure the margin in accordance with use situation.

(*10) When using the serial clock input with continuous data transmitting and receiving mode, lengthen time from the set of the cereal clock of SI0RUN in the state of "H" to the falling of the first cereal clock when it begins to send and receive continuous data more than tSCKHA.

(*11) This is defined for falling of SIOCLK and it is defined as time until output change start in open drain output. (See the figure 4)

8. µ-Controller Chip SIO1 Characteristics (*11) / Ta=-10deg to +65deg, V_{SS}=0V

Parameter			Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Serial Clock	Input Clock	Cycle	tSCK(3)	SCK1(P15)	See the figure 4.	4.5 to 5.5	2			tCYC
		Low level pulse-width	tSCKL(3)				1			
		High level pulse-width	tSCKH(3)				1			
	Output Clock	Cycle	tSCK(4)	SCK1(P15)	・At the CMOS output selection ・See the figure 4.	4.5 to 5.5	2			
		Low level pulse-width	tSCKL(4)				1/2			tSCK
		High level pulse-width	tSCKH(4)				1/2			
Serial Input	Data setup time		tsDI(2)	SI1(P14) SB1(P14)	・Define for rising of SIOCLK. ・See the figure 4.	4.5 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial Output	Output delay time		tdDO(4)	SO1(P16) SB1(P14)	・Define for falling of SIOCLK. ・Define as time until output change start in open drain output. ・See the figure 4.	4.5 to 5.5			(1/3)tCYC +0.05	

(*12) This limited value is theoretical figure. Be sure to ensure the margin in accordance with use situation.

9. µ-Controller Chip Pulse input conditions / Ta=-10deg to +65deg, V_{SS}=0V

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0,INT1,INT2	・Interrupt acceptable ・Timer0, 1 event input enabled	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/P03 (1/1 is selected for noise rejection clock.)	・Interrupt acceptable ・Timer0, 1 event input enabled	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/P03 (1/32 is selected for noise rejection clock.)	・Interrupt acceptable ・Timer0, 1 event input enabled	4.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3/P03 (1/128 is selected for noise rejection clock.)	・Interrupt acceptable ・Timer0, 1 event input enabled	4.5 to 5.5	256			
	tPIL(5)	RES#	Reset acceptable	4.5 to 5.5	200			µs

10. µ-Controller Chip AD converter characteristics / Ta=-10deg to +65deg, V_{SS}=0V

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Limits min	typ	max	unit
Resolution	N	AN3, AN4~AN7 (P04-P07)		4.5 to 5.5		6		bit
Absolute precision	ET		(*13)				±1	LSB
Conversion time	tCAD		Until result of conversion is ensured after Vref selection 1 bit conversion time = 3 × Tcyc			0.636		µs
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}				1	µA
	IAINL		VAIN=V_{SS}		-1			

(*13) Absolute precision does not include quantizing error (1/2LSB).

11. μ-Controller Chip Sample current dissipation characteristics / Ta=-10deg to +65deg, V_{SS}=0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored

Parameter	Symbol	Pins	Conditions	Limits				
				V_{DD}[V]	min	typ	max	unit
Current dissipation during basic operation (*14) (*15)	IDDOP(1)	CpuV_{DD}	·Reference clock=4.43MHz crystal oscillation (Operating mode: BipChip) System clock: V_{CO} (13.0MHz) ·VCO for OSD operating ·Built-in RC oscillation stops ·At the 1/1 frequency dividing ·OSD, DSL enabled	4.5 to 5.5		31	42	mA
	IDDOP(2)	CpuV_{DD}	·Reference clock=4.43MHz crystal oscillation (Stanby mode: BipChip) ·System clock: reference clock frequency dividing (32kHz) ·V_{CO} for the main clock and for OSD stops ·Built-in RC oscillation stops ·At the 1/2 frequency dividing	4.5 to 5.5		2	2.7	mA
Current dissipation in HALT mode (*14) (*15)	IDDHALT(1)	CpuV_{DD}	·HALT mode ·Reference clock=4.43MHz crystal oscillation (Stanby mode: BipChip) ·System clock: VCO (13.0MHz) ·VCO for OSD stops ·Built-in RC oscillation stops ·OSD, DSL enabled	4.5 to 5.5		5	8	mA
	IDDHALT(2)	CpuV_{DD}	·HALT mode ·Reference clock=4.43MHz crystal oscillation (Stanby mode: BipChip) ·System clock: Built-in RC oscillation ·V_{CO} for the main clock and for OSD stops ·At the 1/1 frequency dividing	4.5 to 5.5		1.7	3.2	mA
	IDDHALT(3)	CpuV_{DD}	·HALT mode ·Reference clock=4.43MHz crystal oscillation (Stanby mode: BipChip) ·System clock: reference clock frequency dividing (32kHz) ·V_{CO} for the main clock and for OSD stops ·Built-in RC oscillation stops ·At the 1/2 frequency dividing	4.5 to 5.5		1.3	2	mA
Current dissipation in HOLD mode (*15)	IDDHOLD	CpuV_{DD}	·HOLD mode ·All oscillation stop ·Reference clock=4.43MHz crystal oscillation (Stanby mode:BipChip)	4.5 to 5.5		1.2	1.9	mA

(*14) The currents of the output transistors and the internal pull-up MOS transistors are ignored.

(*15) 4.43MHz crystal oscillation current is contained.

12. μ-Controller Chip Ccrystal Oscillation Circuit and Sample Characteristics／Ta=-10deg to +65deg, V_{SS}=0V

When the base timer count of clock accuracy is necessary , LC87F3664A can use the port terminal (P06,P07) as the crystal oscillation (See the Figure 1). The sample oscillation circuit characteristics and recommended oscillation circuit when port terminal (P06, P07) is used as XTAL oscillation terminal are shown below.

The sample oscillation circuit characteristics in the table below is based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	TmsXtal (*16) Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		Typ	max	
32.768kHz	Epson TOYOCOM	MC-306	18pF	18pF	OPEN	390kΩ	4.5 to 5.5V	1.0S	1.5S	Applicable CL value = 12.5pF SMD-type

(*16) The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see the Figure 3).

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10deg to +65deg. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (P07/XT1 terminal P06/XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's CpuGND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

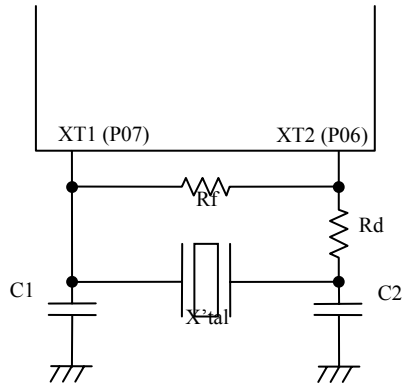


Figure 1 Recommended oscillation circuit.

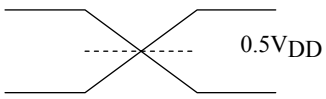
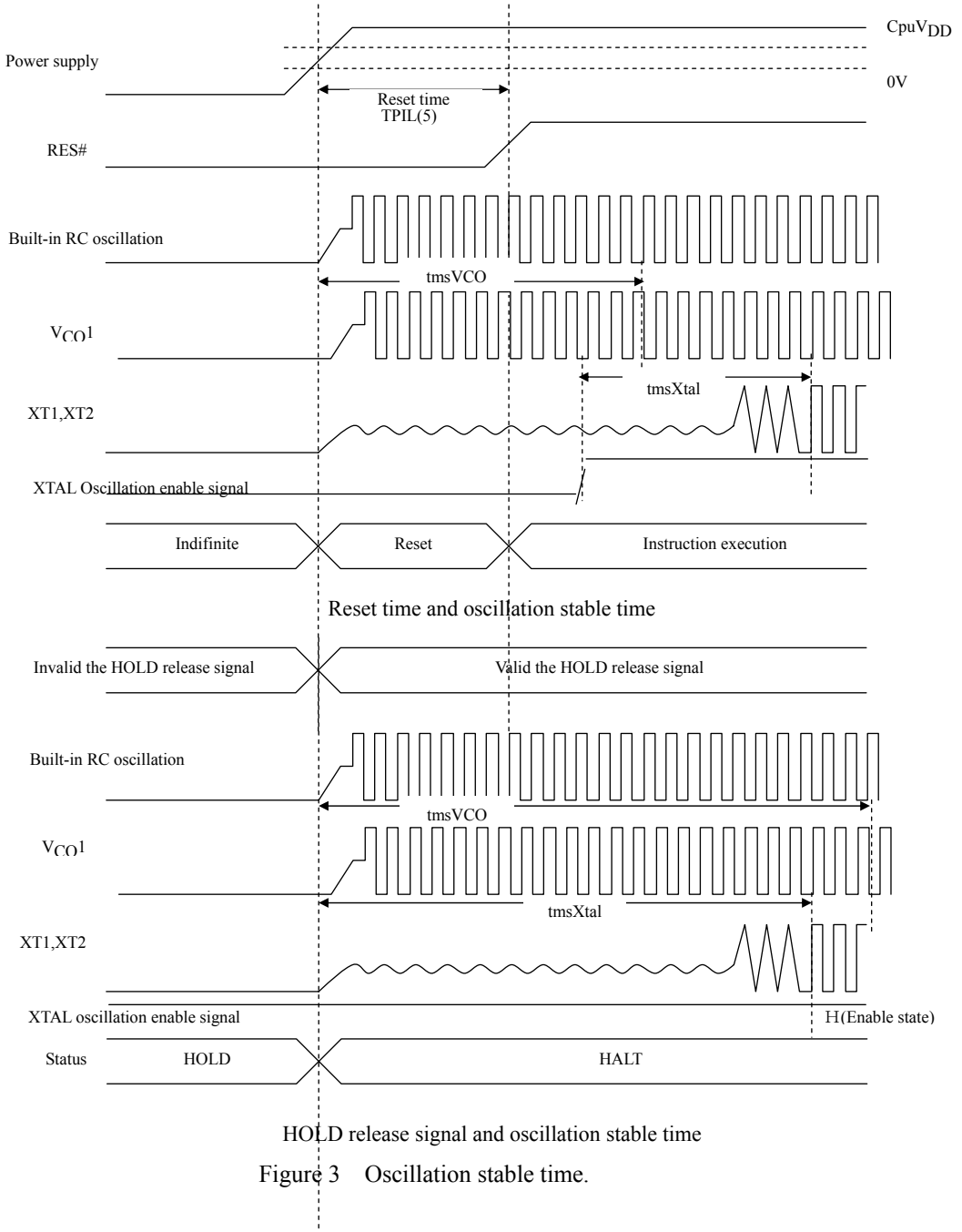


Figure 2 The Point of AC timing measure.



Reset time and oscillation stable time

HOLD release signal and oscillation stable time

Figure 3 Oscillation stable time.

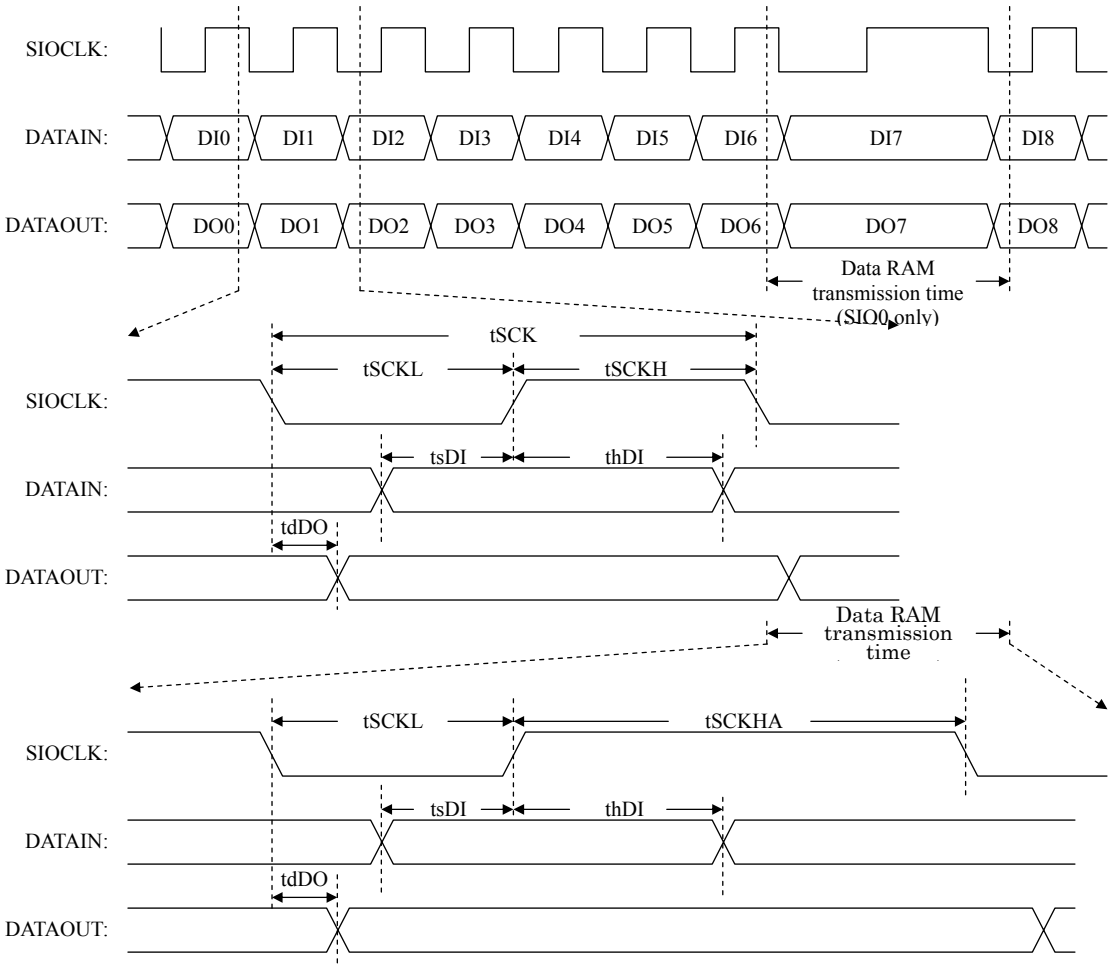


Figure 4 Serial I/O wave.

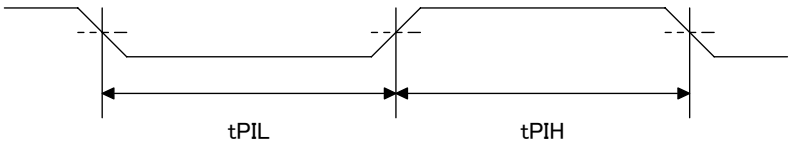


Figure 5 Pulse input timing wave.

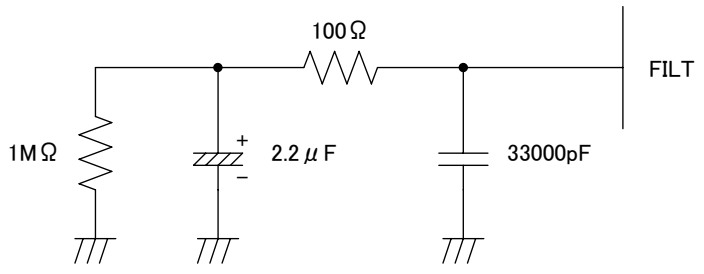


Figure 6 FILT recommended circuit.

(Note) Place FILT parts on board as close to the microcontroller as possible.

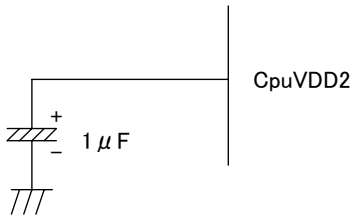


Figure 7 CpuV_{DD}2 recommended circuit.

(Note) Place CpuV_{DD}2 parts on board as close to the microcontroller as possible.

* Refer to the user's manual of LC873600 series,when you know the details about μ-Controller.