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MOTOROLA

MC54/74F283

4-BIT BINARY FULL ADDER (With Fast Carry)

The MC54/74F283 high-speed 4-bit binary full adder with internal carry lookahead, accepts two 4-bit binary words (A_0–A_3, B_0–B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0–S_3) and the Carry output (C_4) from the most significant bit. The F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

4-BIT BINARY FULL ADDER (With Fast Carry)

FAST™ SCHOTTKY TTL

FUNCTIONAL DESCRIPTION

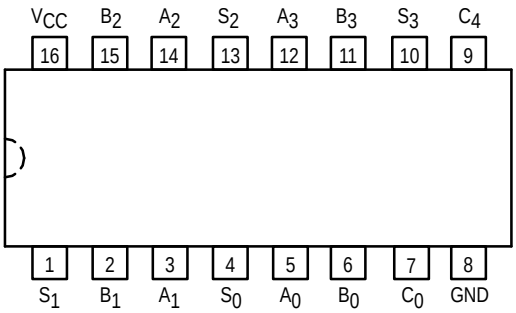
The F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0. The binary sum appears on the Sum (S_0–S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

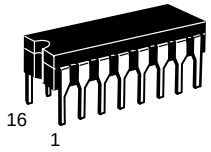
$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3)$
$= S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$
Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if C_0 is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

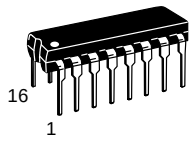
Due to pin limitations, the intermediate carries of the F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1–I_5 that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1–I_5 are true, the output M_5 is true.

CONNECTION DIAGRAM

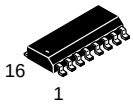




J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

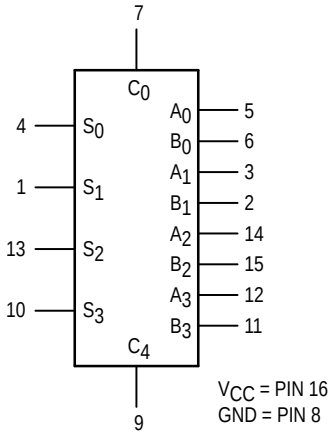


D SUFFIX
SOIC
CASE 751B-03

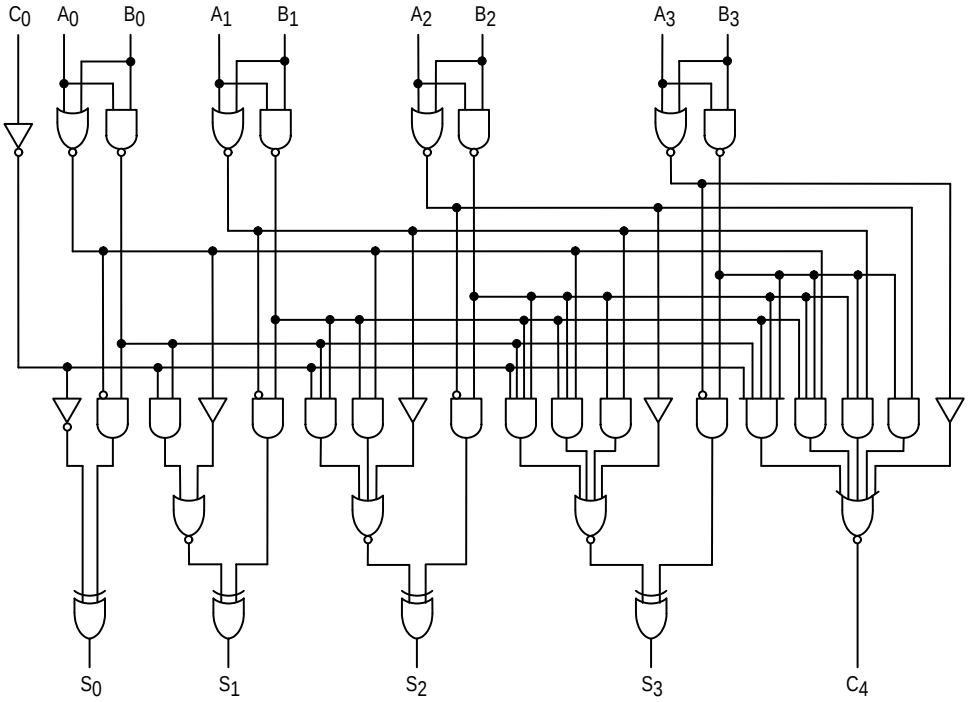
ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74	—	—	–1.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	20	mA

Figure A. Active-HIGH versus Active-LOW Interpretation

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

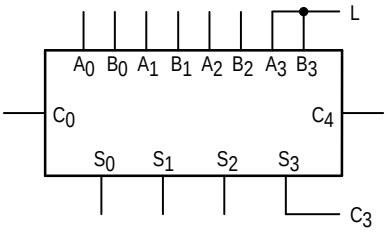


Figure B. 3-Bit Adder

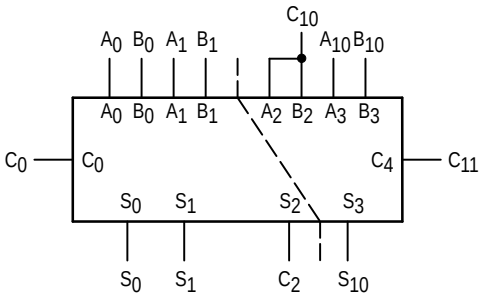


Figure C. 2-Bit and 1-Bit Adders

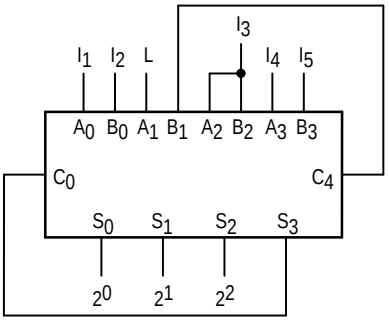


Figure D. 5-Input Encoder

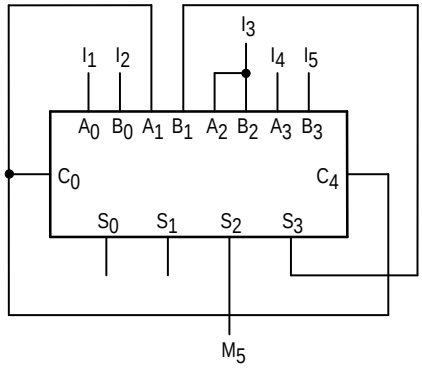


Figure E. 5-Input Majority Gate

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current C_0 Input				–0.6	mA	VIN = 0.5 V	VCC = MAX
	A and B Inputs				–1.2	mA		
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			36	55	mA	Inputs = 4.5 V	V_{CC} = MAX

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A = –55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_0 to S_n	3.5 4.0	7.0 7.0	9.5 9.5	3.5 4.0	14 14	3.5 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n	3.0 3.5	7.0 7.0	9.5 9.5	3.0 3.5	14 14	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay C_0 to C_4	3.5 3.0	5.7 5.4	7.5 7.0	3.5 3.0	10.5 10	3.5 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation A_n or B_n to C_4	3.0 3.0	5.7 5.3	7.5 7.0	3.0 3.0	10.5 10	3.0 3.0	8.5 8.0	ns