

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100/1000 Base T
- ✓ Cellular Phones
- ✓ Audio/Video Inputs
- ✓ Handheld Electronics
- ✓ Personal Digital Assistant (PDA)

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 μ s - Level 2(Line-Ground) & Level 3(Line-Line)

FEATURES

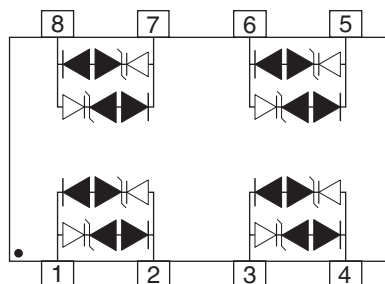
- ✓ 600 Watts Peak Pulse Power per Line ($t_p = 8/20\mu$ s)
- ✓ Provides Protection For Four Line Pairs
- ✓ ESD Protection > 40 kilovolts
- ✓ Low Leakage Current < 1.0 μ A
- ✓ Ultra Low Capacitance: 6pF Typical
- ✓ RoHS Compliant

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 70 milligrams (Approximate)
- ✓ Available in Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
Pure-Tin - Sn, 100: 260-270°C
- ✓ Consult Factory for Leaded Device Availability
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code, Logo, Date Code & Pin One Defined By Dot on Top of Package



PIN CONFIGURATION



SLVU2.8-8

DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20μs) - See Fig. 1	P _{PP}	600	Watts
Peak Pulse Current (tp = 8/20μs)	I _{PP}	30	Amps
Lead Soldering Temperature	I _{FRM}	260	°C
Operating Temperature	T _L	-55 to 150	°C
Storage Temperature	T _{STG}	-55 to 150	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

PART NUMBER	DEVICE MARKING	RATED STAND-OFF VOLTAGE (See Note 1)	MINIMUM BREAKDOWN VOLTAGE (See Note 1)	MINIMUM SNAPBACK VOLTAGE (See Note 1)	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2)				MAXIMUM LEAKAGE CURRENT (See Note 1)	TYPICAL CAPACITANCE (See Note 1)
					@ I _{PP} = 2A	@ I _{PP} = 5A	@ I _{PP} = 24A	@ I _{PP} = 30A		
		V _{WM} VOLTS	@ 1mA V ^(BR) VOLTS	@ I _{SB} = 50mA V _{SB} VOLTS	@ I _{PP} = 2A V _C VOLTS	@ I _{PP} = 5A V _C VOLTS	@ I _{PP} = 24A V _C VOLTS	@ I _{PP} = 30A V _C VOLTS	@ V _{WM} I _D μA	@ 0V, 1MHz C pF
SLVU2.8-8	SL8	2.8	3.0	2.8	5.5	8.5	15	17	1.0	6

Note 1: Device measured between pin 1 to 2, pin 3 to 4, pin 5 to 6 and pin 7 to 8.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

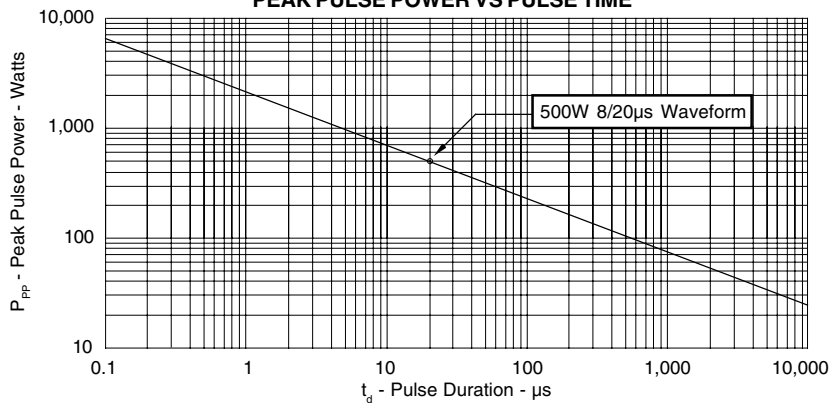
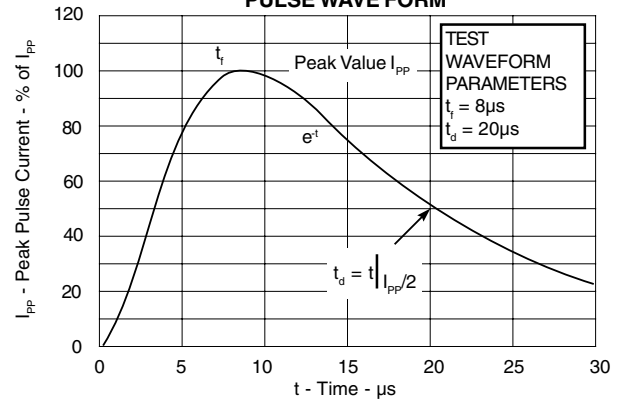
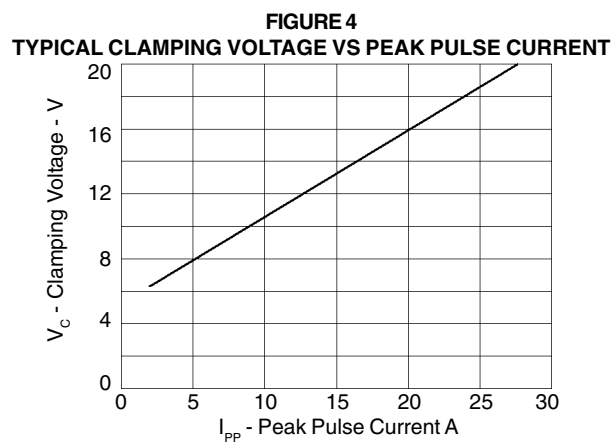
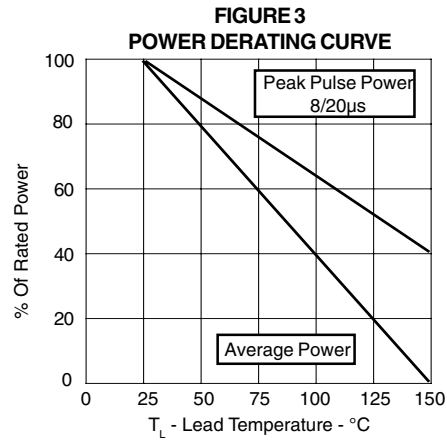


FIGURE 2
PULSE WAVEFORM



GRAPHS



SLVU2.8-8

APPLICATION NOTE

Electronic equipment is susceptible to damage caused by Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and tertiary lightning effects. Knowing that equipment can be damaged, the SLVU2.8-8 was designed to provide the level of protection required to safe guard sensitive equipment. This product can be used in different configurations to provide a level of protection to meet bidirectional requirements either in a common-mode or differential-mode configuration.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

The SLVU2.8-8 provides up to four lines of protection in a common-mode configuration as depicted in figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1
- ✓ Line 2 is connected to Pin 8
- ✓ Line 3 is connected to Pin 5
- ✓ Line 4 is connected to Pin 4
- ✓ Pins 2, 3, 6 and 7 are connected to ground

BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 2)

The SLVU2.8-8 provides up to four line pairs of protection in a differential-mode configuration as depicted in figure 2.

Circuit connectivity is as follows:

- ✓ Line Pair 1 is connected to Pins 1 & 2
- ✓ Line Pair 2 is connected to Pins 3 & 4
- ✓ Line Pair 3 is connected to Pins 7 & 8
- ✓ Line Pair 4 is connected to Pins 5 & 6

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1. Bidirectional Common-Mode Protection

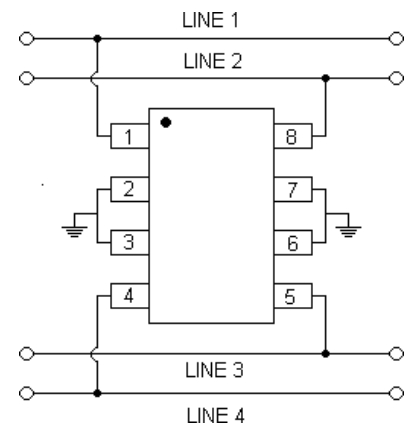
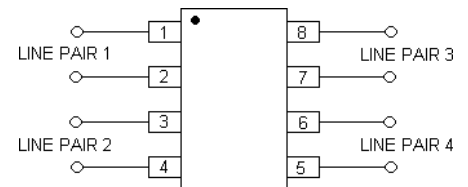
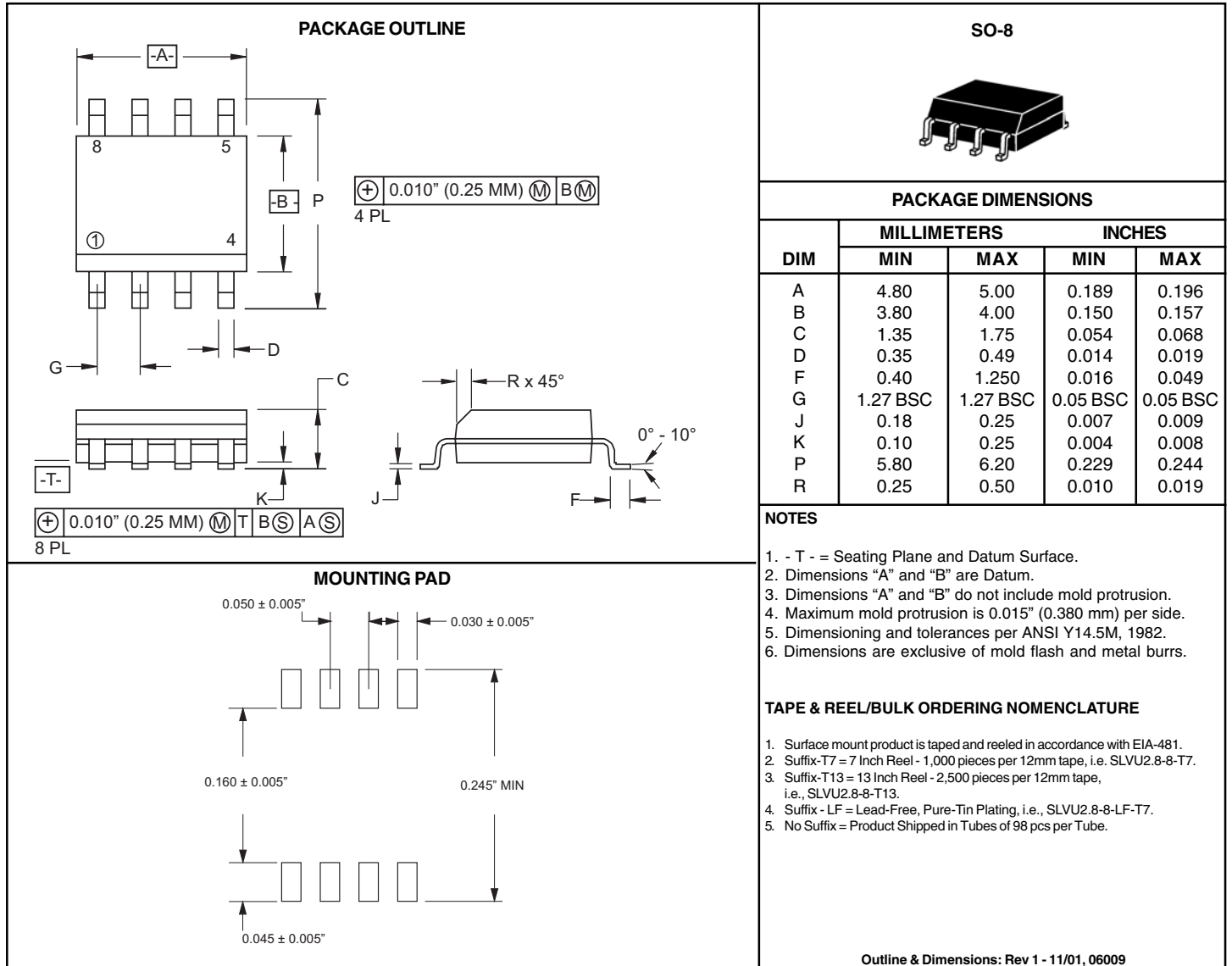


Figure 2. Bidirectional Differential-Mode Protection



SLVU2.8-8

SO-8 PACKAGE OUTLINE & DIMENSIONS



Outline & Dimensions: Rev 1 - 11/01, 06009

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