ALPHA & OMEGA SEMICONDUCTOR

AOL1432A

N-Channel SDMOS™ POWER Transistor

General Description

The AOL1432A is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

-RoHS Compliant
-Halogen Free

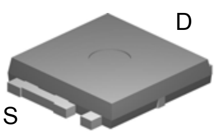
Features

V_{DS} (V) = 25V
I_D = 44A (${V_{GS}}$ = 10V)
$R_{DS(ON)}$ < 7.5mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ <14mΩ (V_{GS} = 4.5V)

100% UIS Tested!
100% R_g Tested!

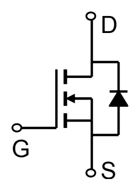
UltraSO-8™ Top View

D



S
G

Bottom tab connected to drain



Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	44	A
	T_C=100°C		31	
Pulsed Drain Current [C]		I_{DM}	120	
Continuous Drain Current [A]	T_A=25°C	I_{DSM}	12	
	T_A=70°C		10	
Avalanche Current [C]		I_{AR}	35	
Repetitive avalanche energy L=50µH [C]		E_{AR}	31	mJ
Power Dissipation [B]	T_C=25°C	P_D	30	W
	T_C=100°C		15	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.1	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14.2	20	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		48	60	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	3.5	5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250uA, V_{GS}=0V		25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V				10	μA
			T_J=55°C			50	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA		1.2	2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=30A			6	7.5	mΩ
			T_J=125°C		8.6	12	
		V_{GS}=4.5V, I_D=20A			11.5	14	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=30A			50		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current					44	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		990	1180	1450	pF
C_{oss}	Output Capacitance			210	275	350	pF
C_{rss}	Reverse Transfer Capacitance			125	175	245	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.1	1.7	2.5	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=30A		18	21.7	26	nC
Q_g(4.5V)	Total Gate Charge			9	11	13	nC
Q_{gs}	Gate Source Charge			3	4	5	nC
Q_{gd}	Gate Drain Charge			4.5	6.4	9	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.42Ω, R_{GEN}=3Ω			6.8		ns
t_r	Turn-On Rise Time				13.8		ns
$t_{D(off)}$	Turn-Off DelayTime				21.5		ns
t_f	Turn-Off Fall Time				8.7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=30A, dI/dt=500A/μs		8.4	10.6	13	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=30A, dI/dt=500A/μs		13	16	20	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev0 : July 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

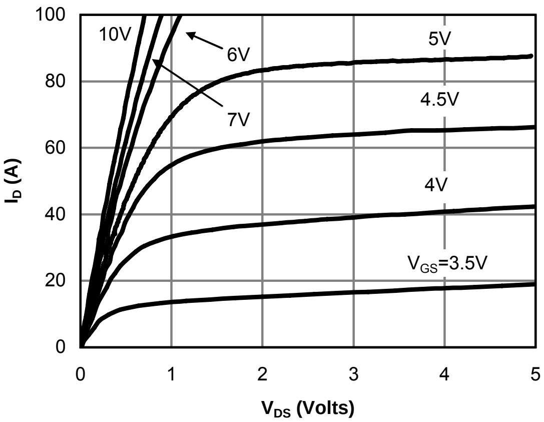


Fig 1: On-Region Characteristics

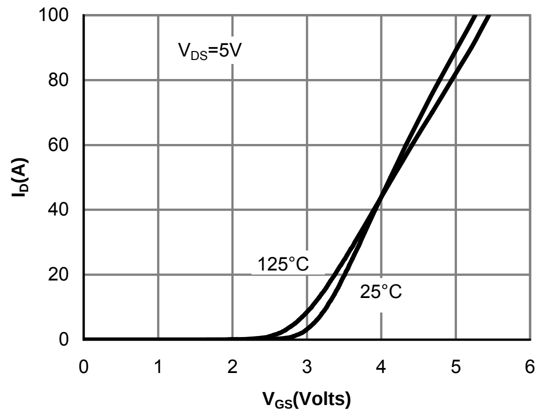


Figure 2: Transfer Characteristics

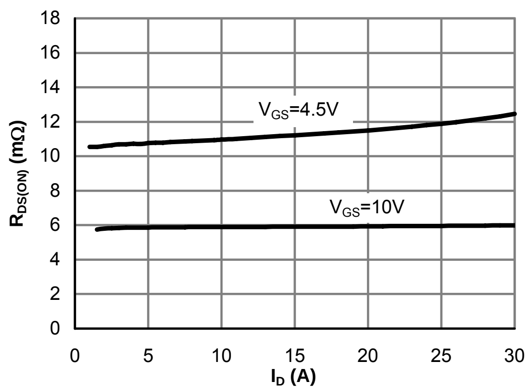


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

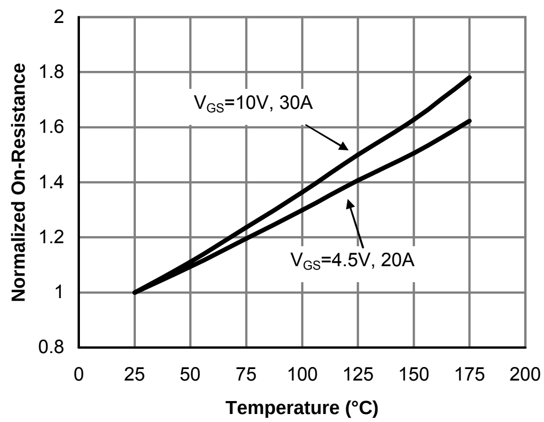


Figure 4: On-Resistance vs. Junction Temperature

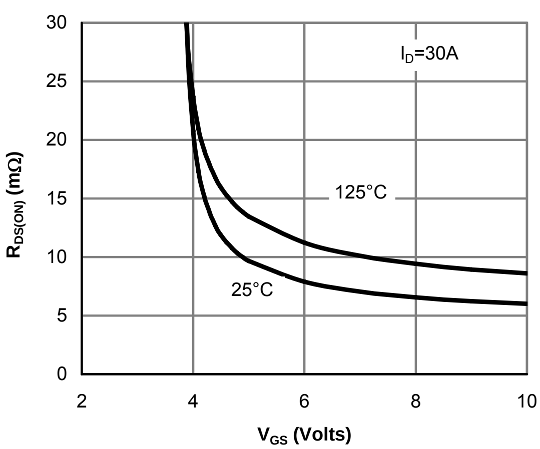


Figure 5: On-Resistance vs. Gate-Source Voltage

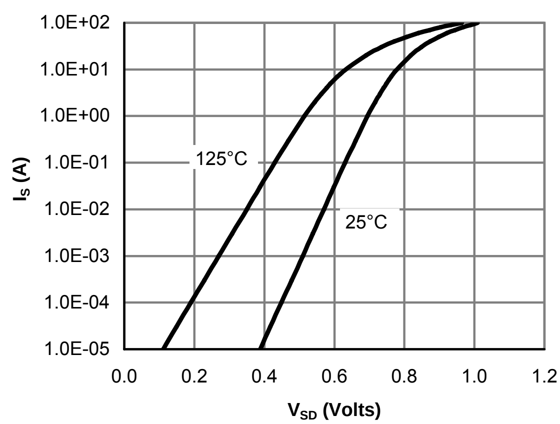


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

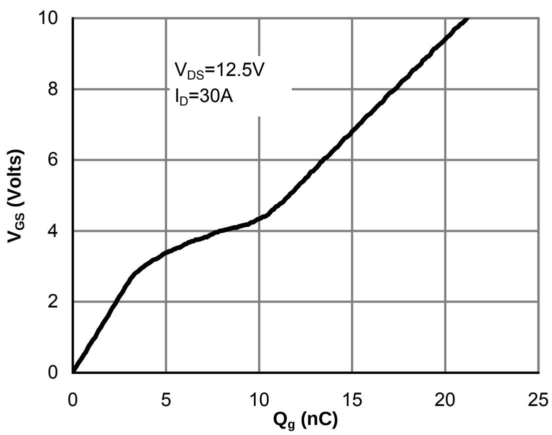


Figure 7: Gate-Charge Characteristics

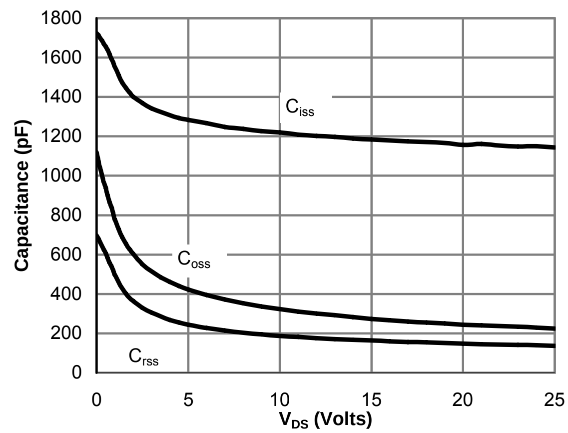


Figure 8: Capacitance Characteristics

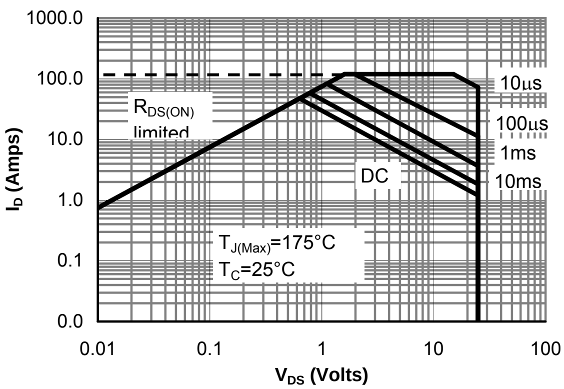


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

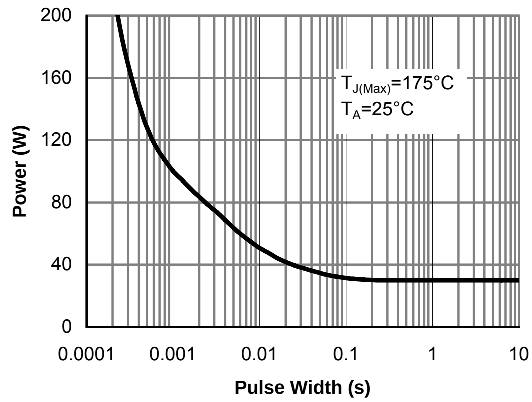


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

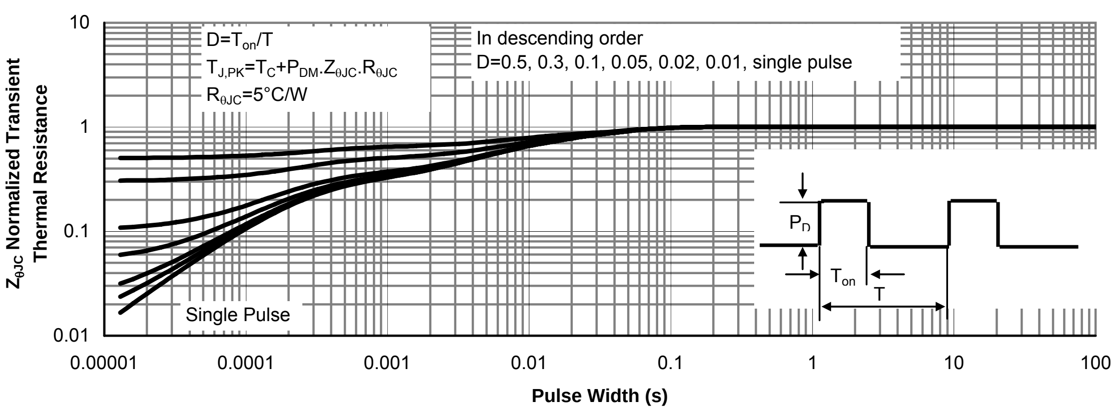


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

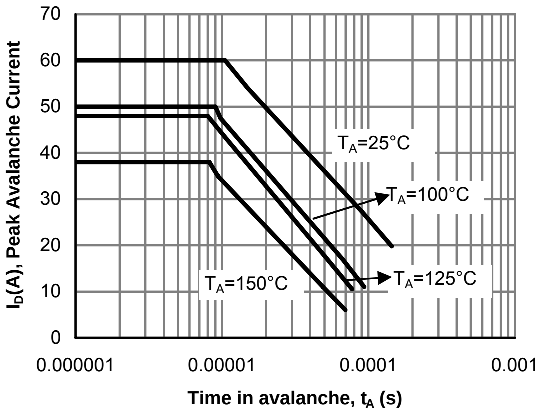


Figure 12: Single Pulse Avalanche capability

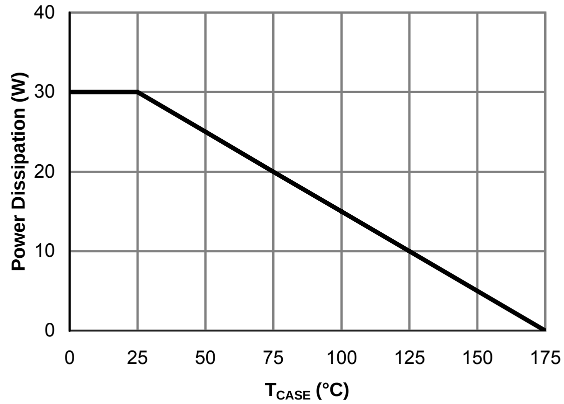


Figure 13: Power De-rating (Note B)

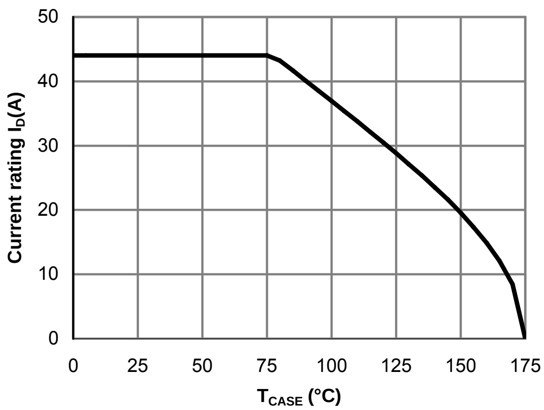


Figure 14: Current De-rating (Note B)

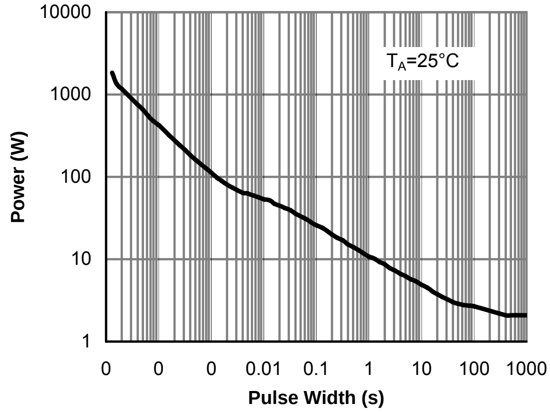


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

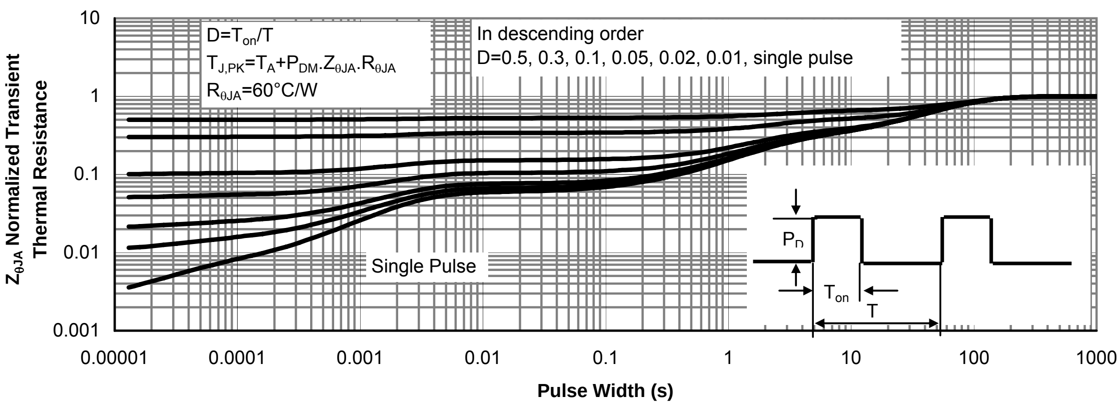


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

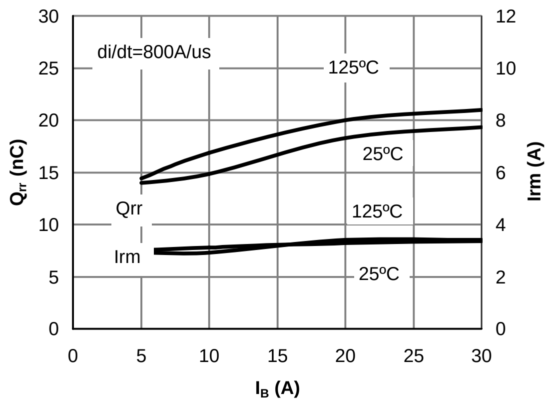


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

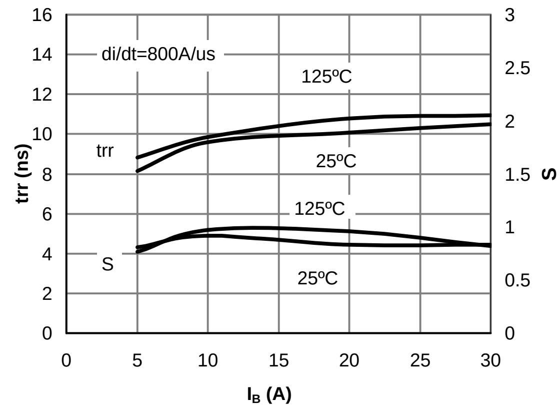


Figure 18: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

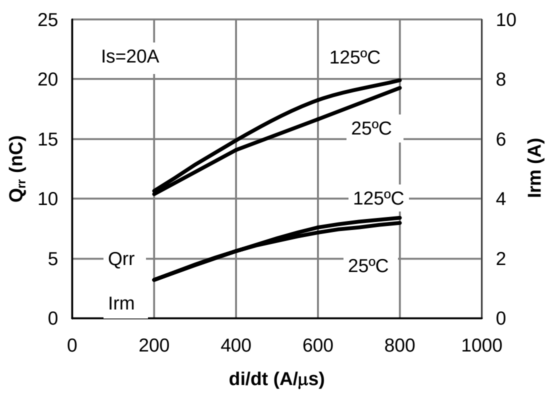


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

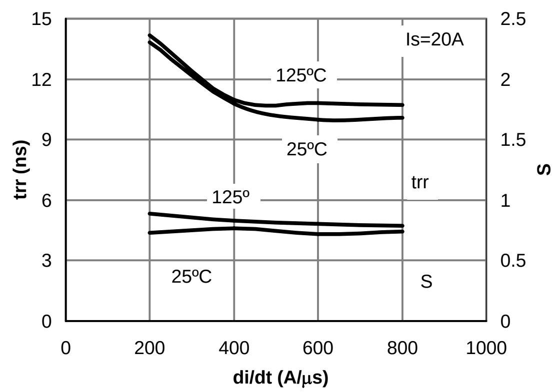
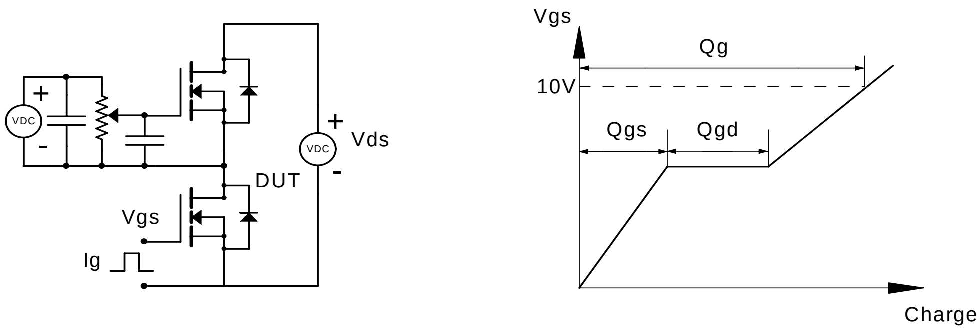
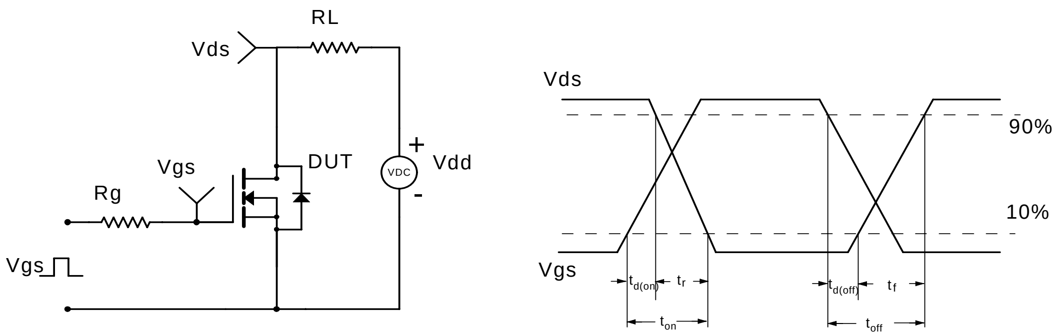


Figure 20: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

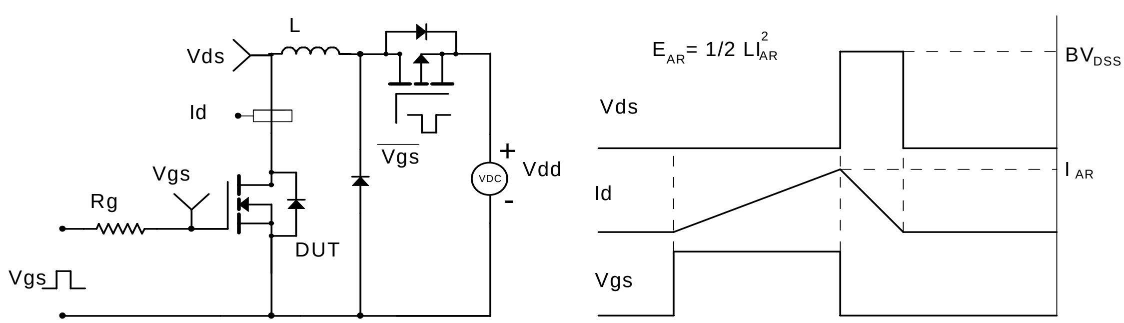
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms