AN-9731

LED Application Design Guide Using BCM Power Factor Correction (PFC) Controller for 100W Lighting System

1. Introduction

This application note presents practical step-by-step design considerations for a Boundary-Conduction-Mode (BCM) Power-Factor-Correction (PFC) converter employing Fairchild PFC controller, FL7930. It includes designing the inductor and Zero-Current-Detection (ZCD) circuit, selecting the components, and closing the control loop. The design procedure is verified through an experimental 140W prototype converter.

Unlike the Continuous Conduction Mode (CCM) technique often used at this power level, BCM offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less-expensive diodes without sacrificing efficiency.

The FL3930B provides an additional OVP pin that can be used to shut down the boost power stage when output voltage exceeds the OVP level due to damaged resistors connected at the INV pin. The FL7930C provides a PFC-ready pin can be used to trigger other power stages when PFC output voltage reaches the proper level (with hysteresis). This signal can be used as the V_{CC} trigger signal for another power stage controller after PFC stage or be transferred to the secondary side to synchronize the operation with PFC voltage condition. This simplifies the external circuit around the PFC controller and saves BOM cost. The internal proprietary logic for detecting input voltage improves the stability of PFC operation. Together with the maximum switching frequency clamping at 300kHz, FL7930 can limit inductor current to within pre-designed ranges at one or two cycles of the AC-input-absent test to simulate a sudden blackout. Due to the startup-without-overshoot design, audible noise from repetitive OVP triggering is eliminated. Protection functions include output over-voltage, over-current, open-feedback, and under-voltage lockout.

An Excel®-based design tool is available with this application note and the design result is shown with the calculation results as an example.

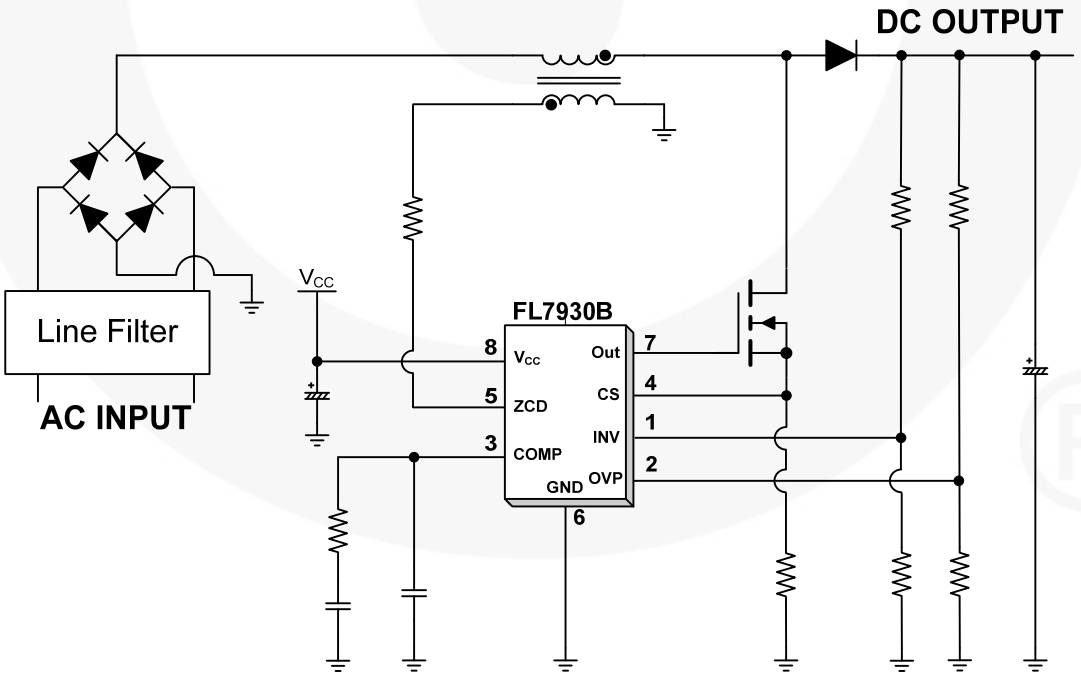


Figure 1. Typical Application Circuit

2. Operation Principle of BCM Boost PFC Converter

The most widely used operation modes for the boost converter are Continuous Conduction Mode (CCM) and Boundary Conduction Mode (BCM). These two descriptive names refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. As the names indicate, the inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. Even though the BCM operation has higher RMS current in the inductor and switching devices, it allows better switching condition for the MOSFET and the diode. As shown in Figure 2, the diode reverse recovery is eliminated and a fast-recovery diode is not needed. The MOSFET is also turned on with zero current, which reduces the switching loss.

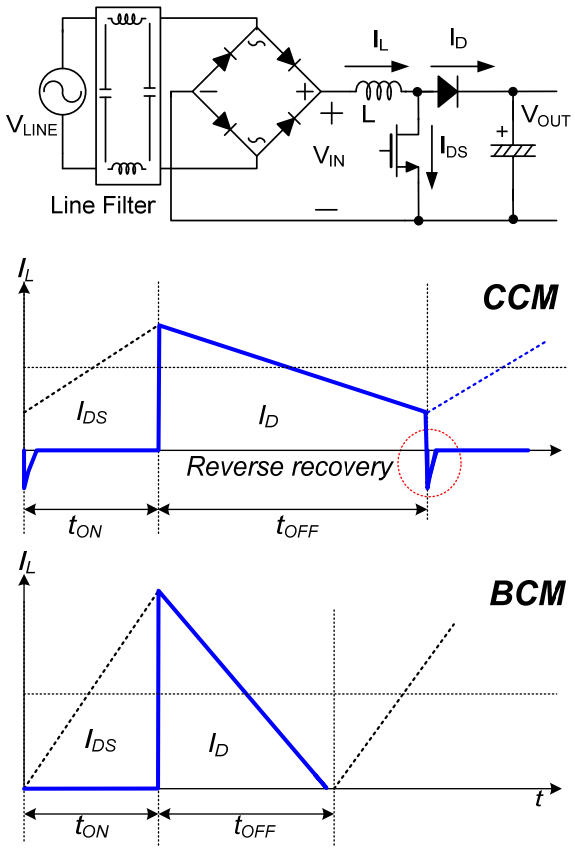


Figure 2. CCM vs. BCM Control

The fundamental idea of BCM PFC is that the inductor current starts from zero in each switching period, as shown in Figure 3. When the power transistor of the boost converter is turned on for a fixed time, the peak inductor current is proportional to the input voltage. Since the current waveform is triangular; the average value in each switching period is proportional to the input voltage. In a sinusoidal input voltage, the input current of the converter follows the input voltage waveform with very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation an ideal candidate for power factor correction.

A by-product of BCM is that the boost converter runs with variable switching frequency that depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input current follows the sinusoidal input voltage waveform, as shown in Figure 3. The lowest frequency occurs at the peak of sinusoidal line voltage.

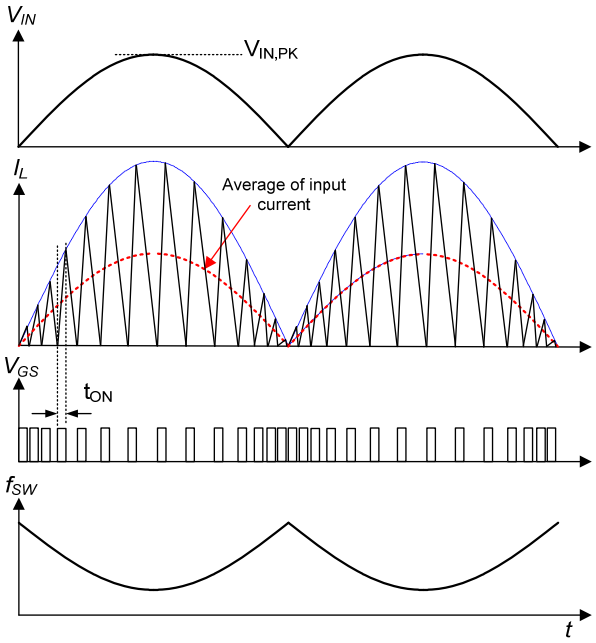


Figure 3. Operation Waveforms of BCM PFC

The voltage-second balance equation for the inductor is:

$$V_{IN}(t)\cdot t_{ON} = (V_{OUT} - V_{IN}(t))\cdot t_{OFF} \quad (1)$$

where $V_{IN(t)}$ is the rectified line voltage and V_{OUT} is the output voltage.

The switching frequency of BCM boost PFC converter is:

$$f_{SW} = \frac{1}{t_{ON}+t_{OFF}} = \frac{1}{t_{ON}}\cdot\frac{V_{OUT}-V_{IN}(t)}{V_{OUT}} = \frac{1}{t_{ON}}\cdot\frac{V_{OUT}-V_{IN,PK}\cdot\left|\sin(2\pi\cdot f_{LINE}\cdot t)\right|}{V_{OUT}} \quad (2)$$

where $V_{IN,PK}$ is the amplitude of the line voltage and f_{LINE} is the line frequency.

Figure 4 shows how the MOSFET on time and switching frequency change as output power decreases. When the load decreases, as shown in the right side of Figure 4, the peak inductor current diminishes with reduced MOSFET on time and, therefore, the switching frequency increases. Since this can cause severe switching losses at light-load condition and too-high switching frequency operation may occur at startup, the maximum switching frequency is limited to 300kHz.

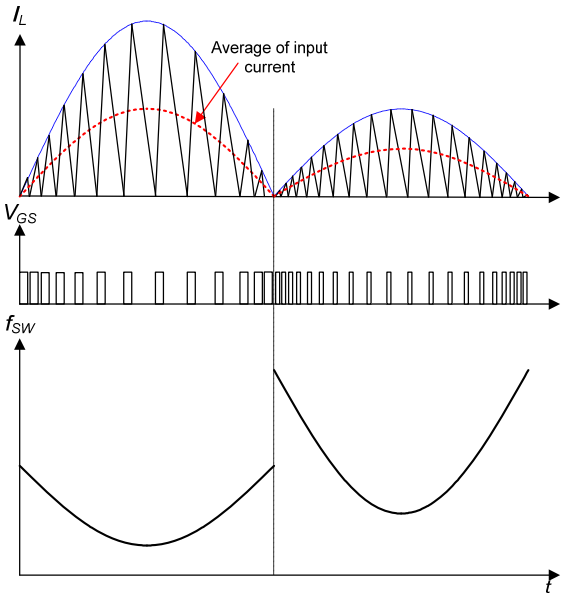


Figure 4. Frequency Variation of BCM PFC

Since the design of the filter and inductor for a BCM PFC converter with variable switching frequency should be at minimum frequency condition, it is worthwhile to examine how the minimum frequency of BCM PFC converter changes with operating conditions.

Figure 5 shows the minimum switching frequency, which occurs at the peak of line voltage as a function of the RMS line voltage for three output voltage settings. It is interesting that, depending on where the output voltage is set, the minimum switching frequency may occur at the minimum or at the maximum line voltage. When the output voltage is approximately 405V, the minimum switching frequency is the same for both low line ($85V_{AC}$) and high line ($265V_{AC}$).

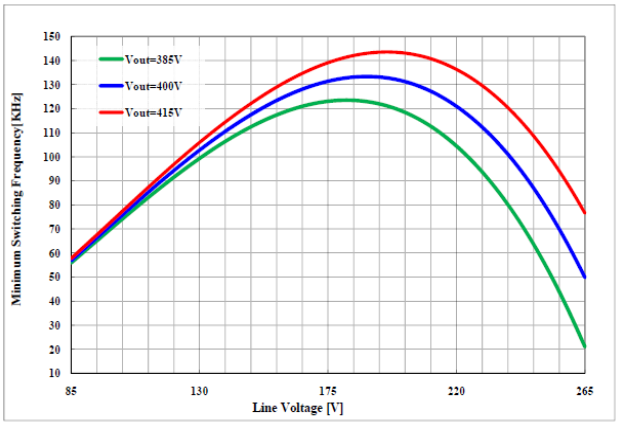


Figure 5. Minimum Switching Frequency vs. RMS Line Voltage (L = 280μH, P_{OUT} = 140W)

3. Startup without Overshoot and AC-Absent Detection

Feedback control speed of the PFC is typically quite slow. Due to the slow response, there is a gap between output voltage and feedback control. That is why Over-Voltage Protection (OVP) is critical at the PFC controller. Voltage dip caused by fast load change from light to heavy is diminished by a large bulk capacitor. OVP is easily triggered at startup. Switching starting and stopping by OVP at startup may cause audible noise and can increase voltage stress at startup, which may be higher than normal operation. This operation is improved when soft-start time is very long. However, too-long startup time raises the time needed for the output voltage to reach the rated value, especially at light load. FL7930 includes a startup-without-overshoot feature. During startup, the feedback loop is controlled by an internal proportional gain controller and, when output voltage approaches the rated value, changes to the external compensator after an internally fixed transition time described in the Figure 6. In short, an internal proportional gain controller prevents overshoot at startup; an external conventional compensator takes over after startup.

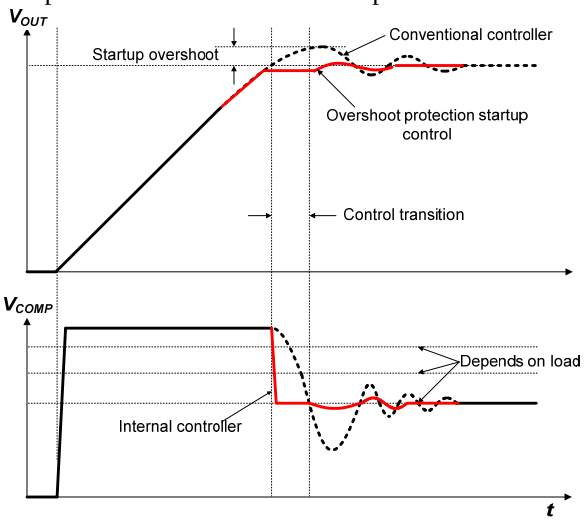


Figure 6. Startup Without Overshoot

FL7930 eliminates AC input voltage detection to save the power loss caused by an input-voltage-sensing resistor array and to optimize THD. Therefore, no information about input voltage is available at the internal controller. In many cases, the V_{CC} of PFC controller is supplied by an independent power source, like standby power. When the electric power is suddenly interrupted during one or two AC line periods, V_{CC} is still alive during that time and PFC output voltage drops. Accordingly, the control loop tries to compensate output voltage drop and control voltage reaches its maximum. When AC line input voltage is live, control voltage allows high switching current and creates stress on the MOSFET and diode. To protect against this, FL7930 checks if the input AC voltage exists. Once the controller verifies that the input voltage does not exist, soft-start is reset and waits until AC input voltage is applied again. Soft-start manages the turn-on time for smooth, operation after detecting that the AC voltage is live and results in less voltage and current stress during startup.

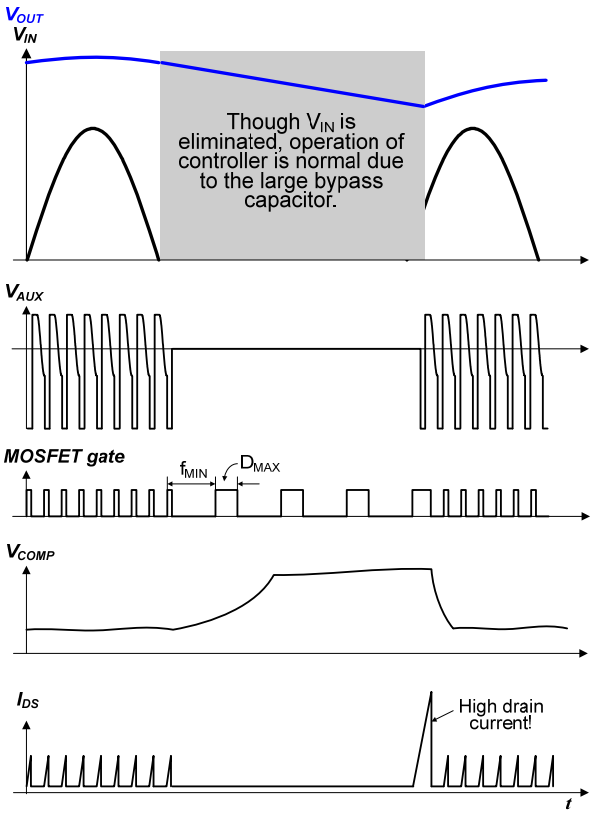


Figure 7. AC-Off Operation without AC-Absent Detection Circuit

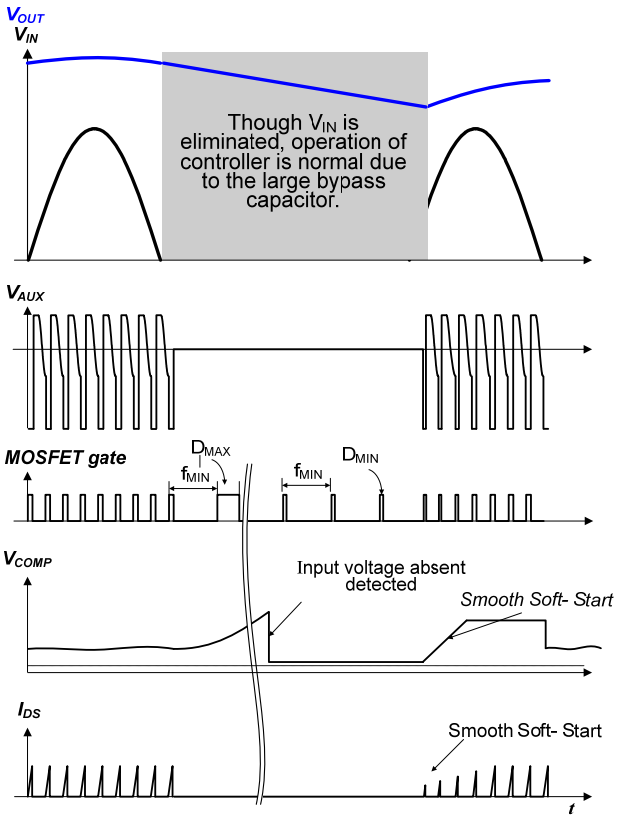


Figure 8. AC-Off Operation with AC-Absent Detection Circuit

4. Design Considerations

In this section, a design procedure is presented using the schematic in Figure 9 as a reference. A 140W PFC application with universal input range is selected as a design example. The design specifications are:

- Line Voltage Range: 90~265V_{AC} (Universal Input), 50Hz
- Nominal Output Voltage and Current: 400V/0.35A (140W)
- Hold-up Time Requirement: Output Voltage Should Not Drop Below 330V During One Line Cycle
- Output Voltage Ripple: Less than 8V_{PP}
- Minimum Switching Frequency: Higher than 50kHz
- Control Bandwidth: 5~15Hz
- V_{CC} Supplied from Auxiliary Power Supply.

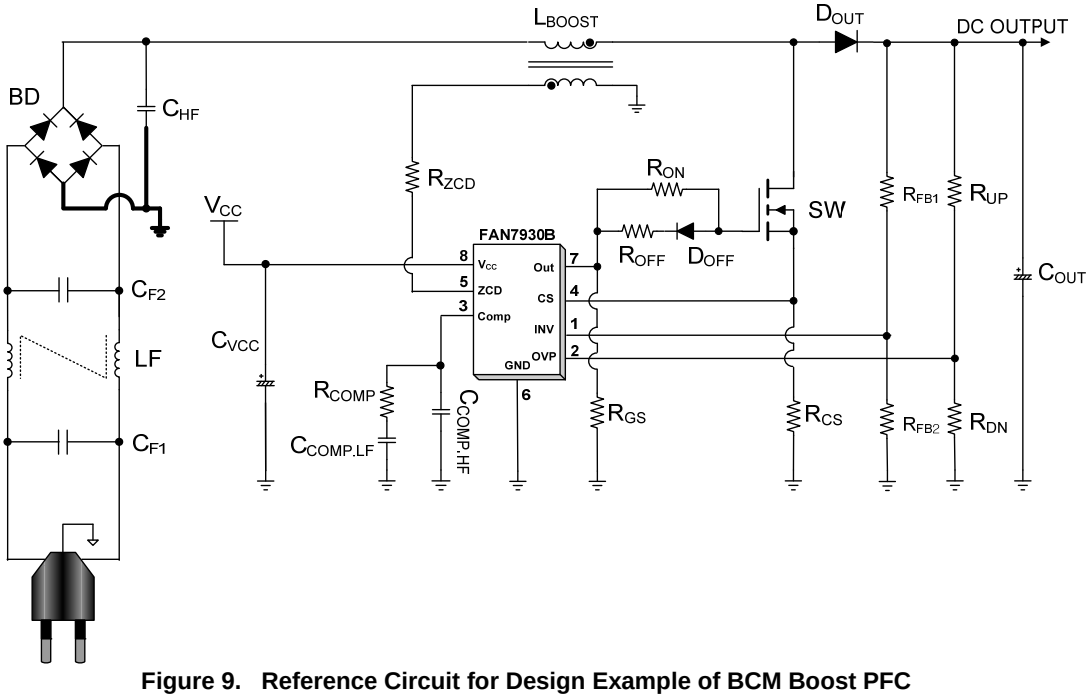


Figure 9. Reference Circuit for Design Example of BCM Boost PFC

[STEP-1] Define System Specifications

- Line Frequency Range ($V_{LINE,MIN}$ and $V_{LINE,MAX}$)
- Line Frequency (f_{LINE})
- Output Voltage (V_{OUT})
- Output Load Current (I_{OUT})
- Output Power ($P_{OUT} = V_{OUT} \times I_{OUT}$)
- Estimated Efficiency (η)

To calculate the maximum input power, it is necessary to estimate the power conversion efficiency. At universal input range, efficiency is recommended at 0.9; 0.93~0.95 is recommended when input voltage is high.

When input voltage is set at the minimum, input current becomes the maximum to deliver the same power compared at high line. Maximum boost inductor current can be detected at the minimum line voltage and at its peak. Inductor current can be divided into two categories; rising current when MOSFET is on and output diode current when MOSFET is off, as shown in Figure 10.

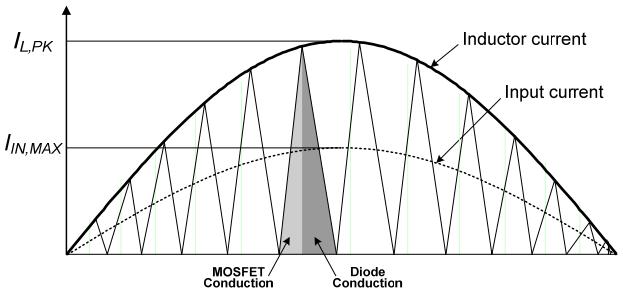


Figure 10. Inductor and Input Current

Because switching frequency is much higher than line frequency, input current can be assumed to be constant during a switching period, as shown in Figure 11.

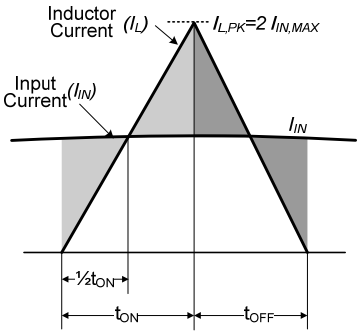


Figure 11. Inductor and Input Current

With the estimated efficiency, Figure 10 and Figure 11 inductor current peak *($I_{L,PK}$)*, maximum input current *($I_{IN,MAX}$)*, and input RMS (Root Mean Square) current *($I_{IN,MAXRMS}$)* are given as:

$$I_{L,PK} = \frac{4 \cdot P_{OUT}}{\eta \cdot \sqrt{2} \cdot V_{LINE,MIN}} \ [A] \quad (3)$$

$$I_{IN,MAX} = I_{L,PK} / 2 \ [A] \quad (4)$$

$$I_{IN,MAXRMS} = I_{IN,MAX} / \sqrt{2} \ [A] \quad (5)$$

(Design Example) Input voltage range is universal input, output load is 350mA, and estimated efficiency is selected as 0.9.

$$V_{LINE,MIN} = 90V_{AC},\ V_{LINE,MAX} = 265V_{AC}$$
$$f_{LINE} = 50Hz$$
$$V_{OUT} = 400V,\ I_{OUT} = 350mA$$
$$\eta = 0.9$$

$$I_{L,PK} = \frac{4 \cdot P_{OUT}}{\eta \cdot \sqrt{2} \cdot V_{LINE,MIN}} = \frac{4 \cdot 400V \cdot 0.35A}{0.9 \cdot \sqrt{2} \cdot 90} = 4.889A$$

$$I_{IN,MAX} = \frac{I_{L,PK}}{2} = \frac{4.889A}{2} = 2.444A$$

$$I_{IN,MAXRMS} = \frac{I_{IN,MAX}}{\sqrt{2}} = \frac{2.444A}{\sqrt{2}} = 1.728A$$

1. Define System Specifications		
Minimum Line Voltage ($V_{LINE,MIN}$)	90	V_{AC}
Maximum Line Voltage ($V_{LINE,MAX}$)	265	V_{AC}
Typical Line Voltage for Transfer Function	230	V_{AC}
Line Frequency	50	Hz
Output specification		
Output Voltage (V_{OUT})	400	V
Output Current (I_{OUT})	350	mA
Minimum Output Current for Transfer Function	125	mA
Estimated Efficiency (η)	0.90	
Output Power (P_{OUT})	140.00	W
Input Power (P_{IN})	155.56	W
Maximum Peak Inductor Current ($I_{L,PK}$)	4.889	A
Maximum Input Current ($I_{IN,MAX}$)	2.444	A
Maximum RMS Input Current ($I_{IN,MAXRMS}$)	1.728	A
Max Peak Inductor Current@$V_{LINE,MAX}$ ($I_{L,PK}$@$V_{LINE,MAX}$)	1.660	A
Maximum Input Current@$V_{LINE,MAX}$ ($I_{IN,MAX}$@$V_{LINE,MAX}$)	0.830	A
Max RMS Input Current@$V_{LINE,MAX}$ ($I_{IN,MAXRMS}$@$V_{LINE,MA}$	0.587	A

[STEP-2] Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. The minimum switching frequency must be higher than the maximum audible frequency band of 20kHz. Minimum frequency near 20kHz can decrease switching loss with the cost of increased inductor size and line filter size. Too-high minimum frequency may increase the switching loss and make the system respond to noise. Selecting in the range of about 30~60kHz is a common choice; 40~50kHz is recommended with FL7930.

The minimum switching frequency may appear at minimum input voltage or maximum input voltage, depending on the output voltage level. When PFC output voltage is less than 405V, minimum switching appears at the maximum input voltage, according to Fairchild application note AN-6086. The inductance is obtained using the minimum switching frequency:

$$L = \frac{\eta \cdot \left(\sqrt{2}V_{LINE}\right)^2}{4 \cdot f_{SW,MIN} \cdot P_{OUT} \cdot \left(1 + \frac{\sqrt{2}V_{LINE}}{V_{OUT} - \sqrt{2}V_{LINE}}\right)} \ [H] \quad (6)$$

where L is boost inductance and $f_{SW,MIN}$ is the minimum switching frequency.

The maximum on time needed to carry peak inductor current is calculated as:

$$t_{ON,MAX} = L \cdot \frac{I_{L,PK}}{\sqrt{2} \cdot V_{LINE,MIN}} \ [s] \quad (7)$$

Once inductance and the maximum inductor current are calculated, the number of turns of the boost inductor should be determined considering the core saturation. The minimum number of turns is given as:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L[\mu H]}{A_e[mm^2] \cdot \Delta B} \ [Turns] \quad (8)$$

where A_e is the cross-sectional area of core and ΔB is the maximum flux swing of the core in Tesla. ΔB should be set below the saturation flux density.

Figure 12 shows the typical B-H characteristics of ferrite core from TDK (PC45). Since the saturation flux density (Δ*B*) decreases as the temperature increases, the high temperature characteristics should be considered.

RMS inductor current *($I_{L,RMS}$)* and current density of the coil *($I_{L,DENSITY}$)* can be given as:

$$I_{L,RMS} = \frac{I_{L,PK}}{\sqrt{6}} \ [A] \quad (9)$$

$$I_{L,DENSITY} = \frac{I_{L,RMS}}{\pi \cdot \left(d_{wire}/2\right)^2 \cdot N_{wire}} \ [A/mm^2] \quad (10)$$

where d_{WIRE} is the diameter of winding wire and N_{WIRE} is the number of strands of winding wire.

When selecting wire diameter and strands; current density, window area *(A_W, refer to* Figure 13*)* of selected core, and fill factor need to be considered. The winding sequence of the boost inductor is relatively simple compared to a DC-DC converter, so fill factor can be assumed about 0.2~0.3.

Layers cause the skin effect and proximity effect in the coil, so real current density may be higher than expected.

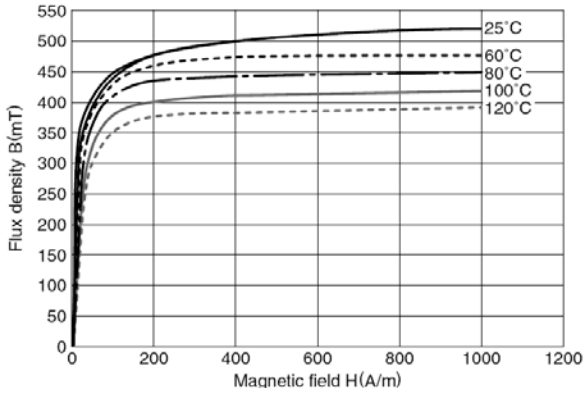


Figure 12. Typical B-H Curves of Ferrite Core

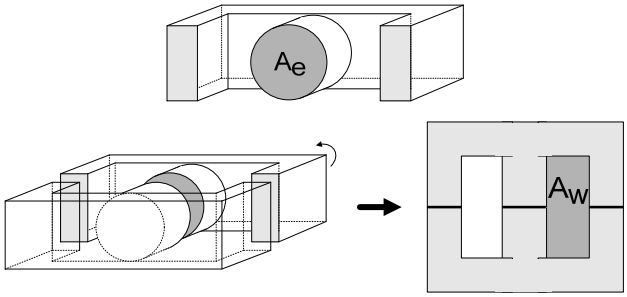


Figure 13. A_e and A_W

(Design Example) Since the output voltage is 400V, the minimum frequency occurs at high-line ($265V_{AC}$) and full-load condition. Assuming the efficiency is 90% and selecting the minimum frequency as 50kHz, the inductor value is obtained as:

$$L = \frac{\eta \cdot \left(\sqrt{2}V_{LINE}\right)^2}{4 \cdot f_{SW,MIN} \cdot P_{OUT} \cdot \left(1 + \frac{\sqrt{2}V_{LINE}}{V_{OUT} - \sqrt{2}V_{LINE}}\right)}$$

$$= \frac{0.9 \cdot \left(\sqrt{2} \times 265\right)^2}{4 \cdot 50 \cdot 10^3 \cdot 140 \cdot \left(1 + \frac{\sqrt{2} \cdot 265}{400 - \sqrt{2} \cdot 265}\right)} = 284.4[\mu H]$$

Assuming EER3019N core (PL-7, A_e=137mm^2) is used and setting ΔB as 0.3T, the primary winding should be:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L[\mu H]}{A_e[mm^2] \cdot \Delta B} = \frac{6.984 \cdot 284}{137 \cdot 0.3} = 34[T]$$

The number of turns (N_{BOOST}) of the boost inductor is determined as 34 turns.

When 0.10mm diameter and 50-strand wire is used, RMS current of inductor coil and current density are:

$$I_{L,RMS} = \frac{I_{L,PK}}{\sqrt{6}} = \frac{4.889}{\sqrt{6}} = 2[A]$$

$$I_{L,DENSITY} = \frac{I_{L,RMS}}{\pi \cdot \left(d_{wire}/2\right)^2 \cdot N_{wire}} = \frac{2}{\pi \cdot (0.1/2)^2 \cdot 50} = 5.1 \ [A/mm^2]$$

2. Boost Inductor Design		
Minimum Switching Frequency ($f_{SW,MIN}$)	50.0	kHz
Needed Boost Inductor @Low Line	355.0	μH
Needed Boost Inductor @High Line	284.8	μH
Boost Inductor (L)	**284.8**	μH
Maximum ON Time @$V_{LINE,MIN}$ ($t_{ON,MAX}$)	**10.9**	μs
Maximum OFF Time @$V_{LINE,MIN,PK}$	5.1	μs
Maximum ON time @$V_{LINE,MAX}$	1.3	μs
Maximum OFF Time @$V_{LINE,MAX,PK}$	18.7	μs
Core Selection		
Saturation Flux Density (B_{sat})	0.30	Tesla
Effective Cross-Sectional Area of Selected Core (A_e)	137.0	mm^2
Winding Area of Selected Bobbin (A_W)	110.0	mm^2
Fill Factor	0.25	
Winding Strands	50	
Winding Diameter	0.10	mm
Minimum Number of Turns (N_{BOOST})	**34**	Turns
Air gap Length	**0.7**	mm
Maximum Current Density of Coil ($I_{L,DENSITY}$)	**5.1**	A/mm^2
Necessary Window Area (A_W)	**53.4**	mm^2
	Core size is O.K	

[STEP-3] Inductor Auxiliary Winding Design

Figure 14 shows the application circuit of nearby ZCD pin from auxiliary winding.

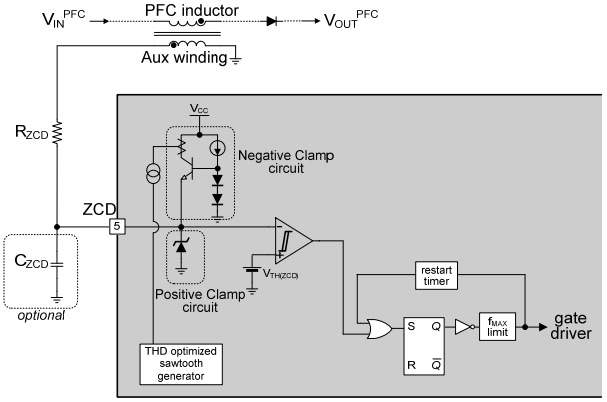


Figure 14. Application Circuit of ZCD Pin

The first role of ZCD winding is detecting the zero-current point of the boost inductor. Once the boost inductor current becomes zero, the effective capacitor shown at the MOSFET drain pin *(C_{eff})* and the boost inductor resonate together. To minimize the constant turn-on time deterioration and turn-on loss, the gate is turned on again when the drain-source voltage of the MOSFET *(V_{DS})* reaches the valley point shown in Figure 15. When input voltage is lower than half of the boosted output voltage, Zero Voltage Switching (ZVS) is possible if MOSFET turn-on is triggered at valley point.

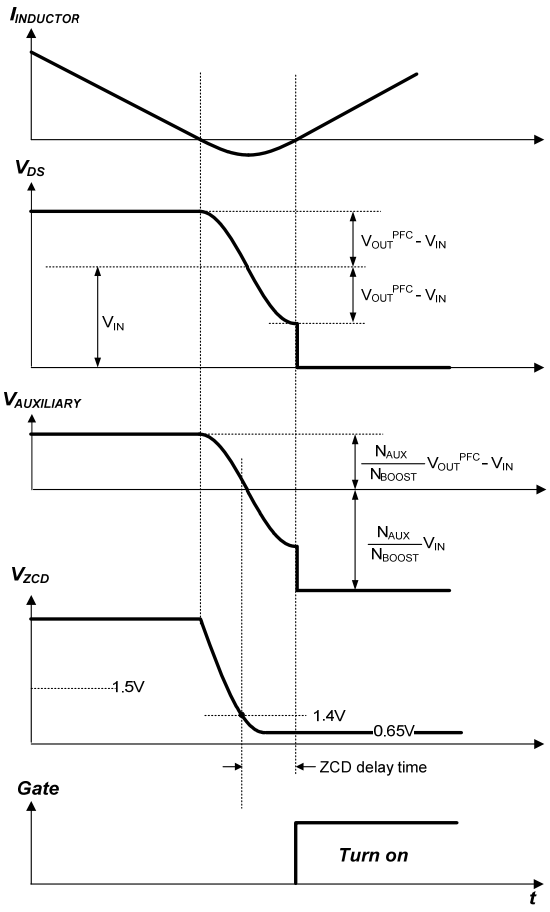


Figure 15. ZCD Detection Waveforms

Auxiliary winding must give enough energy to trigger ZCD threshold to detect zero current. Minimum auxiliary winding turns are given as:

$$N_{AUX} \geq \frac{1.5V \cdot N_{BOOST}}{V_{OUT} - \sqrt{2}V_{LINE,MAX}} \ [Turns] \quad (11)$$

where 1.5V is the positive threshold of the ZCD pin.

To guarantee stable operation, auxiliary winding turns are recommended to add 2~3 turns to the calculation result from Equation (11). However, too many auxiliary winding turns raise the negative clamping loss at high line and positive clamping loss at low line.

(Design Example) 34 turns are selected as boost inductor turns and auxiliary winding turns are calculated as:

$$N_{AUX} \geq \frac{1.5V \cdot N_{BOOST}}{V_{OUT} - \sqrt{2}V_{LINE,MAX}} = \frac{1.5 \cdot 34}{400 - \sqrt{2} \cdot 265} = 2.02[Turns]$$

Choice should be around 4~5 turns after adding 2~3 turns.

3. Inductor Auxiliary Winding Design		
Minimum Aux Winding Turns ($N_{AUX,MIN}$)	3	Turns
User Choice of Aux Winding Turns (N_{AUX})	5	Turns
Winding Diameter	0.10	mm
Maximum Current Density of Coil	1.273	A/mm^2

[STEP-4] ZCD Circuit Design

If a transition time when $V_{AUXILIARY}$ drops from 1.4V to 0V is ignored from Figure 15, the needed additional delay by the external resistor and capacitor is one quarter of the resonant period. The time constant made by ZCD resistor and capacitor should be the same as one quarter of the resonant period:

$$R_{ZCD} \cdot C_{ZCD} = \frac{2\pi\sqrt{C_{eff} \cdot L}}{4} \quad (12)$$

where C_{eff} is the effective capacitor shown at the MOSFET drain pin; C_{ZCD} is the external capacitance at the ZCD pin; and R_{ZCD} is the external resistance at the ZCD pin.

The second role of R_{ZCD} is the current limit of the internal negative clamp circuit when auxiliary voltage drops to negative due to MOSFET turn on. ZCD voltage is clamped 0.65V and minimum R_{ZCD} can be given as:

$$R_{ZCD} \geq \frac{\left(\frac{N_{AUX}}{N_{BOOST}}\sqrt{2}V_{LINE,MAX} - 0.65V\right)}{3mA} \ [\Omega] \quad (13)$$

where 3mA is the clamping capability of the ZCD pin.

The calculated result of Equation (13) is normally higher than 15kΩ. If 20kΩ is assumed as R_{ZCD}, calculated C_{ZCD} from Equation (12) is around 10pF when the other components are assumed as conventional values used in the field. Because most IC pins have several pF parasitic capacitance, C_{ZCD} can be eliminated when R_{ZCD} is higher than 30kΩ. However, a small capacitor would be helpful when auxiliary winding suffers from operating noise.

The PFC control loop has two conflicting goals: output voltage regulation and making the input current shape the same as input voltage. If the control loop reacts to regulate output voltage smoothly, as shown in Figure 16, control voltage varies widely with the input voltage variation. Input current acts to the control loop and sinusoidal input current shape cannot be attained. This is why control response of most PFC topologies is very slow and turn-on time over AC period is kept constant. This is also why output voltage ripple is made by input and output power relationship, not by control-loop performance.

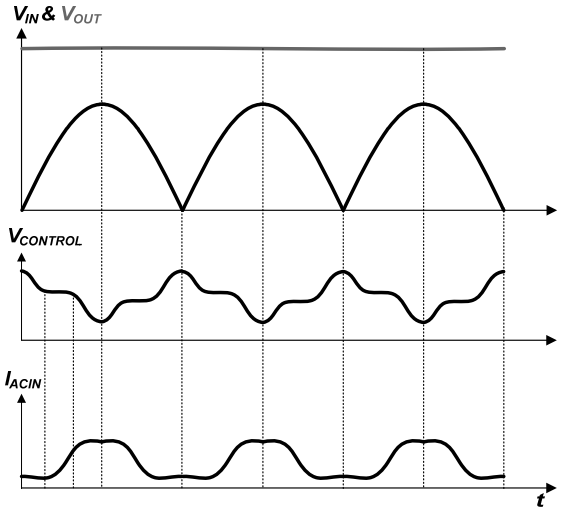


Figure 16. Input Current Deterioration by Fast Control

If on-time is controlled constantly over one AC period, inductor current peak follows the AC input voltage shape and achieves good power factor. Off-time is basically inductor current reset time due to the boundary mode and is determined by the input and output voltage difference. When input voltage is at its peak, the voltage difference between input and output voltage is small and long turn-off time is necessary. When input voltage is near zero, turn-off time is short, as shown in Figure 17 and Figure 18. Though inductor current drops to zero, there is a minor delay, explained above. The delay can be assumed as fixed when AC is at line peak and zero. Near AC line peak, the inductor current decreasing slope is slow and inductor current slope is also slow during the ZCD delay. The amount of negative current is not much higher than the inductor current peak. Near the AC line zero, inductor current decreasing slope is very high and the amount of negative current is higher than positive inductor current peak because input voltage is almost zero.

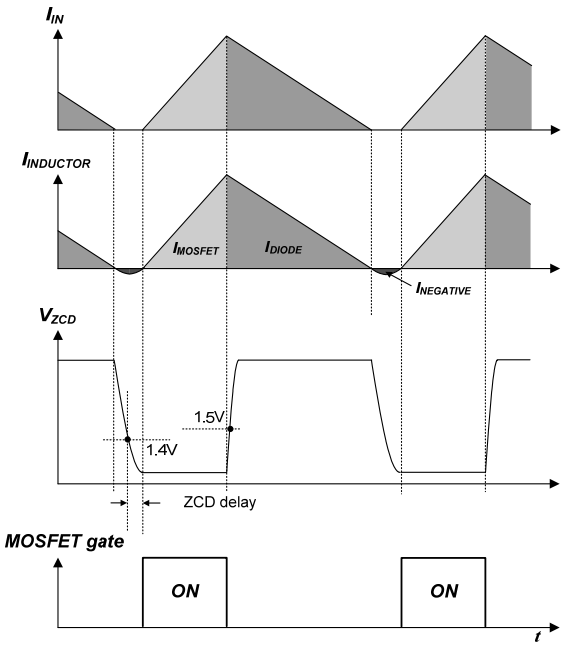


Figure 17. Inductor Current at AC Voltage Peak

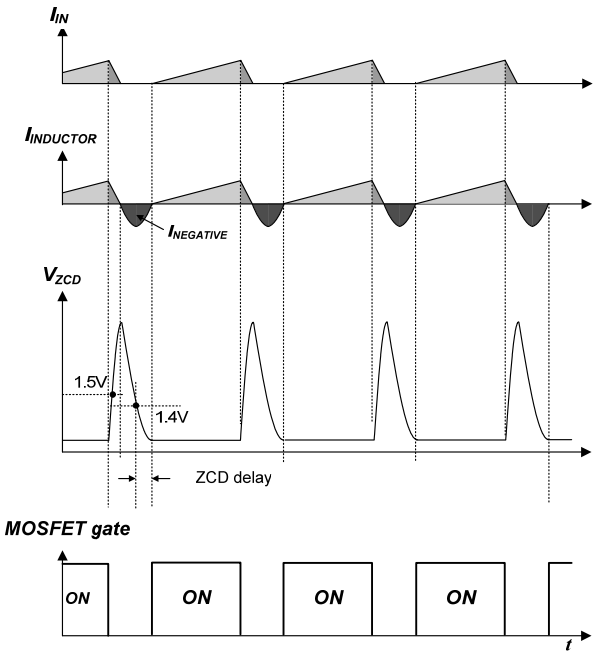


Figure 18. Inductor Current at AC Voltage Zero

Negative inductor current creates zero-current distortion and degrades the power factor. Improve this by extending turn-on time at the AC line input near the zero cross.

Negative auxiliary winding voltage, when MOSFET is turned on, is linearly proportional to the input voltage. Sourcing current generated by the internal negative clamping circuit is also proportional to sinusoidal input voltage. That current is detected internally and added to the internal sawtooth generator, as shown in Figure 19.

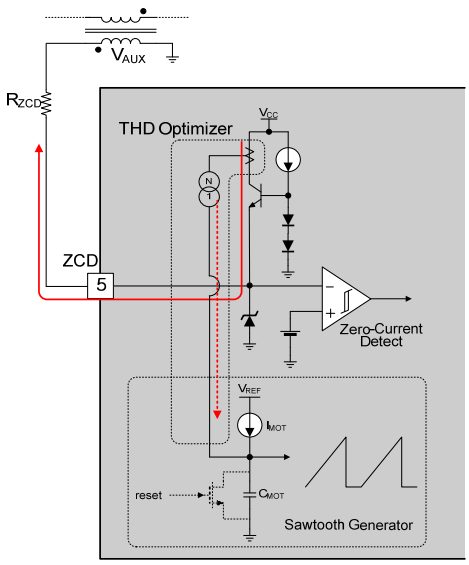


Figure 19. ZCD Current and Sawtooth Generator

When AC input voltage is almost zero, no negative current is generated from inside; but sourcing current, when input voltage is high, is used to raise the sawtooth generator slope and turn-on time is shorter. As a result, turn-on time, when AC voltage is zero, is longer compared to AC voltage, in peaks shown as in Figure 20.

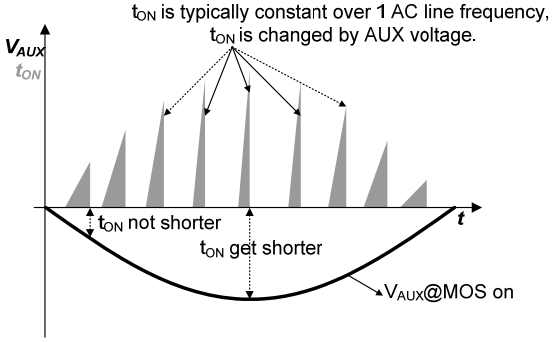


Figure 20. THD Improvement

The current that comes from the ZCD pin, when auxiliary voltage is negative, depends on R_{ZCD}. The second role of R_{ZCD} is related to improving the Total Harmonic Distortion (THD).

The third role of R_{ZCD} is making the maximum turn-on time adjustment. Depending on sourcing current from the ZCD pin, the maximum on-time varies as in Figure 21.

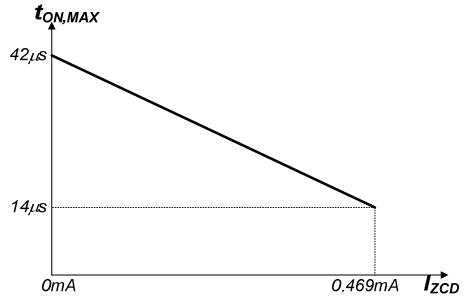


Figure 21. Maximum On-Time Variation vs. I_{ZCD}

With the aid of I_{ZCD}, an internal sawtooth generator slope is changed and turn-on time varies as shown in Figure 22.

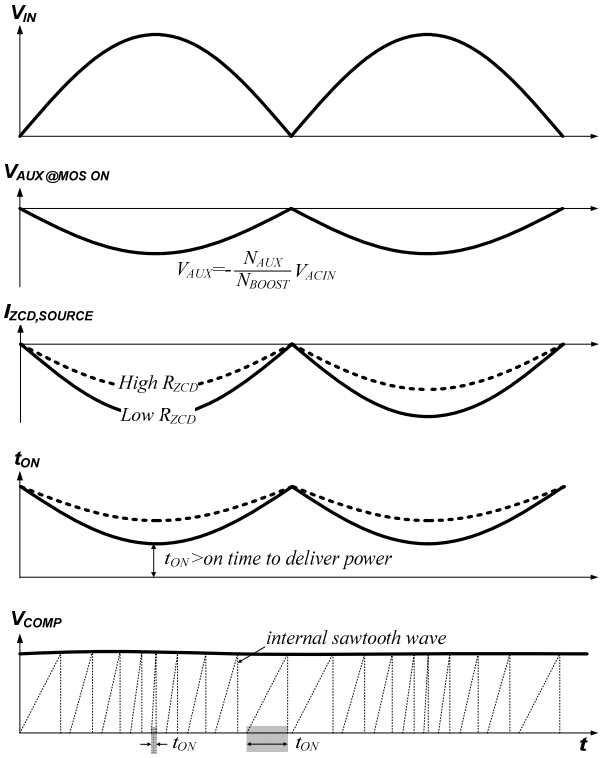


Figure 22. Internal Sawtooth Wave Slope Variation

R_{ZCD} also influences control range. Because FL7930 doesn't detect input voltage, voltage-mode control value is determined by the turn-on time to deliver needed current to boost output voltage. When input voltage increases, control voltage decreases rapidly. For example, if input voltage doubles, control voltage drops to one quarter. Making control voltage maximum when input voltage is low and at full load is necessary to use the whole control range for the rest of the input voltage conditions. Matching maximum turn-on time needed at low line is calculated in Equation (7) and turn-on time adjustment by R_{ZCD} guarantees use of the full control range. R_{ZCD} for control range optimization is obtained as:

$$R_{ZCD} \geq \frac{28\mu s}{t_{ON,MAX1} - t_{ON,MAX}} \cdot \frac{\sqrt{2} \cdot V_{LINE,MIN} \cdot N_{AUX}}{0.469mA \cdot N_{BOOST}} \quad (14)$$

where:
$t_{ON,MAX}$ is calculated by Equation (7);
$t_{ON,MAX1}$ is maximum on-time programming 1;
N_{BOOST} is the winding turns of boost inductor; and
N_{AUX} is the auxiliary winding turns.

R_{ZCD} calculated by Equation (13) is normally lower than the value calculated in Equation (14). To guarantee the needed turn on-time for the boost inductor to deliver rated power, the resulting R_{ZCD} from Equation (13) is normally not suitable. R_{ZCD} should be higher than the result of Equation (14) when output voltage drops as a result of low line voltage.

When input voltage is high and load is light, not much input current is needed and control voltage of V_{COMP} touches switching stop level, such as if FL7930 is 1V. However, in some applications, a PFC block is needed to operate normally at light load. To compensate control

range correctly, input voltage sensing is necessary, such as with Fairchild's interleaved PFC controller FAN9612, or special care on sawtooth generator is necessary. Without it, optimizing R_{ZCD} is only slightly helpful for control range. This is explained and depicted in the associated Excel® design tool "COMP Range" worksheet. To guarantee enough control range at high line, clamping output voltage lower than rated output on the minimum input condition can help.

(Design Example) Minimum R_{ZCD} for clamping capability is calculated as:

$$R_{ZCD} \geq \frac{\left(\frac{N_{AUX}}{N_{BOOST}}\sqrt{2}V_{LINE,MAX} - 0.65V\right)}{3mA}$$

$$= \frac{\left(\frac{5}{34}\sqrt{2}\cdot 265 - 0.65V\right)}{3mA} = 18.2k\Omega$$

Minimum R_{ZCD} for control range is calculated as:

$$R_{ZCD} \geq \frac{28\mu s}{t_{ON,MAX1} - t_{ON,MAX}} \cdot \frac{\sqrt{2}\cdot V_{LINE,MIN}\cdot N_{AUX}}{0.469mA \cdot N_{BOOST}}$$

$$= \frac{28\mu s}{42\mu s - 10.9\mu s} \cdot \frac{\sqrt{2}\cdot 90\cdot 5}{0.469mA\cdot 34} = 37.2k\Omega$$

A choice close to the value calculated by the control range is recommended. 39kΩ is chosen in this case.

4. ZCD Circuit Design		
Minimum Value for R_{ZCD} for THD Improvement	18.2	kΩ
Minimum Value for R_{ZCD} for Control Range	37.2	kΩ
User Choice of R_{ZCD}	39.0	kΩ
R_{ZCD} is also related with COMP (control voltage) range.		
Please refer to the "COMP range" worksheet to select R_{ZCD} optimally.		

[STEP-5] Output Capacitor Selection

The output voltage ripple should be considered when selecting the output capacitor. Figure 23 shows the line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

$$C_{OUT} \geq \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot \Delta V_{OUT,RIPPLE}} [F] \quad (15)$$

where $V_{OUT,RIPPLE}$ is the peak-to-peak output voltage ripple specification.

The output voltage ripple caused by ESR of electrolytic capacitor is not as serious as other power converters because output voltage is high and load current is small. Since too much ripple on the output voltage may cause premature OVP during normal operation, the peak-to-peak ripple specification should be smaller than 15% of the nominal output voltage.

The hold-up time should also be considered when determining the output capacitor as:

$$C_{OUT} \geq \frac{2\cdot P_{OUT}\cdot t_{HOLD}}{(V_{OUT} - 0.5\cdot \Delta V_{OUT,RIPPLE})^2 - V_{OUT,MIN}^2} [f] \quad (16)$$

where t_{HOLD} is the required hold-up time and $V_{OUT,MIN}$ is the minimum output voltage during hold-up time.

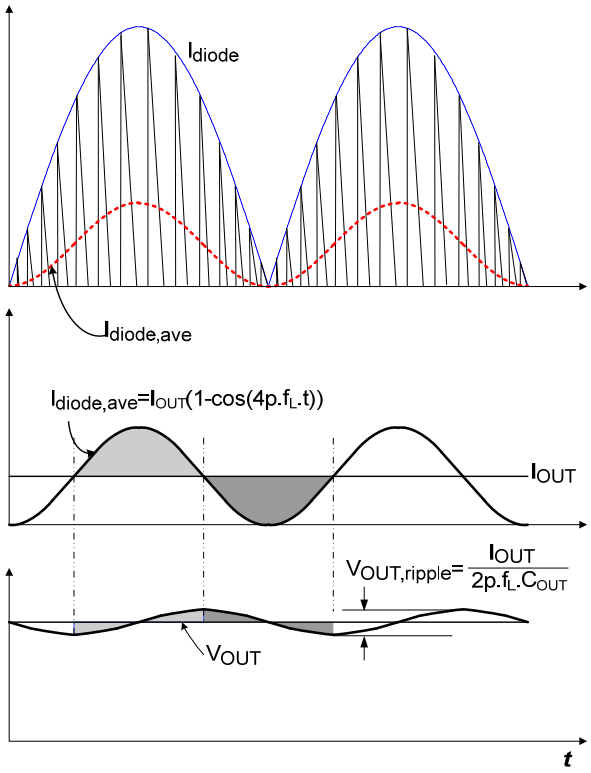


Figure 23. Output Voltage Ripple

The voltage rating of capacitor can be obtained as:

$$V_{ST,COUT} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT}[V] \quad (17)$$

where $V_{OVP,MAX}$ and V_{REF} are the maximum tolerance specifications of over-voltage protection triggering voltage and reference voltage at error amplifier.

(Design Example) With the ripple specification of $8V_{p-p}$, the capacitor should be:

$$C_O \geq \frac{I_{OUT}}{2\pi \cdot f_{LINE}\cdot \Delta V_{OUT,ripple}} = \frac{0.35}{2\pi\cdot 50\cdot 8} = 139.3[\mu F]$$

Since minimum allowable output voltage during one cycle line (20ms) drop-outs is 330V, the capacitor should be:

$$C_O \geq \frac{2\times P_{OUT}\cdot t_{HOLD}}{(V_{OUT} - 0.5\cdot \Delta V_{OUT,ripple})^2 - V_{OUT,MIN}^2}$$

$$= \frac{2\cdot 140\cdot 20\times 10^{-3}}{(400 - 0.5\cdot 8)^2 - 330^2} = 116.9[\mu F]$$

To meet both conditions, the output capacitor must be larger than 140μF. A 240μF capacitor is selected for the output capacitor.

The voltage stress of selected capacitor is calculated as:

$$V_{ST,COUT} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT} = \frac{2.730}{2.500}\cdot 400 = 436.8[V]$$

4. Output Capacitor Selection		
Maximum Allowable Output Voltage Ripple	8.0	V
Minimum Out Capacitance	139.3	µF
Needed Holdup Time	20.0	ms
Minimum Allowable Operating Voltage During Holdup	330.0	V
Minimum Output Capacitance Considering Holdup Tim	116.9	µF
To meet both minimum conditions, select bigger one. Otherwise select proper one to meet system spec.		
Maximum Voltage Stress	436.8	V
Recommended Output Capacitance	139.3	µF
User Choice of Output Capacitance	240.0	µF

[STEP-6] MOSFET and Diode Selection

Selecting the MOSFET and diode needs extensive knowledge and calculation regarding loss mechanisms and gets more complicated if proper selection of a heatsink is added. Sometimes the loss calculation itself is based on assumptions that may be far from reality. Refer to industry resources regarding these topics. This note shows the voltage rating and switching loss calculations based on the linear approximation.

The voltage stress of the MOSFET is obtained as:

$$V_{ST,Q} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT} + V_{DROP,DOUT} \ [V] \quad (18)$$

where $V_{DROP,DOUT}$ is the maximum forward-voltage drop of output diode.

After the MOSFET is turned off, the output diode turns on and a large output electrolytic capacitor is shown at the drain pin. Thus a drain voltage clamping circuit that is necessary on other topologies is not necessary in PFC. During the turn-off transient, boost inductor current changes the path from MOSFET to output diode and before the output diode turns on; a minor voltage peak can be shown at drain pin, which is proportional to MOSFET turn-off speed.

MOSFET loss can be divided into three parts: conduction loss, turn-off loss, and discharge loss. Boundary Mode guarantees Zero Current Switching (ZCS) of MOSFET when turned on, so turn-on loss is negligible.

The MOSFET RMS current and conduction loss are obtained as:

$$I_{Q,RMS} = I_{L,PK} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot V_{LINE}}{9\pi \cdot V_{OUT}}} \ [A] \quad (19)$$

$$P_{Q,CON} = \left(I_{Q,RMS}\right)^2 \cdot R_{DS,ON} \ [W] \quad (20)$$

where $I_{Q,RMS}$ is the RMS value of MOSFET current, $P_{Q,CON}$ is the conduction loss caused by MOSFET current, and $R_{DS,ON}$ is the on resistance of the MOSFET.

On resistance, described as “static on resistance,” varies with junction temperature. That variation information is normally supplied in the datasheet by manufacturer. When calculating conduction loss, generally multiply three with the $R_{DS,ON}$ for more accurate estimation.

The precise turn-off loss calculation is difficult because of the nonlinear characteristics of MOSFET turn off. When piecewise linear current and voltage of MOSFET during turn-off and inductive load are assumed, MOSFET turn-off loss is obtained as:

$$P_{Q,SWOFF} = \frac{1}{2} \cdot V_{OUT} \cdot I_L \cdot t_{OFF} \cdot f_{SW} \ [W] \quad (21)$$

where t_{OFF} is the turn-off time and f_{SW} is the switching frequency.

Boundary Mode PFC inductor current and switching frequency vary at every switching moment. RMS inductor current and average switching frequency over one AC period can be used instead of instantaneous values.

Individual loss portions are changed according to the input voltage; maximum conduction loss appears at low line because of high input current; and maximum switching off loss appears at high line because of the high switching frequency. Thus, resulting loss is always lower than the summation of the two losses calculated above.

Capacitive discharge loss made by effective capacitance shown at drain and source, which includes MOSFET C_{OSS} (an externally added capacitor to reduce dv/dt and parasitic capacitors shown at drain pin) is also dissipated at MOSFET. That loss is calculated as:

$$P_{Q,DISCHG} = \frac{1}{2}\left(C_{OSS} + C_{EXT} + C_{PAR}\right) \cdot V_{OUT}^2 \cdot f_{SW} \ [W] \quad (22)$$

where:
C_{OSS} is the output capacitance of MOSFET;
C_{EXT} is an externally added capacitor at drain and source of MOSFET; and
C_{PAR} is the parasitic capacitance shown at drain pin.

Because the C_{OSS} is a function of the drain and source voltage, it is necessary to refer to graph data showing the relationship between C_{OSS} and voltage.

Estimate the total power dissipation of MOSFET as the sum of three losses:

$$P_Q = P_{Q,CON} + P_{Q,SWOFF} + P_{Q,DISCHG} \ [W] \quad (23)$$

Diode voltage stress is the same as the output capacitor stress calculated in Equation (17).

The average diode current and power loss are obtained as:

$$I_{DOUT,AVE} = \frac{I_{OUT}}{\eta} \ [A] \quad (24)$$

$$P_{DOUT} = V_{DROP,DOUT} \cdot I_{DOUT,AVE} \ [W] \quad (25)$$

where $V_{DROP,DOUT}$ is the forward voltage drop of diode.

(Design Example) Internal reference at the feedback pin is 2.5V and maximum tolerance of OVP trigger voltage is 2.73V. If Fairchild's FDPF12N60NZ MOSFET and FFPF08H60S diode are selected, $V_{D,FOR}$ is 2.1V at 8A, 25°C, maximum $R_{DS,ON}$ is 0.53Ω at drain current 6A, and maximum C_{OSS} is 150pF at drain-source voltage 480V.

$$V_{ST,Q} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT} + V_{DROP,DIODE}$$

$$= \frac{2.73}{2.50} \cdot 400 + 2.1 = 438.9 \ [V]$$

$$P_{Q,CON} = \left(I_{L,PK} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot V_{LINE}}{9\pi \cdot V_{OUT}}} \right)^2 \cdot \left(R_{DS,ON} \right)$$

$$= \left(4.889 \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot 90}{9\pi \cdot 400}} \right)^2 \cdot (0.53 \times 3) = 4.62[W]$$

$$P_{Q,SWOFF} = \frac{1}{2} \cdot V_{OUT} \cdot I_L \cdot t_{OFF} \cdot f_{SW}$$

$$= \frac{1}{2} \cdot 400 \cdot 1.782 \cdot 50ns \cdot (50k / 0.8) = 1.08[W]$$

$$P_{Q,DISCHG} = \frac{1}{2} \cdot (C_{OSS} + C_{EXT} + C_{PAR}) \cdot V_{OUT}^2 \cdot f_{SW}$$

$$= \frac{1}{2} \cdot 150p \cdot 400^2 \cdot (50k / 0.8) = 0.75 \ [W]$$

Diode average current and forward-voltage drop loss as:

$$I_{DOUT,AVE} = \frac{I_{OUT}}{\eta} = \frac{0.35}{0.9} = 0.39[A]$$

$$P_{DOUT,LOSS} = V_{DOUT,FOR} \cdot I_{DOUT,AVE} = 2.1 \cdot 0.39 = 1.02[W]$$

6. Power MOSFET Sselection		
Reference Voltage for Feedback	2.50	V
Maximum OVP Level Considering Tolerance	2.73	V
Maximum Voltage Stress on MOSFET	**438.90**	V
Maximum RMS Current on MOSFET	**1.705**	A
$R_{DS(ON)}$ of Selected MOSFET	0.53	Ω
C_{OSS} of Selected MOSFET	150.0	pF
Maximum Conduction Loss	**4.62**	W
MOSFET Turn Off Loss	**1.08**	W
Discharge Loss	**0.75**	W
Total MOSFET Loss	**6.45**	W

7. Output Diode Selection		
Maximum Reverse Voltage Stress	**436.80**	V
Average Current of Output Diode	**0.39**	A
Forward Voltage Drop of Selected Diode	2.1	V
Estimated Diode Loss	**1.02**	W

[STEP-8] Determine Current-Sense Resistor

It is typical to set pulse-by-pulse current limit level a little higher than the maximum inductor current calculated by Equation (3). For 10% margin, the current-sensing resistor is selected as:

$$R_{CS} = \frac{V_{CS,LIM}}{I_{L,PK} \cdot 1.1} \ [\Omega] \quad (26)$$

Once resistance is calculated, its power loss at low line is calculated as:

$$P_{RCS} = I_{Q,RMS}^2 \cdot R_{CS} \ [W] \quad (27)$$

Power rating of the sensing resistor is recommended a twice the power rating calculated in Equation (27).

(Design Example) Maximum inductor current is 4.889A and sensing resistor is calculated as:

$$R_{CS} = \frac{V_{CS,LIM}}{I_{ind}^{pk} \cdot 1.1} = \frac{0.8}{4.889 \cdot 1.1} = 0.149[\Omega]$$

Choosing 0.1Ω as R_{CS}, power loss is calculated as:

$$P_{RCS,LOSS} = I_{Q,RMS}^2 \cdot R_{CS} = 1.705^2 \cdot 0.1 = 0.29[W]$$

Recommended power rating of sensing resistor is 0.58W.

8. Determine Current Sensing Resistor		
Current Sense Input Threshold Voltage Limit	0.80	V
Maximum Value for R_{CS}	**0.149**	Ω
User Choice of R_{CS}	0.100	Ω
Maximum Power Loss at R_{CS}	**0.29**	W
Recommended Power Rating for R_{CS}	**0.58**	W

[STEP-9] Design Compensation Network

The boost PFC power stage can be modeled as shown in Figure 24. MOSFET and diode can be changed to loss-free resistor model and then be modeled as a voltage-controlled current source supplying RC network.

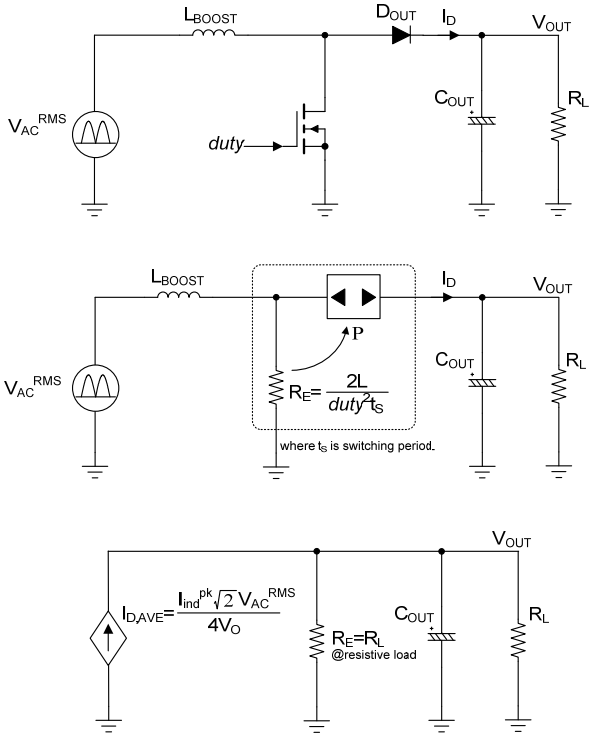


Figure 24. Small Signal Modeling of the Power Stage

By averaging the diode current during the half line cycle, the low-frequency behavior of the voltage controlled current source of Figure 24 is obtained as:

$$I_{DOUT,AVE} = K_{SAW} \cdot \frac{\sqrt{2}V_{LINE}}{4V_{OUT}} \cdot \frac{\sqrt{2}V_{LINE}}{L} \ [A] \quad (28)$$

where:
L is the boost inductance,
V_{OUT} is the output voltage; and
K_{SAW} is the internal gain of sawtooth generator (that of FL7930 is 8.496×10^{-6}).

Then the low-frequency, small-signal, control-to-output transfer function is obtained as:

$$\frac{\hat{v}_{OUT}}{\hat{v}_{COMP}} = K_{SAW} \cdot \frac{(V_{LINE})^2 R_L}{4V_{OUT} \cdot L} \cdot \frac{1}{1+\frac{s}{2\pi f_p}} \quad (29)$$

where $f_p = \frac{2}{2\pi \cdot R_L C_{OUT}}$ and R_L is the output load resistance in a given load condition.

Figure 25 and Figure 26 show the variation of the control-to-output transfer function for different input voltages and different loads. Since DC gain and crossover frequency increase as input voltage increases and DC gain increases as load decreases, high input voltage and light load is the worst condition for feedback loop design.

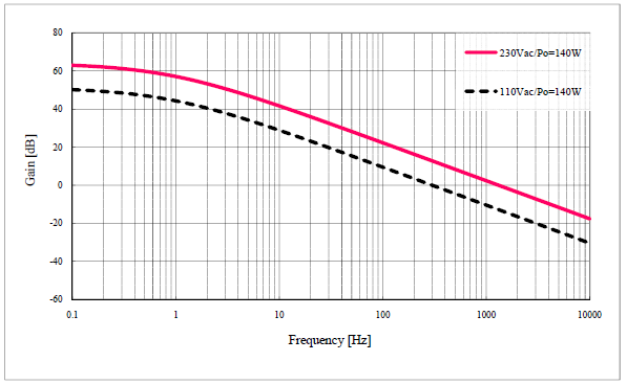


Figure 25. Control-to-Output Transfer Function for Different Input Voltages

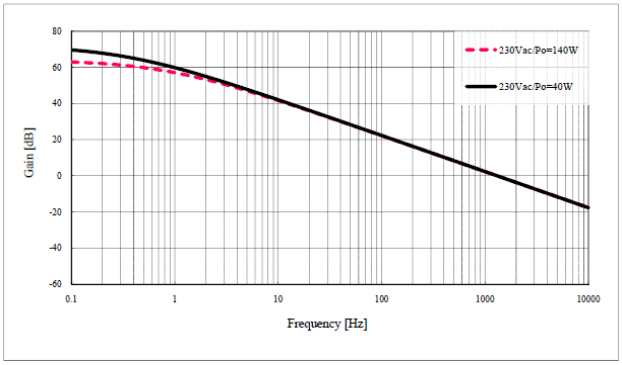


Figure 26. Control-to-Output Transfer Function for Different Loads

Proportional and Integration (PI) control with a high-frequency pole is typically used for compensation, as shown in Figure 27. The compensation zero (f_{CZ}) introduces phase boost, while the high-frequency compensation pole (f_{CP}) attenuates the switching ripple.

The transfer function of the compensation network is obtained as:

$$\frac{\hat{v}_{COMP}}{\hat{v}_{OUT}} = \frac{2\pi f_I}{s} \cdot \frac{1+\frac{s}{2\pi f_{CZ}}}{1+\frac{s}{2\pi f_{CP}}}$$

$$f_I = \frac{2.5}{V_{OUT}} \cdot \frac{115\mu mho}{2\pi \cdot (C_{COMP,LF} + C_{COMP,HF})} \quad (30)$$

where $f_{CZ} = \frac{1}{2\pi \cdot R_{COMP} \cdot C_{COMP,LF}}$

$$f_{CP} = \frac{1}{2\pi \cdot R_{COMP} \cdot \left(\frac{C_{COMP,LF} \cdot C_{COMP,HF}}{C_{COMP,LF} + C_{COMP,HF}}\right)}$$

If $C_{COMP,LF}$ is much larger than $C_{COMP,HF}$, f_I and f_{CP} can be simplified as:

$$f_I \cong \frac{2.5}{V_{OUT}} \cdot \frac{115\mu mho}{2\pi \cdot C_{COMP,LF}} \ [Hz]$$

$$f_{CP} \cong \frac{1}{2\pi \cdot R_{COMP} \cdot C_{COMP,HF}} \ [Hz] \quad (31)$$

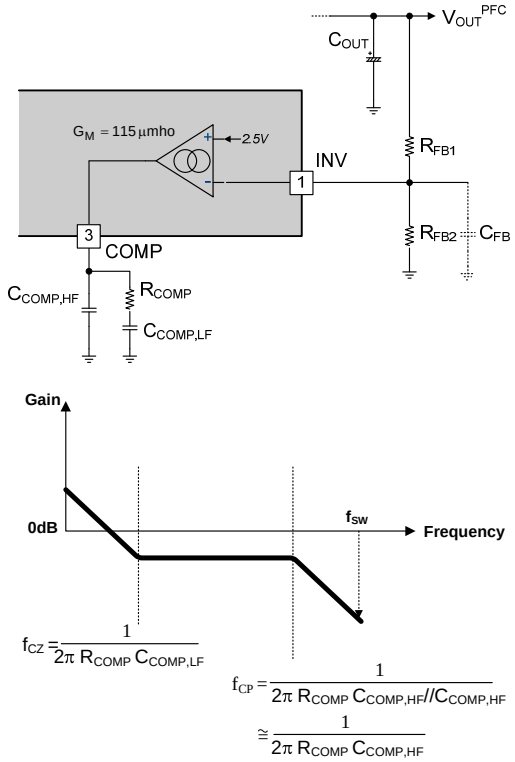


Figure 27. Compensation Network

The feedback resistor is chosen to scale down the output voltage to meet the internal reference voltage:

$$\frac{R_{FB1}}{R_{FB1}+R_{FB2}} \cdot V_{OUT} = 2.5V \quad (32)$$

Typically, high R_{FB1} is used to reduce power consumption and, at the same time, C_{FB} can be added to raise the noise immunity. The maximum C_{FB} currently used is several nano farads. Adding a capacitor at the feedback loop introduces a pole as:

$$f_{FP} = \frac{1}{2\pi \cdot (R_{FB1} // R_{FB2}) \cdot C_{FB}} \cong \frac{1}{2\pi \cdot R_{FB2} \cdot C_{FB}} \ [Hz] \quad (33)$$

where $(R_{FB1} // R_{FB2}) = \frac{R_{FB1} \cdot R_{FB2}}{R_{FB1} + R_{FB2}}$

Though R_{FB1} is high, pole frequency made by the synthesized total resistance and several nano farads is several kilo hertz and rarely affects control-loop response.

The procedure to design the feedback loop is:

a. Determine the crossover frequency (f_C) around 1/10~1/5 of line frequency. Since the control-to-output transfer function of the power stage has -20dB/dec slope and -90° phase at the crossover frequency, as shown in Figure 28; place the zero of the compensation network (f_{CZ}) around the crossover frequency so 45° phase margin is obtained.

The capacitor $C_{COMP,LF}$ is determined as:

$$C_{COMP,\,LF} \cong \frac{K_{SAW}(V_{LINE})^2 2.5 \cdot 115\mu mho}{2 \cdot V_{OUT}^{\ 2} \cdot L \cdot C_{OUT}(2\pi f_C)^2} [f] \quad (34)$$

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

$$R_{COMP} = \frac{1}{2\pi \cdot f_C \cdot C_{COMP,LF}} \ [\Omega] \quad (35)$$

b. Place this compensator high-frequency pole (f_{CP}) at least a decade higher than f_C to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter for noise to be effectively attenuated. The capacitor $C_{COMP,HF}$ is determined as:

$$C_{COMP,HF} = \frac{1}{2\pi \cdot f_{CP} \cdot R_{COMP}} \ [\Omega] \quad (36)$$

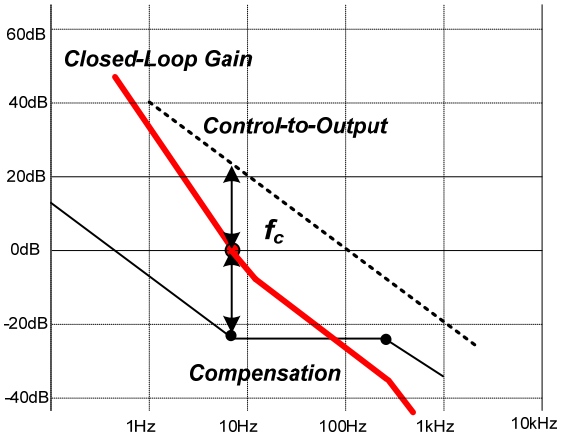


Figure 28. Compensation Network Design

(Design Example) If R_{FB1} is 11.7MΩ, then R_{FB2} is:

$$R_{FB2} = \frac{2.5V}{V_{OUT} - 2.5V} R_{FB1} = \frac{2.5}{400 - 2.5} 11.7 \times 10^6 = 73.58k\Omega$$

Choosing the crossover frequency (control bandwidth) at 15Hz, $C_{COMP,LF}$ is obtained as:

$$C_{COMP,\,LF} \cong \frac{K_{SAW}\,(V_{LINE})^2\, 2.5 \cdot 115\mu mho}{2 \cdot V_{OUT}{}^2 \cdot L \cdot C_{OUT}\,(2\pi\, f_C)^2}$$

$$= \frac{8.496 \times 10^{-6}(230)^2\, 2.5 \cdot 115 \times 10^{-6}}{2 \cdot 400^2 \cdot 280 \times 10^{-6} \cdot 240 \times 10^{-6}(2\pi 15)^2} = 665nF$$

Actual $C_{COMP,LF}$ is determined as 1000nF since it is the closest value among the off-the-shelf capacitors. R_{COMP} is obtained as:

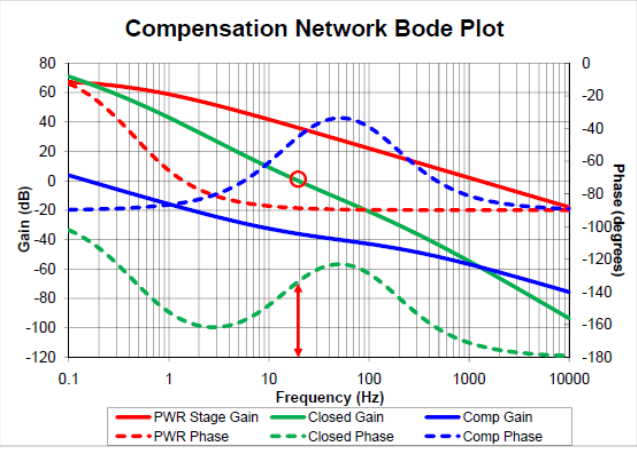
$$R_{COMP} = \frac{1}{2\pi \cdot f_C \cdot C_{COMP,LF}} = \frac{1}{2\pi \cdot 15 \cdot 665 \times 10^{-9}} = 15.95k\Omega$$

Selecting the high-frequency pole as 150Hz, $C_{COMP,HF}$ is obtained as:

$$C_{COMP,HF} = \frac{1}{2\pi \cdot f_{CP} \cdot R_{COMP}} = \frac{1}{2\pi \cdot 150 \cdot 15.95 \times 10^3} = 66.5nF$$

These components result in a control loop with a bandwidth of 19.7Hz and phase margin of 46°. The actual bandwidth is a little larger than the asymptotic design.

9. Design Compensation Network				
Select R_{FB1}			11.7	MΩ
R_{FB2}			73.58	kΩ
Power Loss at Output Sensing Resistors			13.59	mW
Transconductance of Error Amp			115.0	μmho
User Choice of Crossover Frequency			15	Hz
Asymptotic Value for $C_{COMP,LF}$			665.09	nF
Asymptotic Value for R_{COMP}			15.95	kΩ
Asymptotic Value for $C_{COMP,HF}$			66.51	nF
User Choice for $C_{COMP,LF}$			680.00	nF
User Cchoice for R_{COMP}			15.00	kΩ
User Choice for $C_{COMP,HF}$			68.00	nF



[STEP-10] Line Filter Capacitor Selection

It is typical to use small bypass capacitors across the bridge rectifier output stage to filter the switching current ripple, as shown in Figure 29. Since the impedance of the line filter inductor at line frequency is negligible compared to the impedance of the capacitors, the line frequency behavior of the line filter stage can be modeled, as shown in Figure 29. Even though the bypass capacitors absorb switching ripple current, they also generate circulating capacitor current, which leads the line voltage by 90°, as shown in Figure 30. The circulating current through the capacitor is added to the load current and generates displacement between line voltage and current.

The displacement angle is given by:

$$\theta = tan^{-1}\left(\frac{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE} \cdot C_{EQ}}{P_{OUT}}\right) \quad (37)$$

where C_{EQ} is the equivalent capacitance that appears across the AC line ($C_{EQ}=C_{F1}+C_{F2}+C_{HF}$).

The resultant displacement factor is:

$$DF = cos(\theta) \quad (38)$$

Since the displacement factor is related to power factor, the capacitors in the line filter stage should be selected carefully. With a given minimum displacement factor (DF_{MIN}) at full-load condition, the allowable effective input capacitance is obtained as:

$$C_{EA} < \frac{P_{OUT}}{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE}} \cdot tan\left(cos^{-1}(DF_{MN})\right)\,[F] \quad (39)$$

One way to determine if the input capacitor is too high or PFC control routine has problems is to check Power Factor (PF) and Total Harmonic Distortion (THD). PF is the degree to which input energy is effectively transferred to the load by the multiplication of displacement factor. THD is input current shape deterioration ratio. PFC control loop rarely has no relation to displacement factor and input capacitor rarely has no impact on the input current shape. If PF is low (high is preferable), but THD is quite good (low is preferable), it can be concluded that input capacitance is too high and PFC controller is fine.

(Design Example) Assuming the minimum displacement factor at full load is 0.98, the equivalent input capacitance is obtained as:

$$C_{EA} < \frac{P_{OUT}}{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE}} \cdot \tan\left(\cos^{-1}(DF_{MN})\right)$$

$$< \frac{140}{0.9 \cdot (264)^2 \cdot 2\pi \cdot 50} \cdot \tan\left(\cos^{-1}(0.96)\right) = 2.0565\mu F$$

Thus, the sum of the capacitors on the input side should be smaller than 2.0μF.

10. Line Filter Capacitor Selection			
Input Displacement Factor		0.960	
Maximum Input Capacitance ($C_{F1}+C_{F2}+C_{HF}$)		2.0565	μF

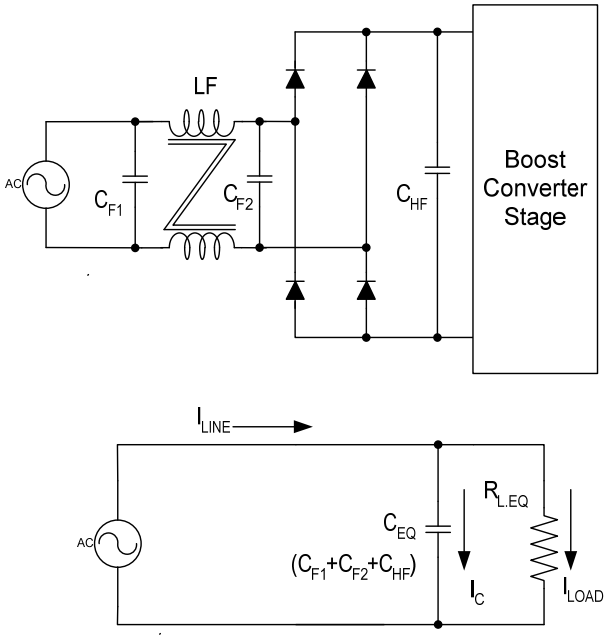


Figure 29. Equivalent Circuit of Line Filter Stage

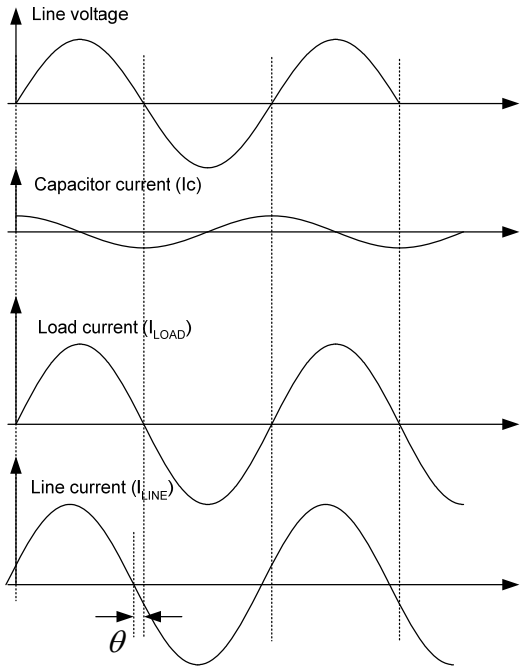


Figure 30. Line Current Displacement

Appendix 1: Use of the RDY Pin for FL7930C

Typically, boosted output voltage from the PFC block is used as input voltage to the DC-DC conversion block. For some types of DC-DC converter, it is recommended to trigger operation after the input voltage rises to some level. For example, LLC resonant converter or forward converter's input voltage is limited to some range to enhance performance or guarantee the stable operation.

The FL7930C provides a PFC-ready pin that can be used to trigger other power stage when PFC output voltage reaches the proper level. For that purpose, the PFC RDY pin is assigned and can be used as a acknowledge signal for the DC-DC conversion stages. When PFC output voltage rises higher than the internal threshold, PFC RDY output is pulled HIGH by the external pull-up voltage and drops to zero with hysteresis.

$$V_{OUT,RDYH} = \frac{2.240V}{2.500V} V_{OUT} \ [V]$$
$$V_{OUT,RDYL} = \frac{1.640V}{2.500V} V_{OUT} \ [V] \quad (40)$$

where $V_{OUT,RDYH}$ is the V_{OUT} voltage to trigger PFC RDY output to pull HIGH and $V_{OUT,RDYL}$ is the V_{OUT} voltage to trigger PFC ready output to drop to zero.

If rated V_{OUT} is $400V_{DC}$, then $V_{OUT,RDYH}$ is $358V_{DC}$, and $V_{OUT,RDYL}$ is $262V_{DC}$.

When LLC resonant converter is assumed to connect at the PFC output, the RDY pin can control the V_{CC} for the LLC controller, as shown in Figure 31.

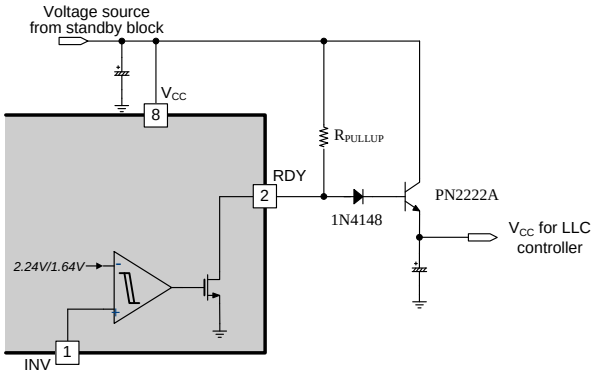


Figure 31. RDY Application Circuit for V_{CC} Driving

R_{PULLUP} is chosen based on the current capability of internal open-drain MOSFET and can be obtained as:

$$R_{PULLUP} \geq \frac{V_{PULLUP} - V_{RDY,SAT}}{I_{RDY,SK}} \ [\Omega] \quad (41)$$

where V_{PULLUP} is the pull-up voltage, $V_{RDY,SAT}$ is the saturation voltage of the internal MOSFET, and $I_{RDY,SK}$ is the allowable sink current for the internal MOSFET.

A fast diode, such as 1N4148, is needed to prohibit the emitter-base breakdown. Without that diode, when RDY voltage drops to $V_{RDY,SAT}$ after being pulled up, emitter voltage maintains operating voltage for LLC controller and almost all the voltage is applied to the emitter and base. Breakdown current flows from emitter, base, and drain of the MOSFET to the source of MOSFET. Because a large electrolytic capacitor is typically used at the V_{CC} supply, that breakdown current flows high for a long time. In this case, the internal MOSFET may be damaged since the external small-signal bipolar junction transistor current capability is higher than the internal RDY MOSFET.

Once circuit configuration is settled, voltage after subtracting forward-voltage drop of the diode and voltage drop (by the multiplication of base current and R_{PULLUP}) from the V_{CC} of FL7930C is available for the LLC controller's V_{CC} source.

Another example is using RDY when the secondary side needs PFC voltage information. When a Cold Cathode Fluorescent Lamp (CCFL) is used for the backlight source of an LCD TV, the inverter stage to ignite CCFL can receive PFC output voltage directly. For that application, Figure 32 can be a suitable circuit configuration.

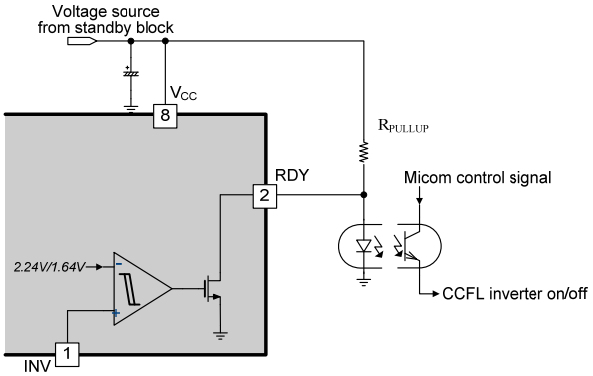


Figure 32. RDY Application Circuit Using Opto-Coupler

With this application circuit, the minimum R_{PULLUP} is given by Equation (42) and the maximum R_{PULLUP} is limited by sufficient current to guarantee stable operation of the opto-coupler. Assuming 1mA is the typical quantity to drive opto-coupler, the maximum R_{PULLUP} is:

$$R_{PULLUP} \leq \frac{V_{PULLUP} - V_{OPTOF}}{1mA} \ [\Omega] \quad (42)$$

where $V_{OPTO,R}$ is the input forward-voltage drop of the opto-coupler.

It may possible that a secondary microcontroller has authority to give a trigger signal to the CCFL inverter controller; however, after combining the microcontroller signal and RDY signal from the primary-side, the inverter stage is triggered only when the two signals meet the requirements at the same time.

Appendix 2: Gate Driver Design

FL7930 directly drives the gate of the MOSFET and various combinations of gate driver circuits are possible. Figure 33 and Figure 31 show the three circuits that are widely used.

When only one resistor is used, the turn-on and turn-off paths follow the same routine and turn-on and turn-off speed cannot be changed simultaneously. To accommodate this, make different paths by two resistors and diodes if possible. Turn-off current flows through the diode first, instead of R_{ON}, and then R_{ON} and R_{OFF} show together. Accordingly, faster turn-off is possible. However, a turn-off path using the internal gate driver's sinking path and current is limited by sinking current capability. If a PNP transistor is added between the gate and source of the MOSFET, the gate is shorted to source locally without sharing the current path to the gate driver. This makes the gate discharge to the much smaller path than that made by the controller. The possibility of ground bounce is reduced and power dissipation in the gate driver is reduced. Due to new high-speed MOSFET types such as SupreMOS® or SuperFET™, gate speed is getting fast. This decreases the switching loss of the MOSFET. At the same time, power systems suffer from the EMI deterioration or noise problems, like gate oscillation. Therefore, sometimes a gate discharge circuit is inevitable to use high-speed characteristics fully.

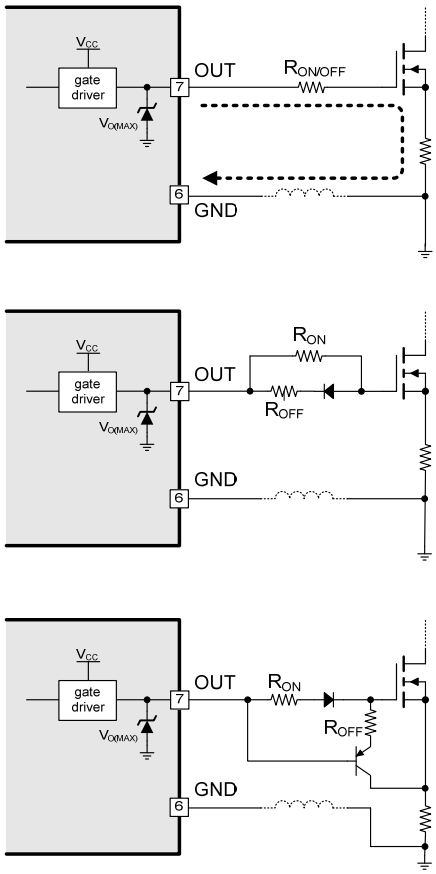


Figure 33. Equivalent Circuit of Line Filter Stage

The most difficult and uncertain task in direct gate drive is optimizing circuit layout. Gate driving path from the OUT pin, resistor, MOSFET gate, and MOSFET source to the GND pin should be as short as possible to reduce parasitic inductance; which may make MOSFET on/off speed slow or introduce unwanted gate oscillation. Using a wider PCB pattern for this lane reduces parasitic inductance. To damp unwanted gate oscillation made by the capacitance at the gate pin and parasitic inductance formed by MOSFET internal bonding wire and PCB pattern, proper resistance can match the impedance at the resonant frequency. To meet EMI regulations or for the redundant system, fast gate speed can be sacrificed by increasing serial resistance between the gate driver and gate.

An optimal gate driver circuit needs intensive knowledge of MOSFET turn-on/off characteristics and consideration of the other critical performance requirements of the system. This is beyond the scope of this paper, but many reference papers can be found in the industry literature.

Appendix 3: Experimental Verification

To show the validity of the design procedure presented in this application note, the converter of the design example was built and tested. All the circuit components are exactly as designed in the example.

Figure 34 and Figure 35 show the inductor current and input current for $115V_{AC}$ and $230V_{AC}$ conditions. Figure 35 shows the startup performance for $95V_{AC}$ full-load condition. Figure 37 (a) and (b) show the PFC output voltage changed under about 35V when AC input voltage was step changed from 115V to 235V and from 235V to 115V at full load. Figure 38 (a) and (b) show the PFC output voltage changed about 32V when output load was step changed from no-load to full-load condition and from full-load to no-load at 235V. The power factor at full load is 0.988 and 0.93 for $110V_{AC}$ and $230V_{AC}$, respectively.

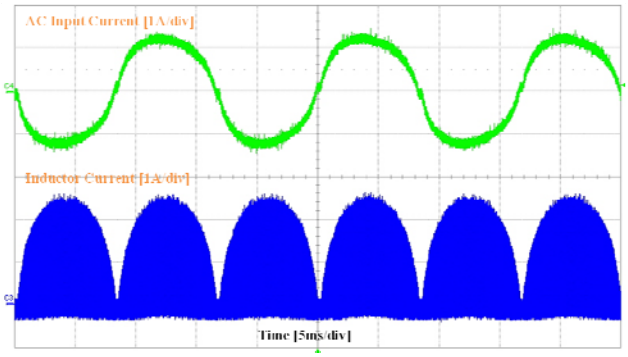


Figure 34. Inductor Current Waveforms at $115V_{AC}$

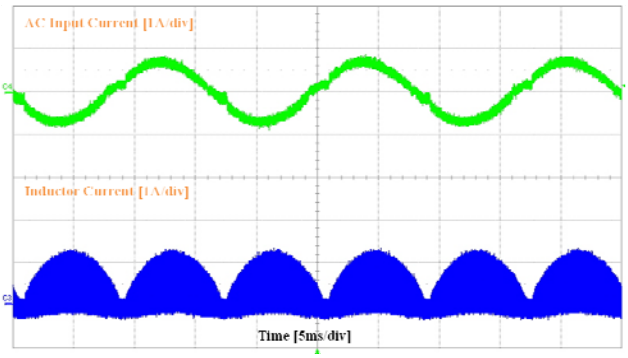


Figure 35. Inductor Current Waveforms at $230V_{AC}$

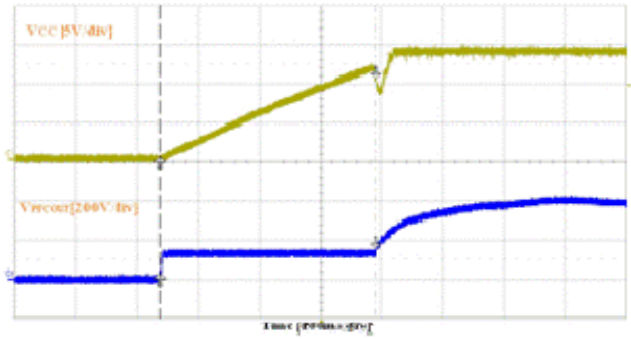
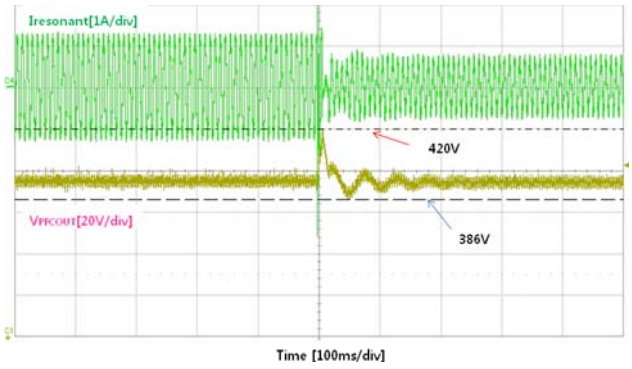
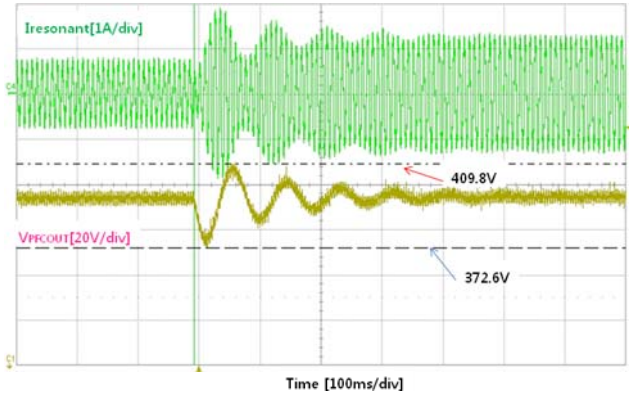


Figure 36. Startup Performance at $95V_{AC}$, Full Load

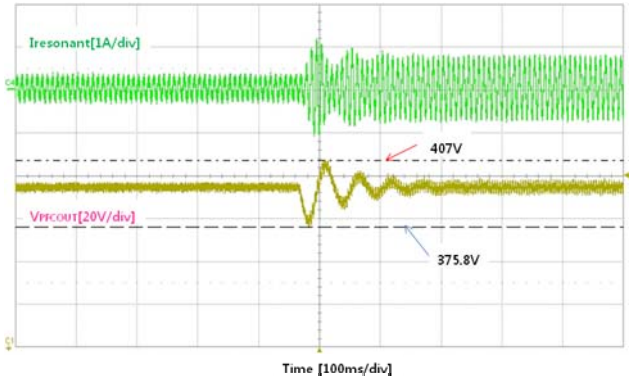


(a) Input Voltage Change from 115V to 235V

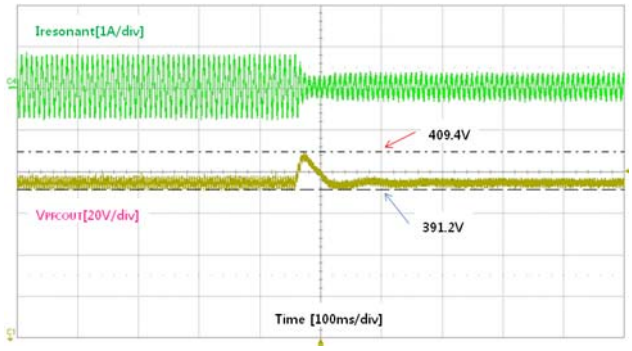


(b) Input Voltage Change from 235V to 115V

Figure 37. Output Dynamic Response at Po=100W



(a) Output Load Change from 0W to 100W



(b) Output Load Change from 100W to 0W

Figure 38. Output Dynamic Response at V_{IN}=$235V_{AC}$

Definition of Terms

η is the efficiency.
θ is the displacement angle.
ΔB is the maximum flux swing of the core at nominal output power in Tesla.
A_e is the cross-sectional area of core.
A_W is the window area of core.
B_{MAX} is the maximum flux density of boost inductor at maximum output power in Tesla.
$C_{COMP,HF}$ is the high-frequency compensation capacitance.
$C_{COMP,LF}$ is the low-frequency compensation capacitance.
C_{eff} is the effective capacitance shown at the MOSFET drain pin.
C_{EA} is the effective input capacitance to meet a given displacement factor.
C_{EXT} is the external capacitance at drain-source to decrease the turn-off slope.
C_{EQ} is the equivalent input capacitance.
C_{FB} is the feedback capacitance parallel with R_{FB2}.
C_{OUT} is the output capacitance.
C_{OSS} is the output capacitance of power MOSFET.
C_{PAR} is the parasitic capacitance at drain-source of power MOSFET.
C_{ZCD} is the capacitance connected at ZCD pin to improve noise immunity.
d_{WIRE} is the diameter of boost inductor winding wire.
DF is the displacement factor between input voltage and input current.
f_C is the crossover frequency.
f_{CP} is the high-frequency compensation pole to attenuate the switching ripple.
f_{CZ} is the compensation zero.
f_{LINE} is the line frequency.
f_I is the integral gain of the compensator.
f_P is the pole frequency in the PFC power stage transfer function.
f_{SW} is the switching frequency.
$f_{SW,MIN}$ is the minimum switching frequency.
$I_{CS,LIM}$ is the pulse-by-pulse current limit level determined by sensing resistor.
$I_{DOUT,AVE}$ is the average current of output diode.
$I_{IN,MAX}$ is the maximum input current from the AC outlet.
$I_{IN,MAXRMS}$ is the maximum RMS (Root Mean Square) input current from the AC outlet.
I_L is the inductor current at the nominal output power.
$I_{L,PK}$ is the maximum peak inductor current at the nominal output power.
$I_{L,RMS}$ is the RMS value of the inductor current at the nominal output power.
$I_{L,DENSITY}$ is the current density of the boost inductor coil.
I_{OUT} is the nominal output current of the boost PFC stage.
$I_{Q,RMS}$ is the RMS current at the power switch.
$I_{RDY,SK}$ is the allowable sink current for the internal MOSFET in RDY pin.
K_{SAW} is the internal gain of sawtooth generator (that of FL7930 is 8.496×10^{-6}).
L is the boost inductance.
N_{AUX} is the number of turns of auxiliary winding in boost inductor.
N_{BOOST} is the number of turns of primary winding in boost inductor.
N_{WIRE} is the number of strands of boost inductor winding wire.
P_{DOUT} is the loss of output diode.
P_{OUT} is the nominal output power of boost PFC stage.
$P_{Q,CON}$ is conduction loss of the power MOSFET.
$P_{Q,SWOFF}$ is turn-off loss of power MOSFET.
$P_{Q,DISCHRGE}$ is the drain-source capacitance discharge loss and consumed at power MOSFET.
P_Q is the total loss of power MOSFET made by $P_{Q,CON}$, $P_{Q,SWOFF}$, and $P_{Q,DISCHARGE}$.
P_{RCS} is the power loss caused by current-sense resistance.
R_{COMP} is the compensation resistance.
R_{CS} is the power MOSFET current-sense resistance.
$R_{DS,ON}$ is the static drain-source on resistance of the power switch.
R_{FB1} is the feedback resistance between the INV pin and output voltage.
R_{FB2} is the feedback resistance between the INV pin and ground.
R_L is the output load resistance in a given load condition.
R_{PULLUP} is the pull-up resistance between the RDY pin and pull-up voltage.

R_{ZCD} is the resistor connected at the ZCD pin to optimize THD.
t_{HOLD} is the required hold-up time.
t_{OFF} is the inductor current reset time.
$t_{ON,MAX}$ is the maximum on time fixed internally.
$t_{ON,MAX1}$ is the programmed maximum on time.
V_{COMP} is compensation pin voltage.
$V_{CS,LIM}$ is power MOSFET current-sense limit voltage.
$V_{DROP,DOUT}$ is the forward-voltage drop of output diode.
$V_{IN}(t)$ is the rectified line voltage.
$V_{IN,PK}$ is the amplitude of line voltage.
V_{LINE} is RMS line voltage.
$V_{LINE,MAX}$ is the maximum RMS line voltage.
$V_{LINE,MIN}$ is the minimum RMS line voltage.
$V_{LINE,OVP}$ is the line OVP trip point in RMS.
$V_{OPTO,F}$ is the input forward voltage drop of opto-coupler.
V_{OUT} is the PFC output voltage.
$V_{OUT,MIN}$ is the allowable minimum output voltage during the hold-up time.
$V_{OUT,RDYH}$ is the V_{OUT} to trigger PFC RDY out pulls high.
$V_{OUT,RDYL}$ is the V_{OUT} to trigger PFC RDY out drops to zero.
$\Delta V_{OUT,RIPPLE}$ is the peak-to-peak output voltage ripple.
V_{PULLUP} is the pull-up voltage for RDY pin.
$V_{RDY,SAT}$ is the internal saturation voltage of RDY pin.
V_{REF} is the internal reference voltage for the feedback input.
$V_{OVP,MAX}$ is the maximum tolerance of Over-Voltage Protection specification
$V_{ST,COUT}$ is the voltage stress at the output capacitor.
$V_{ST,Q}$ is the voltage stress at the power MOSFET.

References

[1] *Fairchild Datasheet FAN9612, Interleaved Dual BCM, PFC Controller*

[2] *Fairchild Datasheet FL7930 Critical Conduction Mode PFC Controller*

[3] *Fairchild Application Note AN-6027, Design of Power Factor Correction Circuit Using FAN7530*

[4] *Fairchild Application Note AN-8035, Design of Power Factor Correction Circuit Using FAN7930*

[5] *Fairchild Application Note AN-6086, Design Consideration for Interleaved BCM PFC using FAN9612*

[6] Robert W. Erikson, Dragan Maksimovic, *Fundamentals of Power Electronics, Second Edition*, Kluwer Academic Publishers, 2001.

Related Datasheets

FL7930 — Critical Conduction Mode PFC Controller

FAN9611 / FAN9612 — Interleaved Dual BCM PFC Controllers

1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 Small Signal Diode

PN2222A/MMBT2222A/PZT2222A NPN General Purpose Amplifier

FDP12N60NZ *— 600V N-Channel MOSFET, UniFET™*

FFPF08H60S — 8A, 600V Hyperfast Rectifier