

MM74HCT14

Hex Inverting Schmitt Trigger

Features


- Typical Propagation Delay: 13ns
- Wide Power Supply Range: 4.5V–5.5V
- Low Quiescent Current: 10µA Maximum
- Low Input Current: 1µA Maximum
- Fanout of 10 LS-TTL Loads
- Typical Hysteresis Voltage: 0.6V at $V_{CC} = 4.5V$
- TTL, LS Pin-out and Input Threshold Compatible

Description

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout-compatible with the standard 74LS logic family. Inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

Part Number	Operating Temperature Range	 Eco Status	Package	Packing Method
MM74HCT14M	-40°C to +85°C	RoHS	14-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150in Narrow	Tube
MM74HCT14MX	-40°C to +85°C	RoHS	14-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150in Narrow	Tape & Reel
MM74HCT14SJ	-40°C to +85°C	RoHS	14-Lead, Small-Outline Package (SOP), EIAJ Type II, 5.3mm Wide	Tube
MM74HCT14SJX	-40°C to +85°C	RoHS	14-Lead, Small-Outline Package (SOP), EIAJ Type II, 5.3mm Wide	Tape & Reel
MM74HCT14MTC	-40°C to +85°C	RoHS	14-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tube
MM74HCT14MTCX	-40°C to +85°C	RoHS	14-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape & Reel
MM74HCT14SN	-40°C to +85°C	RoHS	14-Lead, Plastic Dual-Inline Package (PDIP), JEDEC MS-001, 0.300in Wide	Tube

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Connection Diagram

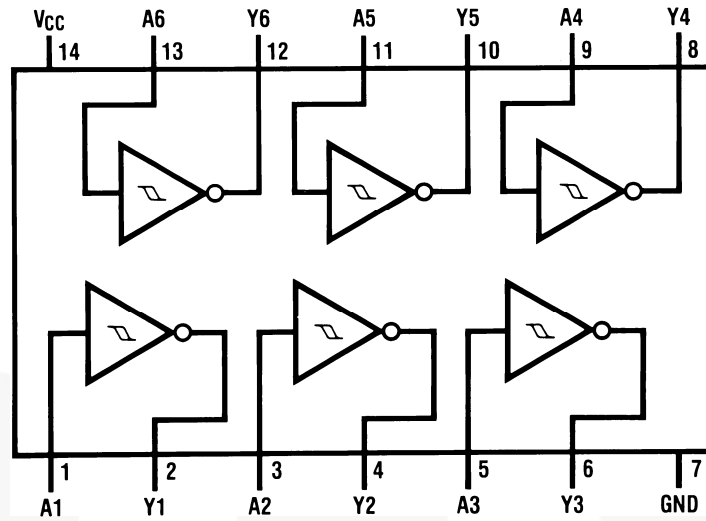


Figure 1. Pin Assignments

Schematic Diagram

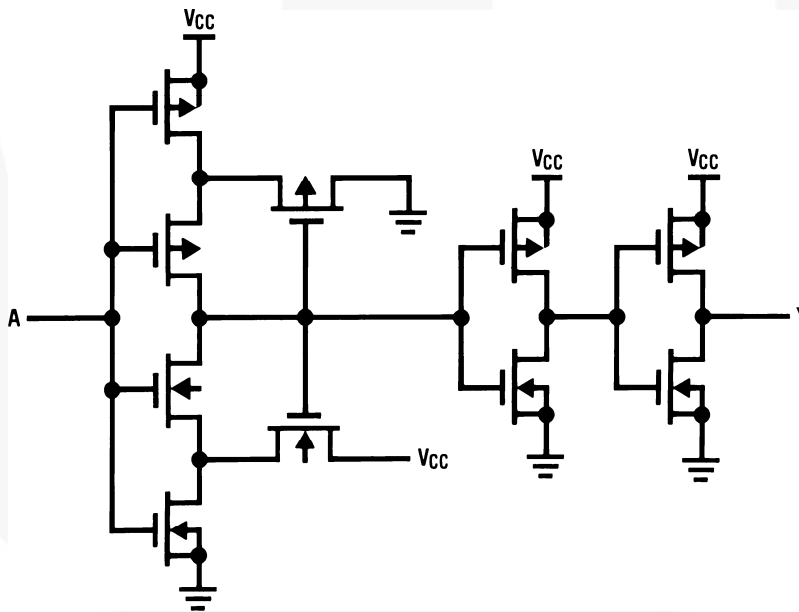


Figure 2. Schematic

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Unless otherwise specified, all voltages are referenced to ground.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+7.0	V
V_{IN}	DC Input Voltage	-1.5	$V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage	-0.5	$V_{CC} + 0.5$	V
I_K, I_{OK}	Clamp Diode Current		± 20	mA
I_{OUT}	DC Output Current, Per Pin		± 25	mA
I_{CC}	DC V_{CC} or GND Current, Per Pin		± 50	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_L	Lead Temperature (Soldering 10 Seconds)		+260	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-40	+85	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A =+25°C		T _A =-40°C to +85°C	Units
				Typ.	Guaranteed Limits		
V _{T+}	Positive-Going Threshold Voltage	Minimum	4.5	1.5	1.2	1.2	V
			5.5	1.7	1.4	1.4	
		Maximum	4.5	1.5	1.9	1.9	
			5.5	1.7	2.1	2.1	
V _{T-}	Negative-Going Threshold Voltage	Minimum	4.5	0.9	0.5	0.5	V
			5.5	1.0	0.6	0.6	
		Maximum	4.5	0.9	1.2	1.2	
			5.5	1.0	1.4	1.4	
V _H	Hysteresis Voltage	Minimum	4.5	0.6	0.4	0.4	V
			5.5	0.7	0.4	0.4	
		Maximum	4.5	0.6	1.4	1.4	
			5.5	0.7	1.5	1.5	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IL} , I _{OUT} = 20μA	4.5	V _{CC}	V _{CC} - 0.1	V _{CC} - 0.1	V
		V _{IN} = V _{IL} , I _{OUT} = 4.0mA	4.5	4.20	3.98	3.84	
		V _{IN} = V _{IL} , I _{OUT} = 4.8mA	5.5	5.20	4.98	4.98	
V _{OL}	Maximum LOW Level Voltage	V _{IN} = V _{IL} , I _{OUT} = 20μA	4.5	0	0.1	0.1	V
		V _{IN} = V _{IL} , I _{OUT} = 4.0mA	4.5	0.2	0.26	0.33	
		V _{IN} = V _{IL} , I _{OUT} = 4.8mA	5.5	0.2	0.26	0.33	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}	5.5		±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA	5.5		1.0	10.0	μA
		V _{IN} = 2.4V or 0.5V			2.4	2.4	mA

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, $t_r = t_f = 6ns$.

Symbol	Parameter	Typ.	Guaranteed Limit	Unit
t_{PHL} , t_{PLH}	Maximum Propagation Delay	10	18	ns

AC Electrical Characteristics

Unless otherwise specified, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $t_r = t_f = 6ns$.

Symbol	Parameter	Conditions	$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$	Units
			Typ.	Guaranteed Limits		
t_{PHL} , t_{PLH}	Maximum Propagation Delay			20	25	ns
t_{TLH} , t_{THL}	Maximum Output Rise and Fall Time		9	15	19	ns
C_{PD}	Power Dissipation Capacitance ⁽¹⁾	Per Gate		25		pF
C_{IN}	Maximum Input Capacitance		5	10	10	pF

Note:

- C_{PD} determines the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no-load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Applications

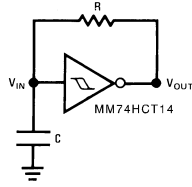


Figure 3. Low Power Oscillator

The following equations assume $t_1+t_2 \gg t_{pd0}+t_{pd1}$:

$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \quad (1)$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}} \quad (2)$$

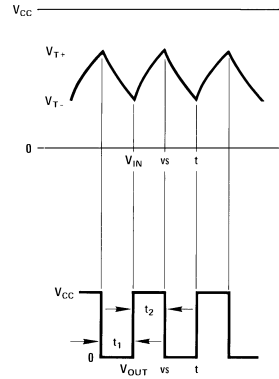


Figure 4. Oscillator Input and Output Waveforms



Physical Dimensions

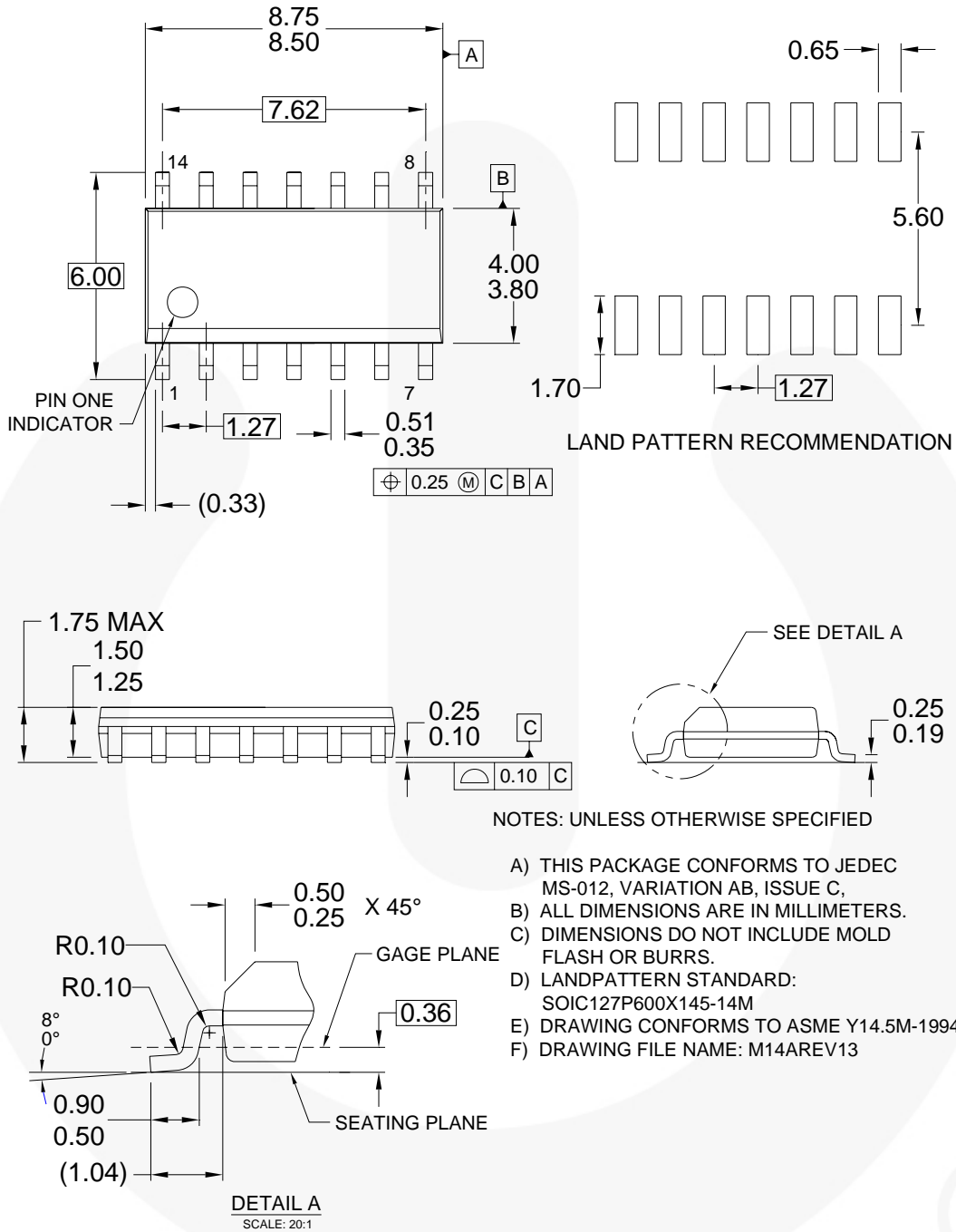
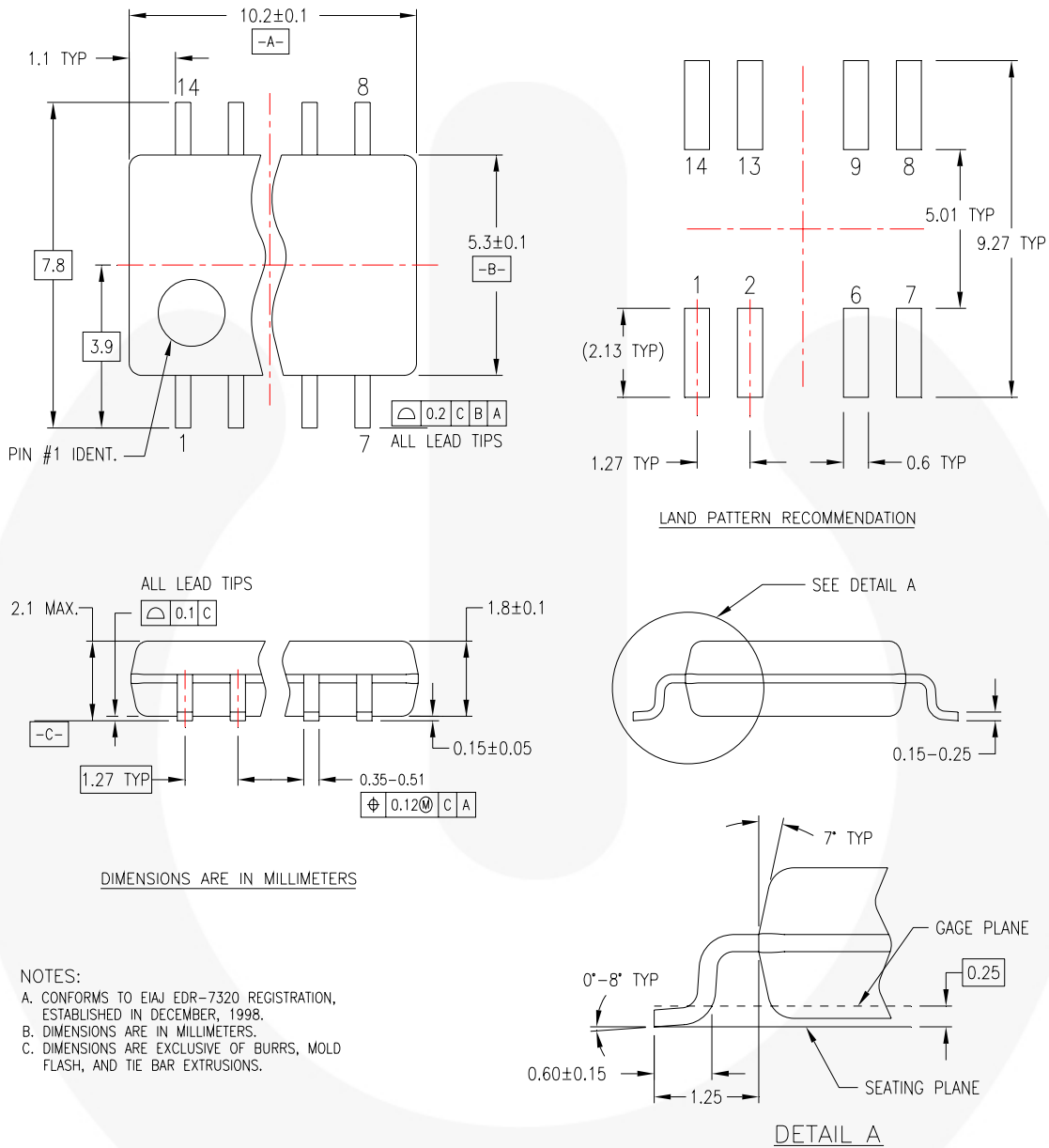


Figure 5. 14-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150in Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>

Physical Dimensions



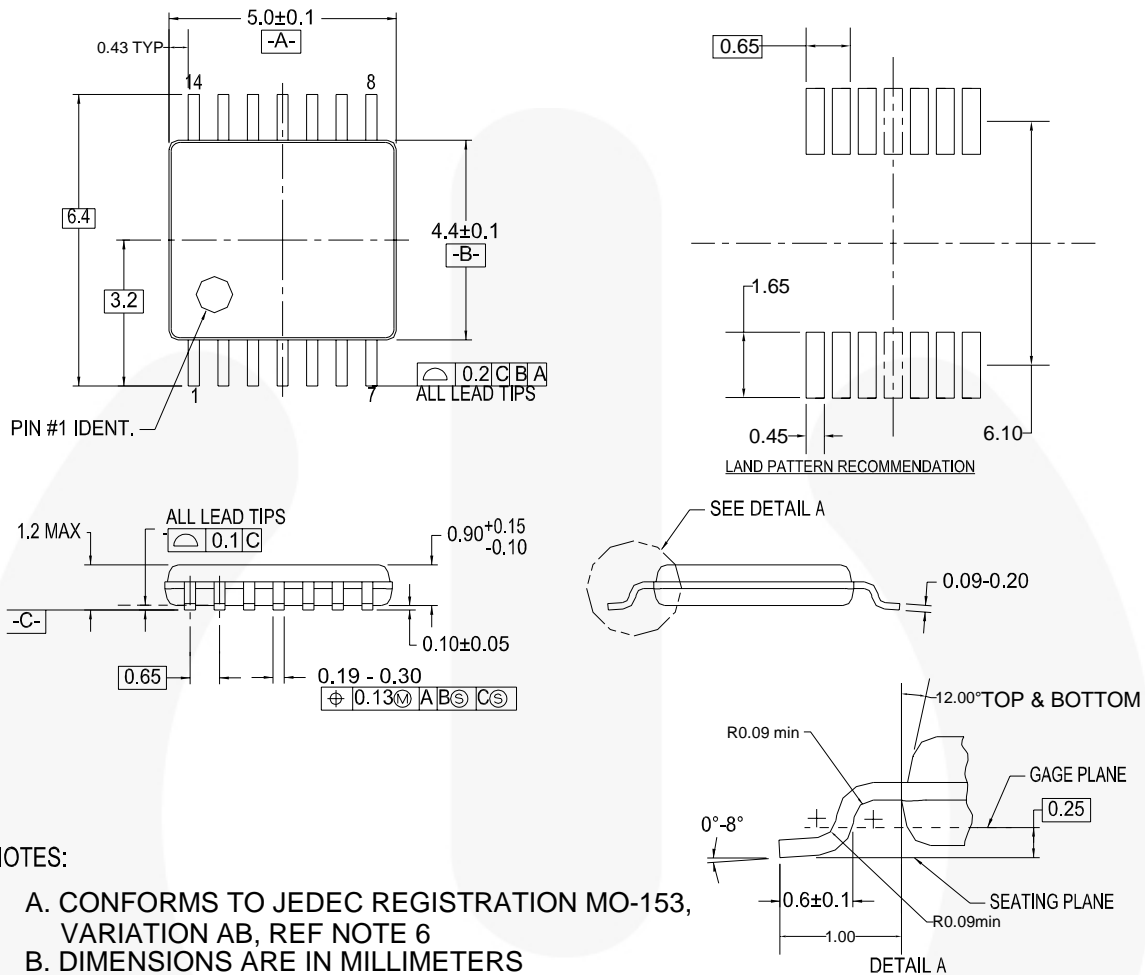
M14DREVC

Figure 6. 14-Lead, Small-Outline Package (SOP), EIAJ Type II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>

Physical Dimensions



NOTES:

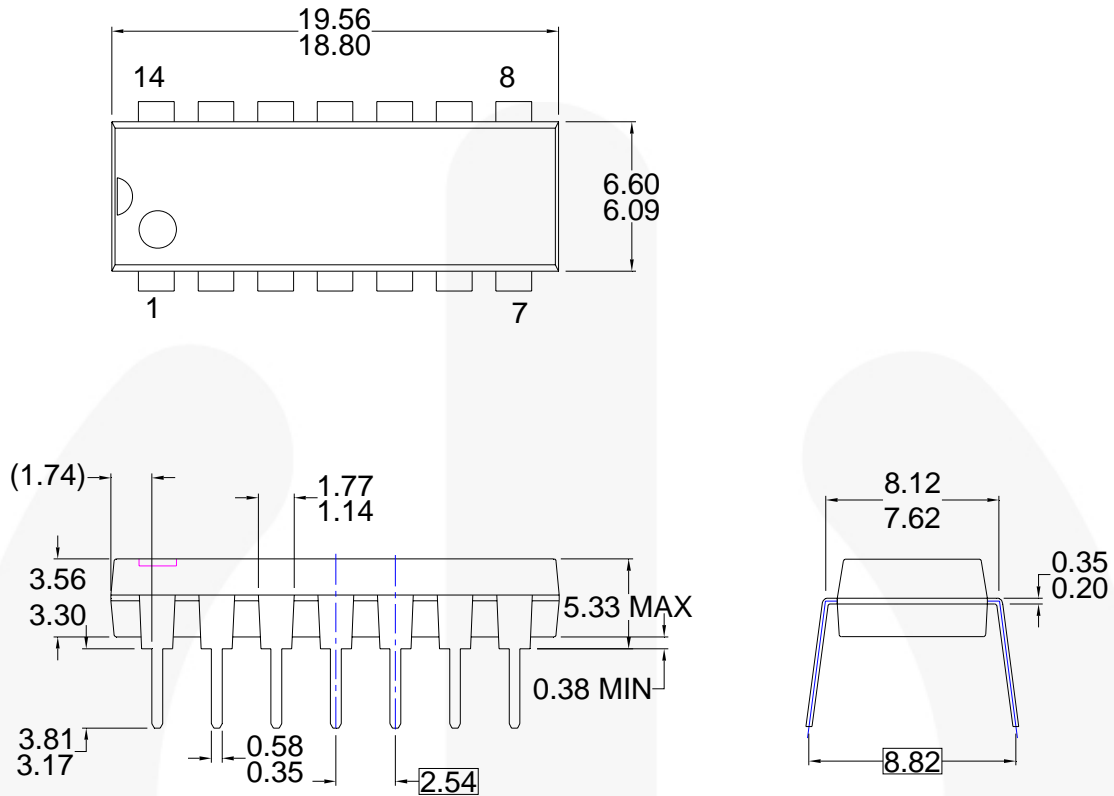
- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- LANDPATTERN STANDARD: SOP65P640X110-14M
- DRAWING FILE NAME: MTC14REV6

Figure 7. 14-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.

Physical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
THIS PACKAGE CONFORMS TO**
- A) JEDEC MS-001 VARIATION BA
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994
 - E) DRAWING FILE NAME: MKT-N14AREV7

Figure 8. 14-Lead, Plastic Dual-Inline Package (PDIP), JEDEC MS-001, 0.300in Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
 Auto-SPM™
 Build it Now™
 CorePLUS™
 CorePOWER™
 CROSSVOLT™
 CTL™
 Current Transfer Logic™
 EcoSPARK®
 EfficientMax™
 EZSWITCH™
™
 DEUXPEED™
®
 Fairchild®
 Fairchild Semiconductor®
 FACT Quiet Series™
 FACT®
 FAST®
 FastvCore™
 FETBench™

FlashWriter®*
 FPS™
 F-PFS™
 FRFET®
 Global Power Resource™
 Green FPST™
 Green FPST™ e-Series™
 Gmax™
 GTO™
 IntelliMAX™
 ISOPLANAR™
 MegaBuck™
 MICROCOUPLER™
 MicroFET™
 MicroPak™
 MillerDrive™
 MotionMax™
 Motion-SPM™
 OPTOLOGIC®
 OPTOPLANAR®

 PDP SPM™

Power-SPM™
 PowerTrench®
 PowerXS™
 Programmable Active Droop™
 QFET®
 QST™
 Quiet Series™
 RapidConfigure™
™
 Saving our world, 1mW/W/kW at a time™
 SignalWise™
 SmartMax™
 SMART START™
 SPM®
 STEALTH™
 SuperFET™
 SuperSOT™-3
 SuperSOT™-6
 SuperSOT™-8
 SupreMOS™
 SyncFET™
 Sync-Lock™

 SYSTEM®
 GENERAL®
 The Power Franchise®
 the power franchise
 TinyBoost™
 TinyBuck™
 TinyCalc™
 TinyLogic®
 TINYOPTO™
 TinyPower™
 TinyPWM™
 TinyWire™
 TriFault Detect™
 TRUECURRENT™
 µSerDes™
 SerDes®
 UHC®
 Ultra FRFET™
 UniFET™
 VCX™
 VisualMax™
 XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I43