PM50CSD120

FLAT-BASE TYPE
INSULATED PACKAGE

PM50CSD120

FEATURE

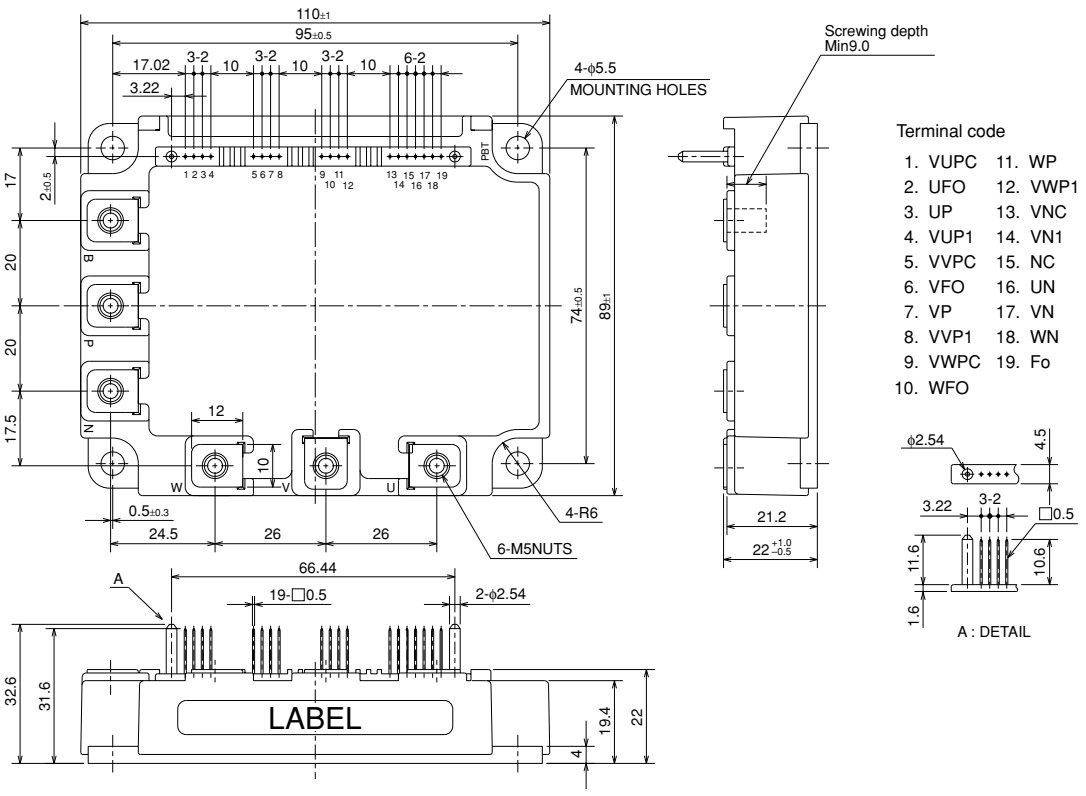
a) Adopting new 4th generation planar IGBT chip, which performance is improved by 1μm fine rule process.
b) Using new Diode which is designed to get soft reverse recovery characteristics.
c) Keeping the package compatibility.
The layout/position of both terminal pin and mounting hole is same as S-series 3rd generation IPM.

- 3ϕ 50A, 1200V Current-sense IGBT for 15kHz switching
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage (P-Fo available from upper leg devices)
- Acoustic noise-less 5.5/7.5kW class inverter application

APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES **Dimensions in mm**



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PM50CSD120

FLAT-BASE TYPE
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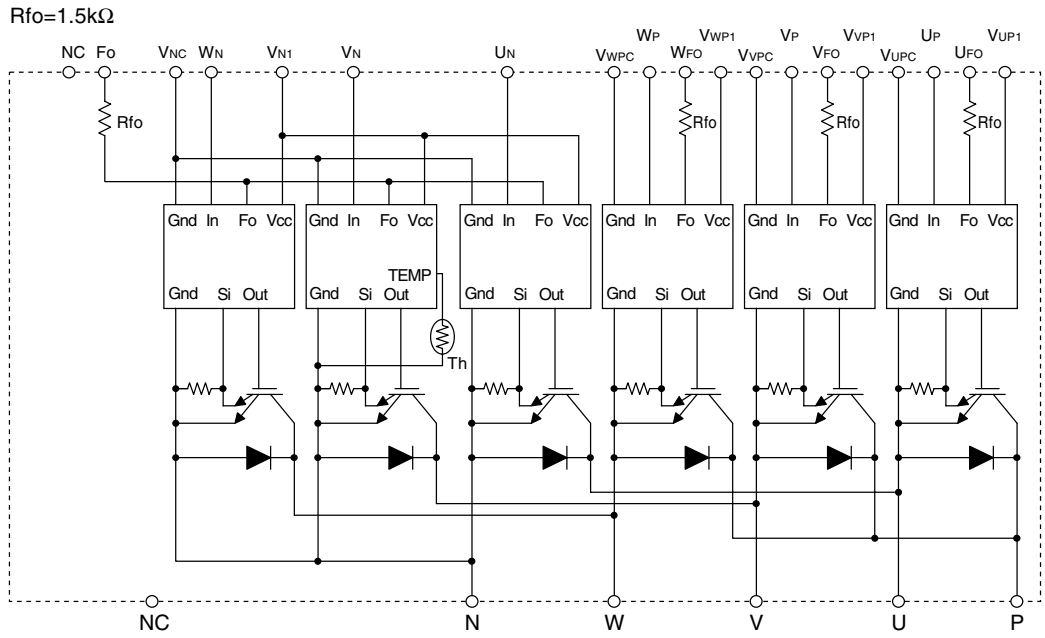
INTERNAL FUNCTIONS BLOCK DIAGRAM



MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	V_D = 15V, V_{CIN} = 15V	1200	V
±I_C	Collector Current	T_C = 25°C	50	A
±I_{CP}	Collector Current (Peak)	T_C = 25°C	100	A
P_C	Collector Dissipation	T_C = 25°C	328	W
T_j	Junction Temperature		–20 ~ +150	°C

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Supply Voltage	Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, U_N • V_N • W_N-V_{NC}	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : U_{FO}-V_{UPC}, V_{FO}-V_{VPC}, W_{FO}-V_{WPC}, F_O-V_{NC}	20	V
I_{FO}	Fault Output Current	Sink current at U_{FO}, V_{FO}, W_{FO}, F_O terminals	20	mA

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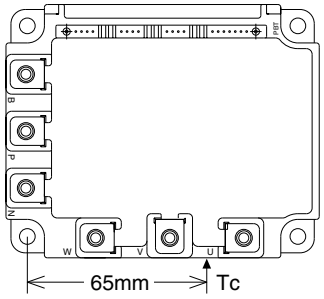
TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by OC & SC	V_D = 13.5 ~ 16.5V, Inverter Part, T_j = 125°C Start	800	V
$V_{CC(surge)}$	Supply Voltage (Surge)	Applied between : P-N, Surge value or without switching	1000	V
T_C	Module Case Operating Temperature	(Note-1)	–20 ~ +100	°C
T_{stg}	Storage Temperature		–40 ~ +125	°C
V_{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V_{rms}

(Note-1) T_C measurement point is as shown below. (Base plate depth 3mm)



THERMAL RESISTANCES

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element), (Note-1)	—	—	0.38	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1 element), (Note-1)	—	—	0.70	
$R_{th(j-c')Q}$		Inverter IGBT part (per 1 element), (Note-2)	—	—	0.23	
$R_{th(j-c')F}$		Inverter FWDi part (per 1 element), (Note-2)	—	—	0.36	
$R_{th(c-f)}$	Contact Thermal Resistance	Case to fin, Thermal grease applied (per 1 module)	—	—	0.027	

(Note-2) T_C measurement point is just under the chips.
If you use this value, $R_{th(f-a)}$ should be measured just under the chips.

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_D = 15V, I_C = 50A, V_{CIN} = 0V, Pulsed (Fig. 1)	T_j = 25°C	—	2.4	3.2	V
			T_j = 125°C	—	2.1	2.8	
V_{EC}	FWDi Forward Voltage	–I_C = 50A, V_D = 15V, V_{CIN} = 15V (Fig. 2)		—	2.5	3.5	V
t_{on}	Switching Time	V_D = 15V, V_{CIN} = 15V↔0V, V_{CC} = 600V, I_C = 50A, T_j = 125°C, Inductive Load (upper and lower arm) (Fig. 3)		0.5	1.0	2.5	µs
t_{rr}				—	0.15	0.3	
$t_{c(on)}$				—	0.4	1.0	
t_{off}				—	2.5	3.5	
$t_{c(off)}$				—	0.7	1.2	
I_{CES}	Collector-Emitter Cutoff Current	V_{CE} = V_{CES}, V_{CIN} = 15V (Fig. 4)	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

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CONTROL PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit Current	V_D = 15V, V_{CIN} = 15V	V_{N1}-V_{NC}	—	40	55	mA
			V_{XP1}-V_{XPC}	—	13	18	
$V_{th(on)}$	Input ON Threshold Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}		1.2	1.5	1.8	V
$V_{th(off)}$	Input OFF Threshold Voltage	U_N • V_N • W_N-V_{NC}		1.7	2.0	2.3	
OC	Over Current Trip Level	V_D = 15V (Fig. 5,6)	T_j = 25°C	93	157	—	A
			T_j = 125°C	59	—	—	
SC	Short Circuit Trip Level	–20≤ T_j ≤ 125°C, V_D = 15V (Fig. 5,6)		—	183	—	A
$t_{off(OC)}$	Over Current Delay Time	V_D = 15V (Fig. 5,6)		—	10	—	µs
OT	Over Temperature Protection	Base-plate Temperature detection, V_D = 15V	Trip level	111	118	125	°C
OT_r			Reset level	—	100	—	
UV	Supply Circuit Under-Voltage Protection	–20 ≤ T_j ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV_r			Reset level	—	12.5	—	
$I_{FO(H)}$	Fault Output Current	V_D = 15V, V_{FO} = 15V (Note-3)		—	—	0.01	mA
$I_{FO(L)}$				—	10	15	
t_{FO}	Minimum Fault Output Pulse Width	V_D = 15V (Note-3)		1.0	1.8	—	ms

(Note-3) Fault output is given only when the internal OC, SC, OT & UV protection.
Fault output of OC, SC and UV protection operate by upper and lower arms.
Fault output of OT protection operate by lower arm.
Fault output of OC, SC protection given pulse.
Fault output of OT, UV protection given pulse while over level.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	560	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V_{CC}	Supply Voltage	Applied across P-N terminals	≤ 800	V
V_D	Control Supply Voltage	Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC} V_{WP1}-V_{WPC}, V_{N1}-V_{NC} (Note-4)	15 ± 1.5	V
$V_{CIN(on)}$	Input ON Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}	≤ 0.8	V
$V_{CIN(off)}$	Input OFF Voltage	U_N • V_N • W_N-V_{NC}	≥ 4.0	
f_{PWM}	PWM Input Frequency	Using Application Circuit input signal of IPM, 3ϕ sinusoidal PWM VVVF inverter (Fig. 8)	≤ 20	kHz
t_{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 3.0	µs

(Note-4) Allowable Ripple rating of Control Voltage : $dv/dt \leq \pm 5V/\mu s$, $2V_{p\text{-}p}$

PRECAUTIONS FOR TESTING

1. Before appling any control supply voltage (V_D), the input terminals should be pulled up by resistores, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “OC” and “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

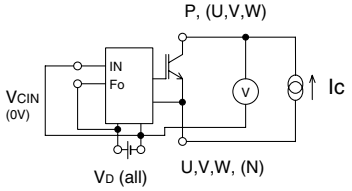

Fig. 1 $V_{CE(sat)}$ Test

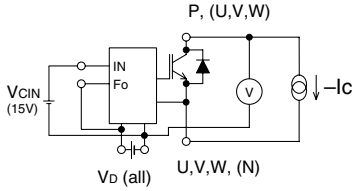

Fig. 2 V_{EC} Test

a) Lower Arm Switching

b) Upper Arm Switching

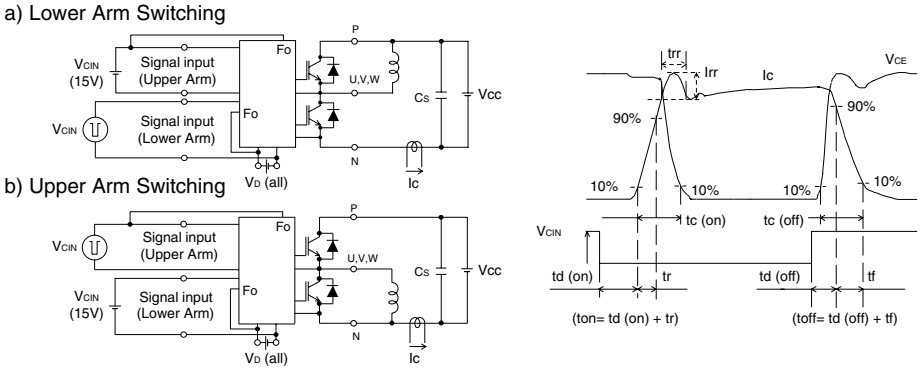

Fig. 3 Switching time Test circuit and waveform

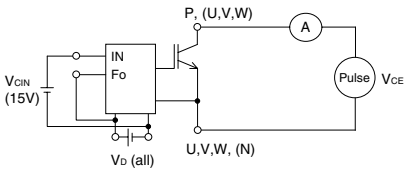

Fig. 4 I_{CES} Test

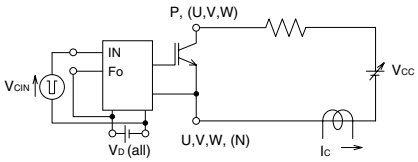

Fig. 5 OC and SC Test

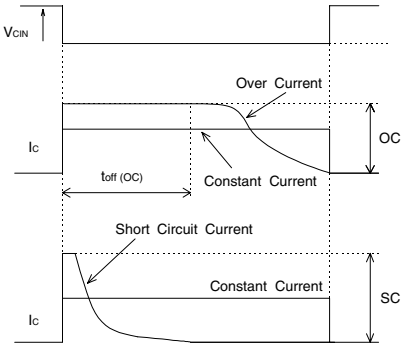

Fig. 6 OC and SC Test waveform

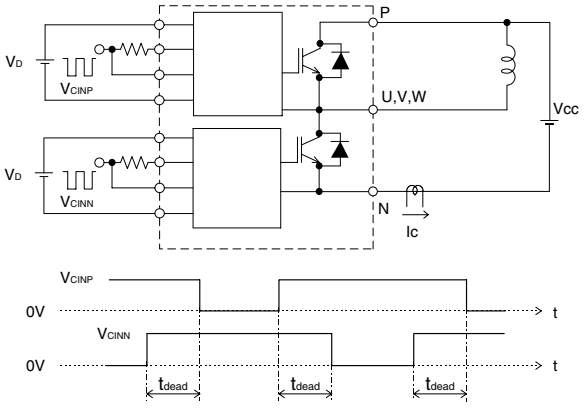

Fig. 7 Dead time measurement point example

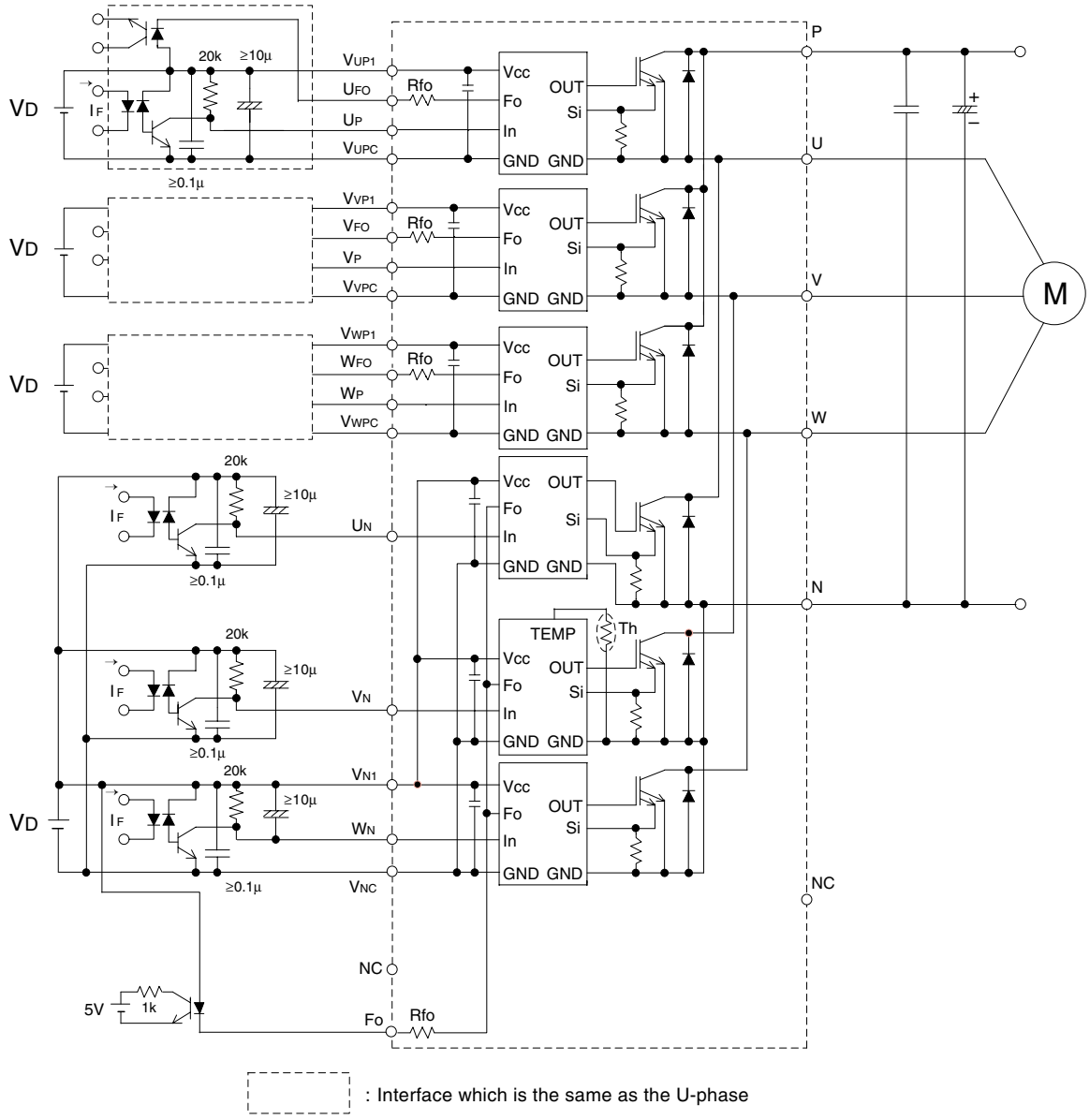

Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Quick opto-couplers: TPLH, TPLH ≤ 0.8μs. Use High CMR type. The line between opto-coupler and intelligent module should be shortened as much as possible to minimize the floating capacitance.
- Slow switching opto-coupler: recommend to use at CTR = 100 ~ 200%, Input current = 8 ~ 10mA, to work in active.
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.