

### Features:

- Advanced trench process technology
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Avalanche Energy 100% test

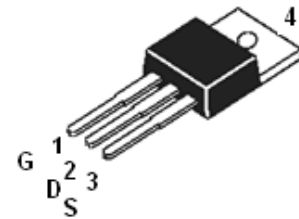
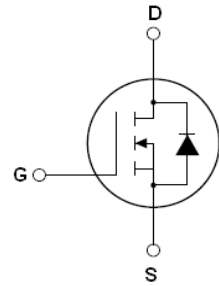
### Description:

The SSF3018D is a new generation of middle voltage and high current N-Channel enhancement mode trench power MOSFET. This new technology increases the cell density and reduces the on-resistance; its typical Rdson can reduce to 11.6mohm.

### Application:

- Power switching application

**ID=80A**  
**BV=100V**  
**Rdson=14mohm**



SSF3018D TOP View (TO220)

### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D@T_c=25^\circ\text{C}$	Continuous drain current, VGS@10V	80	A
$I_D@T_c=100^\circ\text{C}$	Continuous drain current, VGS@10V	70	
$I_{DM}$	Pulsed drain current ①	320	
$P_D@T_c=25^\circ\text{C}$	Power dissipation	192	W
	Linear derating factor	2.0	W/°C
$V_{GS}$	Gate-to-Source voltage	±20	V
$E_{AS}$	Single pulse avalanche energy ②	460	mJ
$E_{AR}$	Repetitive avalanche energy	TBD	
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C

### Thermal Resistance

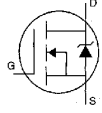
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	0.65	—	°C/W

### Electrical Characteristics @TJ=25 °C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source breakdown voltage	100	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	11.6	14	mΩ	$V_{GS}=10V, I_D=30A$
$V_{GS(th)}$	Gate threshold voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward transconductance	33	55	—	S	$V_{DS}=10V, I_D=40A$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	μA	$V_{DS}=100V, V_{GS}=0V$
		—	—	5		$V_{DS}=100V, V_{GS}=0V, T_J=150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	200	nA	$V_{GS}=20V$
	Gate-to-Source reverse leakage	—	—	-200		$V_{GS}=-20V$
$Q_g$	Total gate charge	—	60	—	nC	$I_D=25A$
$Q_{gs}$	Gate-to-Source charge	—	21	—	nC	$V_{DS}=0.5V_{DSS}$

$Q_{gd}$	Gate-to-Drain("Miller") charge	—	15	—		$V_{GS}=10V$
$t_{d(on)}$	Turn-on delay time	—	31	—	nS	$V_{DS}=0.5V_{DSS}$ $I_D=10A$ $R_G=15\Omega$ $V_{GS}=10V$
$t_r$	Rise time	—	54	—		
$t_{d(off)}$	Turn-Off delay time	—	40	—		
$t_f$	Fall time	—	48	—		
$C_{iss}$	Input capacitance	—	3040	—	pF	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHZ$
$C_{oss}$	Output capacitance	—	420	—		
$C_{rss}$	Reverse transfer capacitance	—	90	—		

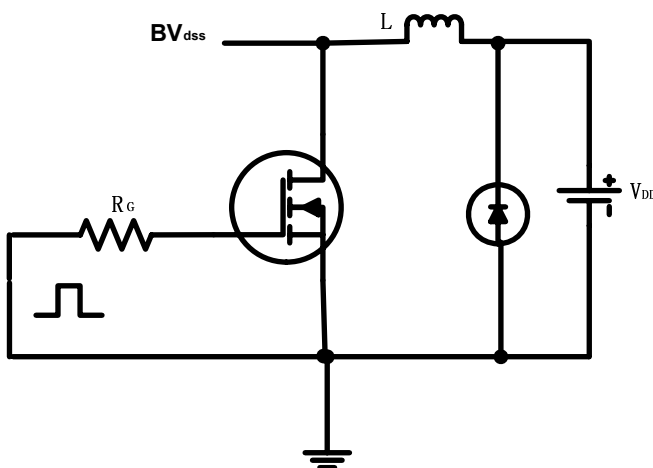
### Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current. (Body Diode)	—	—	80	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	320		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J=25^\circ C, I_S=30A, V_{GS}=0V$ ③
$t_{rr}$	Reverse Recovery Time	—	100	—	nS	$I_F=25A, V_R=50V, V_{GS}=0V,$ $-di/dt=100A/\mu s$ ③
$t_{on}$	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

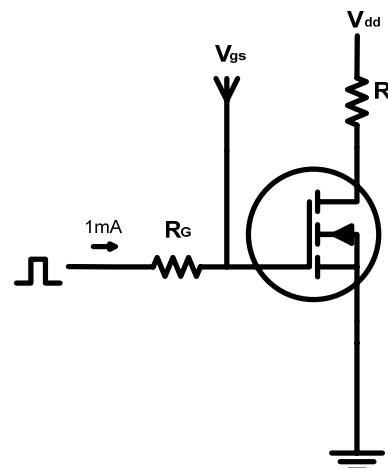
#### Notes:

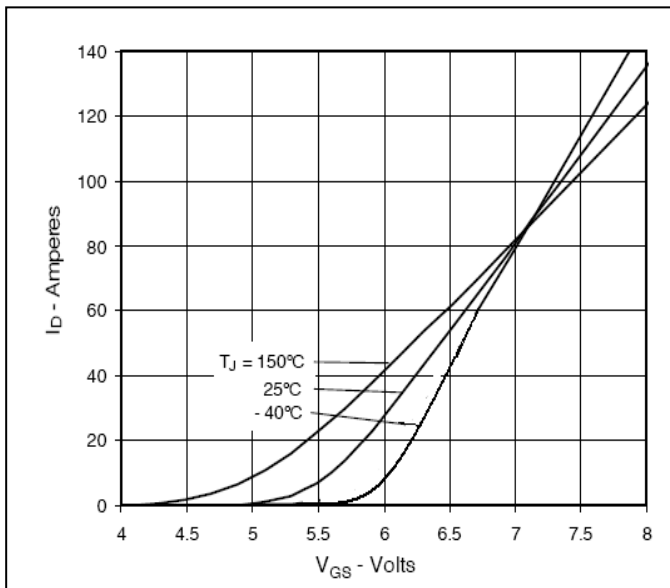
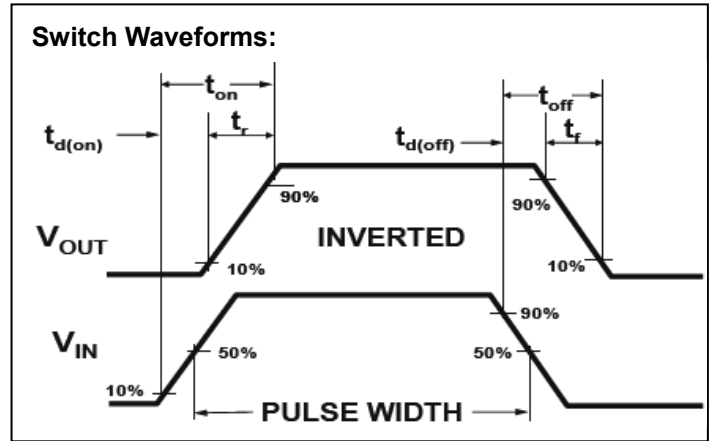
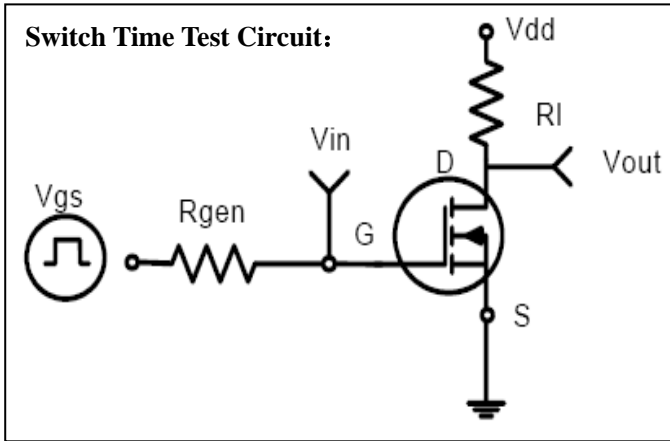
- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Test condition:  $L = 0.3mH, I_D = 37A, V_{DD} = 50V$
- ③ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 1.5\%$   $R_G = 25\Omega$  Starting  $T_J = 25^\circ C$

#### EAS test circuits:

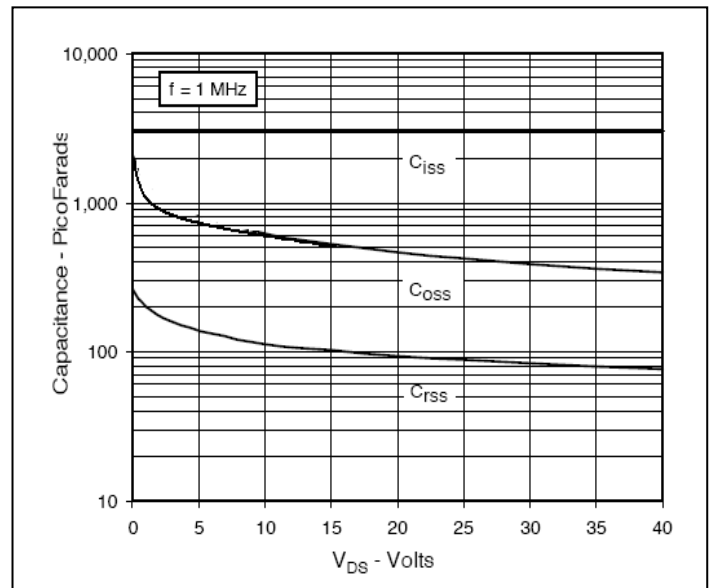


#### Gate charge test circuit:

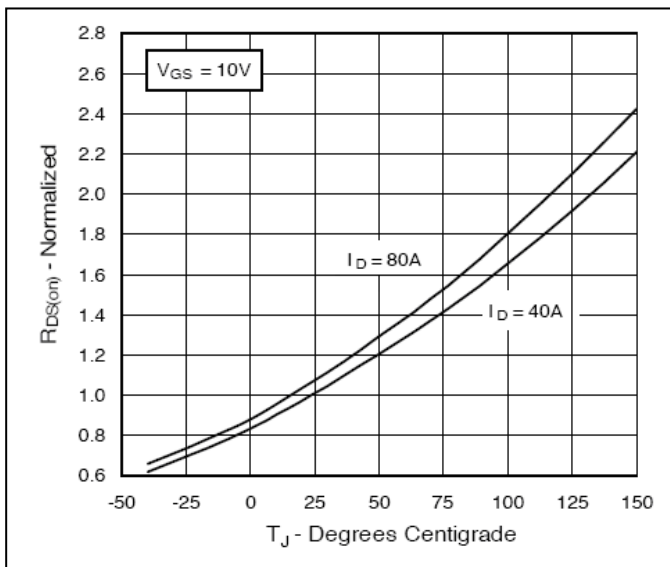




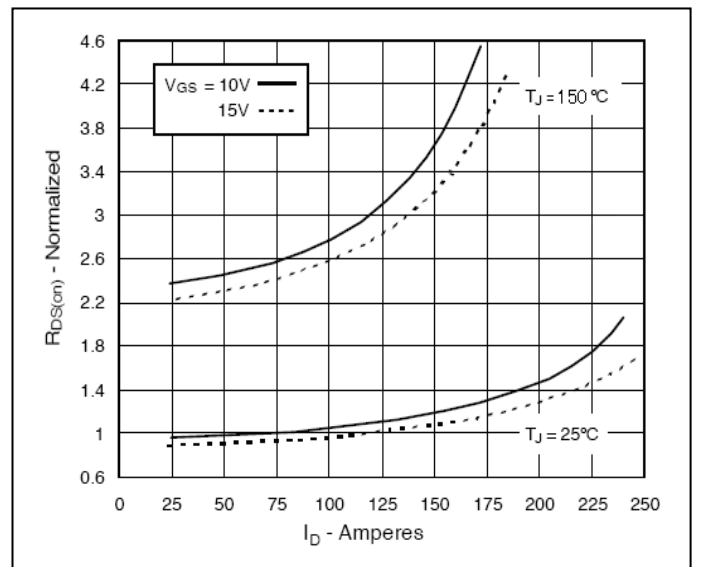
**Input Admittance**



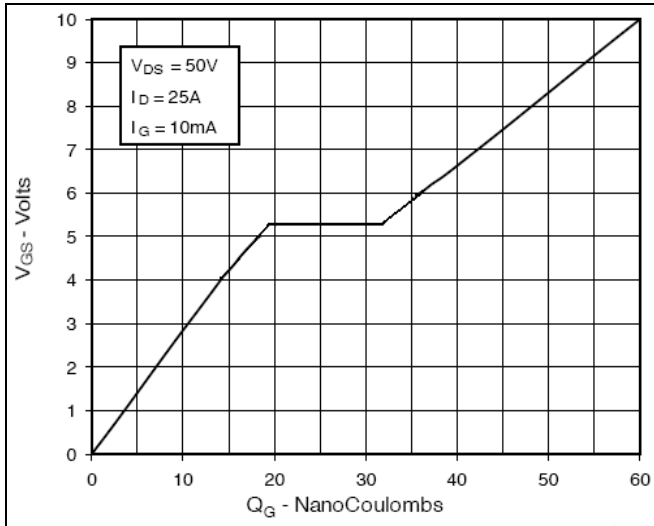
**Capacitance**



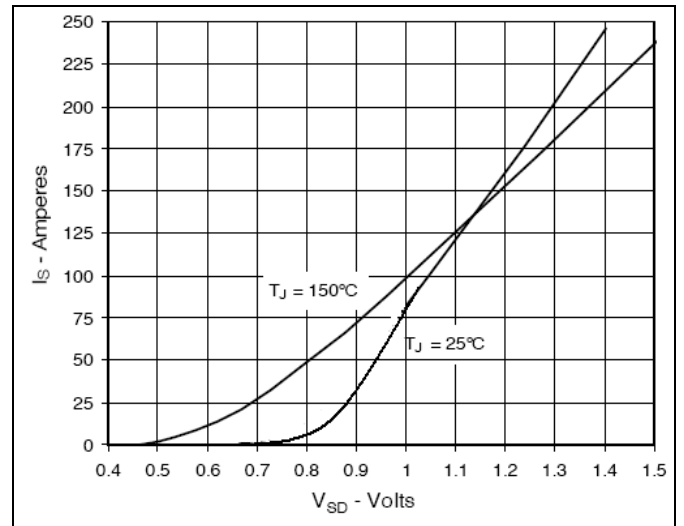
**On Resistance vs. Junction Temperature**



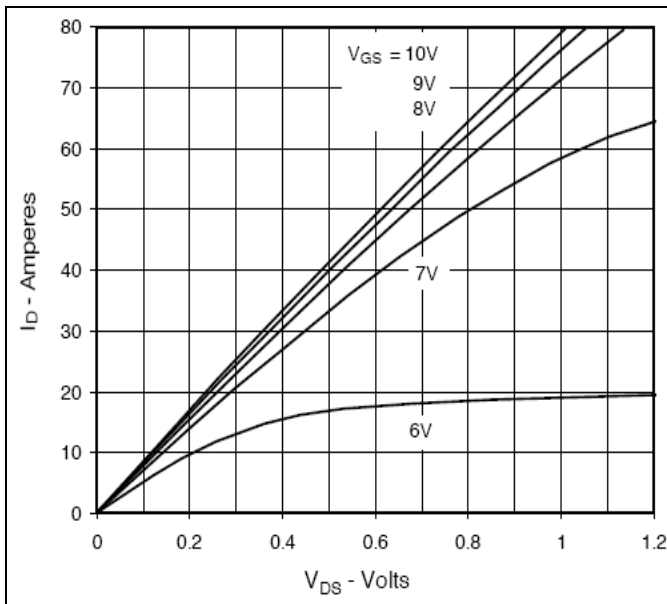
**On Resistance vs. Drain Current**



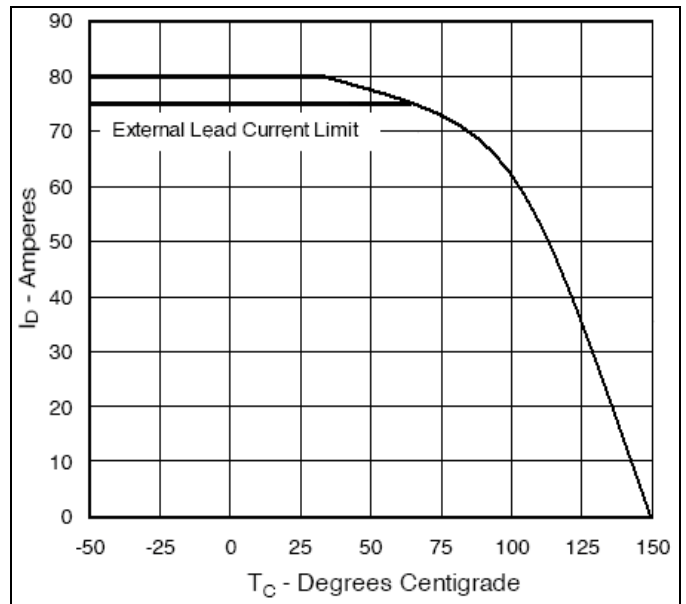
**Gate Charge**



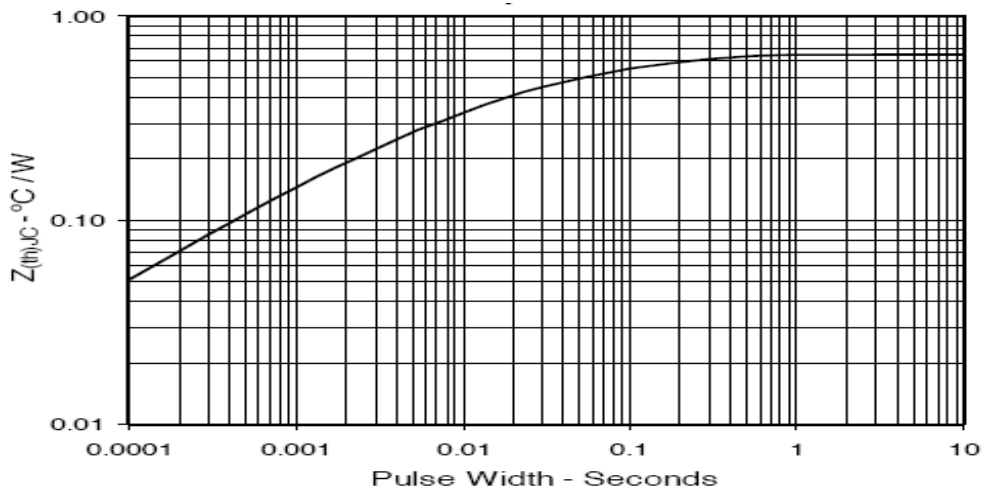
**Forward Voltage Drop of Intrinsic Diode**



**Output Characteristics@25°C**



**Drain Current vs. Case Temperature**



**Maximum Transient Thermal Impedance**

## TO220 MECHANICAL DATA:

