## **General Description**

**Applications** 

The MAX9752/MAX9753/MAX9754 combine a high-efficiency, filterless, stereo Class D audio power amplifier with a DirectDrive<sup>TM</sup> headphone amplifier in a single device. The Class D amplifier operates from a single 4.5V to 5.5V supply and provides 2.2W per channel into a 4 $\Omega$  load. The headphone amplifier operates from a single 3V to 5.5V supply, and uses Maxim's patented<sup>†</sup> DirectDrive architecture to produce a ground-referenced output from a single supply.

The MAX9754 features a Class D stereo speaker amplifier and headphone driver. The MAX9752 adds an analog volume control and a BEEP input. The MAX9753 adds a stereo 2:1 input multiplexer. All devices feature logic-selectable gain, and a headphone sense input that detects the presence of a headphone.

The MAX9752/MAX9753/MAX9754 come in 28-pin thin QFN (5mm x 5mm x 0.8mm) packages, and are specified over the extended -40°C to +85°C temperature range. For a pin-for-pin-compatible Class AB version of these devices, refer to the MAX9750/MAX9751/MAX9755 data sheet.

Notebook PCs	Flat-Panel TVs
Tablet PCs	PC Displays
Portable DVDs	LCD Projectors

## Pin Configurations appear at end of data sheet.

†U.S. Patent# 7,061,327

## Features

- PC2001 Compliant
- ♦ 2.2W Class D Stereo Speaker Amplifier
- Pin-for-Pin Compatible with Class AB MAX9750/MAX9751/MAX9755
- ♦ 85% Efficiency (R<sub>L</sub> = 8Ω, P<sub>OUT</sub> = 1W)
- ♦ 62mW DirectDrive Headphone Amplifier
- High PSRR (70dB at 1kHz)
- Analog Volume Control (MAX9752)
- Beep Input with Glitch Filter (MAX9752)
- ♦ 2:1 Stereo Input MUX (MAX9753)
- ♦ ±8kV ESD-Protected Headphone Outputs
- No Output DC-Blocking Capacitors
- Industry-Leading Click-and-Pop Suppression

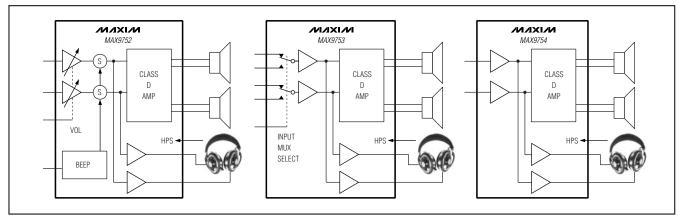
## \_Ordering Information

PART	PIN-PACKAGE	PKG CODE	MAXIMUM GAIN (dB)
MAX9752AETI+	28 TQFN-EP*	T2855-1	13.5
MAX9752BETI+	28 TQFN-EP*	T2855-1	19.5
MAX9752CETI+	28 TQFN-EP*	T2855-1	10.5
MAX9753ETI+	28 TQFN-EP*	T2855-1	13.5
MAX9754ETI+	28 TQFN-EP*	T2855-1	13.5

**Note:** All devices specified for -40°C to +85°C operation. +Denotes lead-free package. \*EP = Exposed paddle.

Er = Exposea padale.

## Block Diagrams



## 

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.



## **ABSOLUTE MAXIMUM RATINGS**

VDD, PVDD, HPVDD, CPVDD to GND	
GND to PGND or CPGND CPV <sub>SS</sub> or V <sub>SS</sub> to PGND	-6.0V to +0.3V
C1N to PGND	(CPV <sub>SS</sub> - 0.3V) to +0.3V
C1P to PGND	0.3V to (CPV <sub>DD</sub> + 0.3V)
HP_ to PGND (HPV <sub>SS</sub>	- 0.3V) to (HPV <sub>DD</sub> + 0.3V)
HP_ to PGND	
Any Other Pin to PGND	0.3V to (V <sub>DD</sub> + 0.3V)
Duration of OUT_Short Circuit to PGND	or PV <sub>DD</sub> Continuous
Duration of OUT_+ Short Circuit to OU	TContinuous
Duration of HP_ Short Circuit to PGND	Continuous

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

 $(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = +5.0V, GND = PGND = HPGND = 0V, V_{\overline{SHDN}} = V_{DD}, CPV_{SS} = V_{SS}, C_{BIAS} = 1\mu F, C_{CPVSS} = 1\mu F, C1 = 1\mu F, speaker impedance = 8\Omega connected between OUT_+ and OUT_-, headphone load is terminated to GND; MAX9752: GAIN1 = GAIN2 = 0, V_{VOL} = 0V; MAX9753: GAIN = 0, V_{\overline{A}/B} = 0V; MAX9754: GAIN = 0; T_A = T_{MIN}$  to T\_MAX, unless otherwise noted. Typical values are at T\_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
GENERAL	•	·					
Supply Voltage Range, Speaker Amplifier	V <sub>DD</sub> , PV <sub>DD</sub>	Inferred from PSRR test		4.5		5.5	V
Supply Voltage Range, Headphone Amplifier	HPVDD	Inferred from PSRR te	st	3.0		5.5	V
Outine course of	1	Speaker mode, no load			14	18	A
Quiescent Current	IDD	Headphone mode, no	load		7.2	9.5	mA
Shutdown Supply Current	ISHDN	V <del>SHDN</del> = 0V			0.2	8	μA
Gain Switching Time	tswg				3		μs
Mux Switching Time	tswm	MAX9753 only			3		μs
Input Decistopee	Dut	MAX9752		10	20	30	kΩ
Input Resistance	R <sub>IN</sub>	MAX9753/MAX9754	MAX9753/MAX9754		6.6	10.0	
Turn-On Time	ton				25		ms
CLASS D SPEAKER AMPLIFIE	RS (HPS = GNI	D)					
		MAX9752A, MAX9752B,	$T_A = +25^{\circ}C$		±9.6	±38.8	
Output Offset Voltage OUT + to OUT -	V <sub>OS</sub>	MAX9753, MAX9754	$T_A = T_{MIN}$ to $T_{MAX}$			±55	mV
001_+ 10 001		MAYOZEOO	$T_A = +25^{\circ}C$		±7	±40	
		MAX9752C	$T_A = T_{MIN}$ to $T_{MAX}$			±60	
		$PV_{DD}$ or $V_{DD} = 4.5V$ to	o 5.5V, T <sub>A</sub> = +25°C	50	74		
Power-Supply Rejection Ratio (Note 3)	PSRR	$f = 1 kHz, V_{RIPPLE} = 10$	00mV <sub>P-P</sub>		70		dB
		f = 10kHz, V <sub>RIPPLE</sub> = <sup>-</sup>	100mV <sub>P-P</sub>		60		

## **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = +5.0V, GND = PGND = HPGND = 0V, V_{\overline{SHDN}} = V_{DD}, CPV_{SS} = V_{SS}, C_{BIAS} = 1\mu F, C_{CPVSS} = 1\mu F, C1 = 1\mu F, speaker impedance = 8\Omega connected between OUT_+ and OUT_-, headphone load is terminated to GND; MAX9752: GAIN1 = GAIN2 = 0, V_{VOL} = 0V; MAX9753: GAIN = 0, V_{\overline{A}/B} = 0V; MAX9754: GAIN = 0; T_A = T_{MIN}$  to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T\_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CON	DITIONS	MIN	ТҮР	MAX	UNITS	
			GAIN1 = 0, GAIN2 = 0		9.0			
			GAIN1 = 0, GAIN2 = 1		10.5			
		MAX9752A	GAIN1 = 1, GAIN2 = 0		12.0		1	
			GAIN1 = 1, GAIN2 = 1		13.5			
			GAIN1 = 0, GAIN2 = 0		15.0			
			GAIN1 = 0, GAIN2 = 1		16.5			
	A	MAX9752B	GAIN1 = 1, GAIN2 = 0		18.0			
Speaker Amplifier Gain (Note 4)	Av_sp		GAIN1 = 1, GAIN2 = 1		19.5		dB	
			GAIN1 = 0, GAIN2 = 0		6.0		]	
		NAN/07500	GAIN1 = 0, GAIN2 = 1		7.5			
		MAX9752C	GAIN1 = 1, GAIN2 = 0		9.0			
			GAIN1 = 1, GAIN2 = 1		10.5			
			GAIN = 1		9.0		1	
		MAX9753/MAX9754	GAIN = 0		10.5		İ	
	Pout_sp	f = 1  kHz,  THD+N = 1%, T <sub>A</sub> = +25°C, R <sub>I</sub> = 8Ω	MAX9752A, MAX9752B, MAX9753, MAX9754		1.3		- W	
		11[ - 022	MAX9752C		0.8			
Output Power		$f = 1 \text{ kHz}, \text{ THD+N}$ $= 1\%, \text{ T}_{\text{A}} = +25^{\circ}\text{C},$ $\text{R}_{\text{I}} = 4\Omega$	MAX9752A, MAX9752B, MAX9753, MAX9754		2.2			
		11[ - 422	MAX9752C	1.7				
Total Harmonic Distortion Plus			, $R_L = 8\Omega$		0.023		0/	
Noise	THD+N	$f = 1 kHz, P_{OUT} = 1 W$	$R_L = 4\Omega$		0.03		%	
	0115	$P_{OUT} = 1W, f = 1kHz$	z, Unweighted		90		10	
Signal-to-Noise Ratio	SNR	BW = 22Hz to $22kHz$			91		dB	
	14	Into shutdown			-47			
Click-and-Pop Level (Note 5)	KCP	Out of shutdown			-34		dBV	
Capacitive-Load Drive	CL_MAX	Differential			200		рF	
Switching Frequency	fsw			1000	1200	1400	kHz	
Crosstalk		Channel to channel, $f = 10kHz$ , $P_{OUT} = 1W$			70		dB	
Off-Isolation		MAX9753, unselecte input, f = 10kHz	ed input to any active		70		dB	
Efficiency	η	$R_L = 8\Omega$ , $P_{OUT} = 1W$	/, f = 1kHz		85		%	

## **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = +5.0V, GND = PGND = HPGND = 0V, V_{\overline{SHDN}} = V_{DD}, CPV_{SS} = V_{SS}, C_{BIAS} = 1\mu F, C_{CPVSS} = 1\mu F, C1 = 1\mu F, speaker impedance = 8\Omega connected between OUT_+ and OUT_-, headphone load is terminated to GND; MAX9752: GAIN1 = GAIN2 = 0, V_{VOL} = 0V; MAX9753: GAIN = 0, V_{\overline{A}/B} = 0V; MAX9754: GAIN = 0; T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
HEADPHONE AMPLIFIER (HPS	= V <sub>DD</sub> )	•					
		$T_A = +25^{\circ}C$			±0.5	±3.5	
Output Offset Voltage	Vos	$T_A = T_{MIN}$ to $T_{MAX}$				±8	mV
		MAX9752,	GAIN2 = 0		0		
Maximum Headphone Amplifier	A	GAIN1 = don't care	GAIN2 = 1		3		dB
Gain (Note 6)	Av_hp	MAX9753/MAX9754	GAIN = 1		0		uБ
		WAA9755/WAA9754	GAIN = 0		3		
		$HPV_{DD}$ or $V_{DD} = 3V$ to	5.5V, T <sub>A</sub> = +25°C	66	73		
Power-Supply Rejection Ratio (Note 3)	PSRR	$f = 1 kHz, V_{RIPPLE} = 100$	)mV <sub>P-P</sub>		80		dB
		$f = 10kHz, V_{RIPPLE} = 10$	00mV <sub>P-P</sub>		60		
Output Power	Pour up	THD+N = 1%, f <sub>IN</sub> =	$R_L = 32\Omega$		31		mW
Output Power	Pout_hp	1kHz, $T_A = +25^{\circ}C$	$R_L = 16\Omega$		62		11100
Total Harmonic Distortion Plus	THD+N	f <sub>IN</sub> = 1kHz	$R_L = 32\Omega$ , $P_{OUT} = 31mW$		0.005		%
Noise			$\begin{array}{l} R_{L} = 16\Omega, \\ P_{OUT} = 62 \mathrm{mW} \end{array}$		0.005		
Signal-to-Noise Ratio	SNR	$\label{eq:RL} \begin{array}{l} R_{L} = 32\Omega, \\ P_{OUT} = 31 \text{mW}, \\ f_{IN} = 1 \text{kHz}, \\ BW = 22 \text{Hz} \text{ to } 22 \text{kHz} \end{array}$	Unweighted		95		
			A-weighted		101		dB
		Into shutdown			-33		
Click-and-Pop Level (Note 7)	KCP	Out of shutdown			-37		dBV
Capacitive-Load Drive	CL_MAX	No sustained oscillation	IS		300		рF
Crosstalk		$f = 10$ kHz, $P_{OUT} = 62$ m	W, $R_L = 16\Omega$		60		dB
Off-Isolation		MAX9753, unselected i input, f = 10kHz	nput to any active		60		dB
Slew Rate	SR				0.8		V/µs
Output Impedance		HPS = GND (disabled)			1		kΩ
CHARGE PUMP	•						•
Charge-Pump Frequency	fCP			540	600	660	kHz
VOLUME CONTROL (MAX9752	Only)						
VOL Input Impedance	R <sub>VOL</sub>				100		MΩ
VOL Input Hysteresis	HYST <sub>VOL</sub>	V <sub>VOL</sub> falling			50		mV
Full Mute Input Voltage	V <sub>VOL_MUTE</sub>				0.858 x V <sub>DD</sub>		V
Full Mute Attenuation	AV_MUTE	f <sub>IN</sub> = 1kHz			-85		dB
		I		1			



## **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = +5.0V, GND = PGND = HPGND = 0V, V_{\overline{SHDN}} = V_{DD}, CPV_{SS} = V_{SS}, C_{BIAS} = 1\mu F, C_{CPVSS} = 1\mu F, C1 = 1\mu F, speaker impedance = 8\Omega connected between OUT_+ and OUT_-, headphone load is terminated to GND; MAX9752: GAIN1 = GAIN2 = 0, V_{VOL} = 0V; MAX9753: GAIN = 0, V_{\overline{A}/B} = 0V; MAX9754: GAIN = 0; T_A = T_{MIN}$  to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T\_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
		Gain 10.5dB to 13.5dB		±0.2		
		Gain 6.0dB to 10.0dB		±0.2		
Channel Matching		Gain -26dB to +4.0dB		±0.3		dB
		Gain -62dB to +30dB		±1.0		1
BEEP INPUT (MAX9752 Only)						
Beep Signal Minimum Amplitude (Note 8)	VBEEP	$R_{\text{BEEP}} = 47 k\Omega \qquad 400$			mV	
Beep Signal Minimum Frequency	fBEEP		300			Hz
LOGIC INPUTS (GAIN_, IN1/2, SH	IDN, HPS)					•
Input High Voltage	VIH		2.0			V
Input Low Voltage	VIL				0.8	V
		GAIN_, SHDN	-1		+1	
Input Leakage Current	ILEAK	IN1/2	-2		+2	μΑ
		HPS	-20		+1	

**Note 1:** All devices are 100% production tested at  $T_A = +25$ °C. All temperature limits are guaranteed by design.

Note 2: Speaker amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For  $R_L = 4\Omega$ ,  $L = 33\mu$ H. For  $R_L = 8\Omega$ ,  $L = 68\mu$ H.

Note 3: Measured with the amplifier input connected to GND through  $C_{\text{IN}}$ .

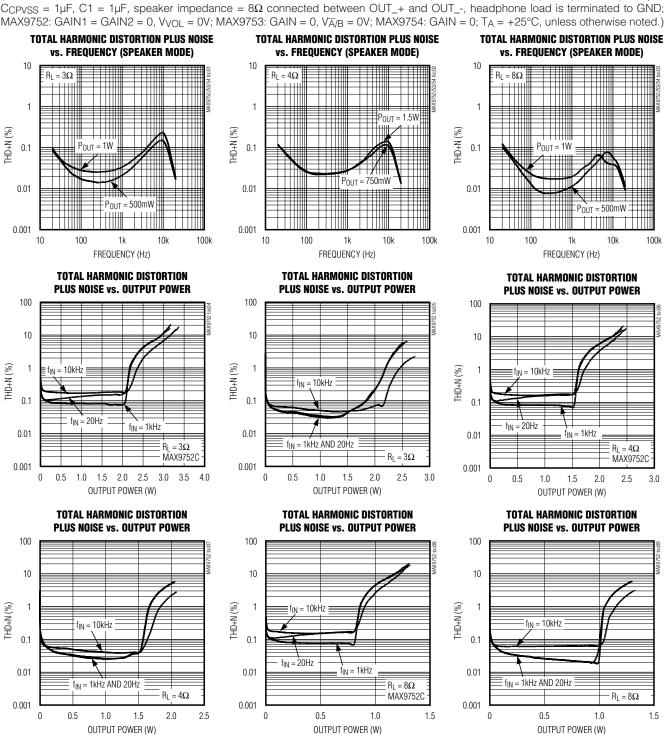
**Note 4:** Speaker amplifier gain is defined as  $A = (V_{OUT_+} - V_{OUT_-}) / V_{IN_-}$ .

Note 5: Testing performed with 8Ω resistive load in series with 68µH inductive load connected across the BTL output. Mode transitions are controlled by SHDN. Peak reading, THD+N = 1%, A-weighted, 32 samples per second. K<sub>CP</sub> level is calculated as: 20 x log[(peak voltage under normal operation at rated power level) / (peak voltage during mode transition, no input signal)].

**Note 6:** Headphone amplifier gain is defined as  $A = V_{HP} / V_{IN}$ .

Note 7: Testing performed with  $32\Omega$  resistive load connected from HP\_ output to GND. Mode transitions are controlled by SHDN. Peak reading, THD+N = 1%, A-weighted, 32 samples per second. K<sub>CP</sub> level is calculated as:

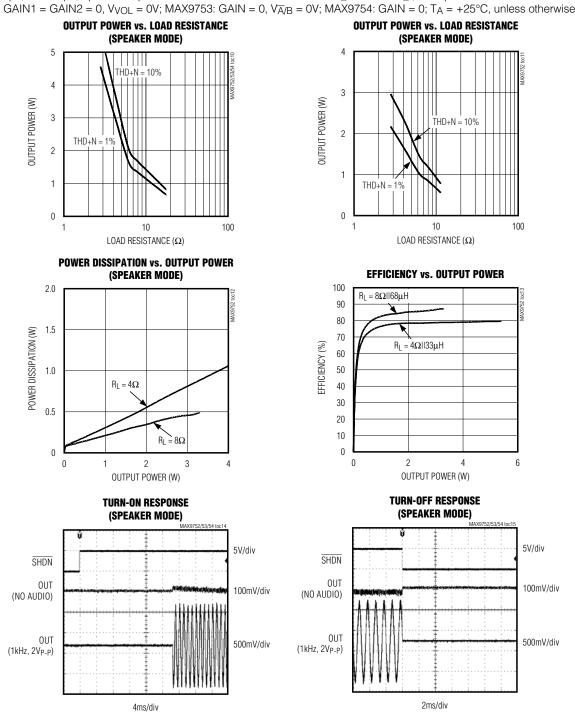
20 x log[(peak voltage under normal operation at rated power level) / (peak voltage during mode transition, no input signal)]. **Note 8:** The value of R<sub>BEEP</sub> dictates the minimum beep signal amplitude that is detected (see the *Beep Input (MAX9752)* section).



## **Typical Operating Characteristics** (VDD = PVDD = HPVDD = CPVDD = 5.0V, GND = PGND = HPGND = 0V, V<u>SHDN</u> = VDD, CPVSS = VSS, CBIAS = 1µF,

\_\_\_\_\_

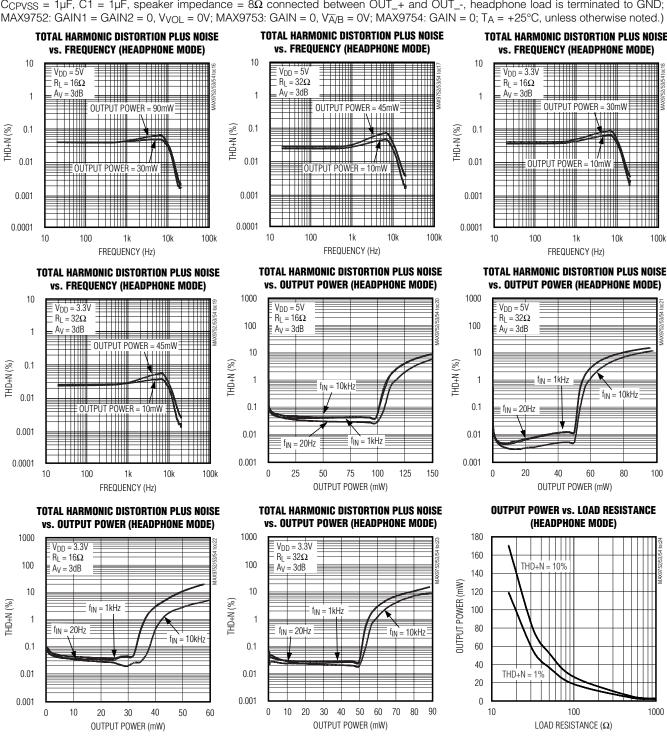
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## **Typical Operating Characteristics (continued)**

 $(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = 5.0V, GND = PGND = HPGND = 0V, V_{\overline{SHDN}} = V_{DD}, CPV_{SS} = V_{SS}, C_{BIAS} = 1\mu F, C_{DV} = 0, C_{DV$ 



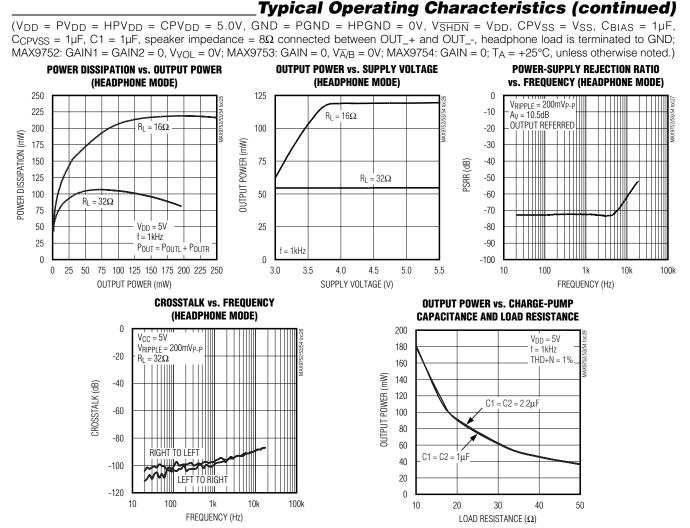


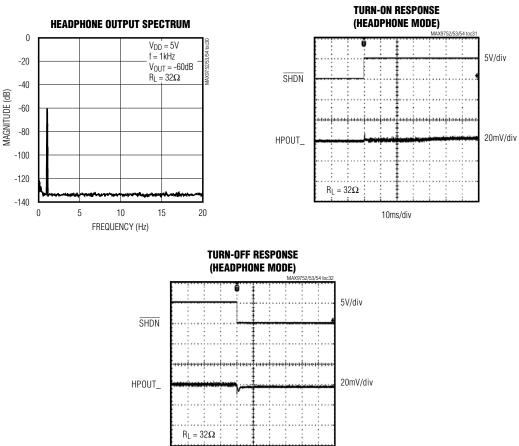
## Typical Operating Characteristics (continued) (VDD = PVDD = HPVDD = CPVDD = 5.0V, GND = PGND = HPGND = 0V, VSHDN = VDD, CPVSS = VSS, CBIAS = 1µF,

C<sub>CPVSS</sub> = 1μF, C1 = 1μF, speaker impedance = 8Ω connected between OUT\_+ and OUT\_-, headphone load is terminated to GND; TOTAL HARMONIC DISTORTION PLUS NOISE



/N/IXI/N





## **Typical Operating Characteristics (continued)**

 $(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = 5.0V, \text{ GND} = PGND = HPGND = 0V, V_{\overline{SHDN}} = V_{DD}, CPV_{SS} = V_{SS}, C_{BIAS} = 1\mu F, C_{CPVSS} = 1\mu F, C_1 = 1\mu F, \text{speaker impedance} = 8\Omega \text{ connected between OUT_+ and OUT_-, headphone load is terminated to GND;} MAX9752: GAIN1 = GAIN2 = 0, V_{VOL} = 0V; MAX9753: GAIN = 0, V_{\overline{A}/B} = 0V; MAX9754: GAIN = 0; T_A = +25^{\circ}C, unless otherwise noted.)$ 

10ms/div

## \_Pin Descriptions

	PIN				
MAX9752	MAX9753	MAX9754	NAME	FUNCTION	
1	_	2	INL	Left-Channel Audio Input	
2		_	BEEP	Audible Alert Beep Input	
3, 19	3, 19	3, 19	PGND	Power Ground	
4	4	4	OUTL+	Left-Channel Positive Speaker Output	
5	5	5	OUTL-	Left-Channel Negative Speaker Output	
6, 16	6, 16	6, 16	PVDD	Speaker Amplifier Power Supply	
7	7	7	CPVDD	Charge-Pump Power Supply	
8	8	8	C1P	Charge-Pump Flying-Capacitor Positive Terminal	
9	9	9	CPGND	Charge-Pump Ground	
10	10	10	C1N	Charge-Pump Flying-Capacitor Negative Terminal	
11	11	11	CPVSS	Charge-Pump Output. Connect to VSS.	
12	12	12	V <sub>SS</sub>	Headphone Amplifier Negative Power Supply	
13	13	13	HPOUTR	Right-Channel Headphone Output	
14	14	14	HPOUTL	Left-Channel Headphone Output	
15	15	15	HPVDD	Headphone Positive Power Supply	
17	17	17	OUTR-	Right-Channel Negative Speaker Output	
18	18	18	OUTR+	Right-Channel Positive Speaker Output	
20	20	20	HPS	Headphone Sense Input	
21	21	21	BIAS	Common-Mode Bias Voltage. Bypass with a 1µF capacitor to GND.	
22	22	22	SHDN	Shutdown. Drive $\overline{SHDN}$ low to disable the device. Connect $\overline{SHDN}$ to $V_{DD}$ for normal operation.	
23		_	GAIN2	Gain-Control Input 2	
24		_	GAIN1	Gain-Control Input 1	
25	25	25	V <sub>DD</sub>	Power Supply	
26	26	23, 26	GND	Ground	
27		28	INR	Right-Channel Audio Input	
28		_	VOL	Analog Volume Control Input	
_	1		INL1	Left-Channel Audio Input 1	
_	2	—	INL2	Left-Channel Audio Input 2	
_	23		IN1/2	Input Select	
_	24	24	GAIN	Gain Select	
_	27	_	INR1	Right-Channel Audio Input 1	
_	28	—	INR2	Right-Channel Audio Input 2	
_	_	1, 27	N.C.	No Connection. Not internally connected.	

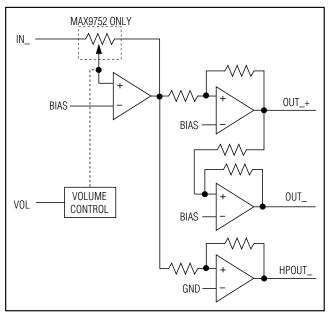


Figure 1. MAX9752/MAX9753/MAX9754 Signal Path

## **Detailed Description**

The MAX9752/MAX9753/MAX9754 combine a 2.2W, Class D speaker amplifier and a 62mW DirectDrive headphone amplifier with integrated headphone sensing and comprehensive click-and-pop suppression. The speaker amplifiers offer Class AB performance with Class D efficiency, while occupying minimal board space. A unique filterless modulation scheme and spread-spectrum switching create a compact, flexible, low-noise, efficient audio power amplifier.

The MAX9752 features an analog volume control, BEEP input, and four-level gain control. The MAX9753 features a 2:1 input stereo multiplexer and two-level gain control. The MAX9754 has only the Class D amplifiers and the headphone amplifiers.

An input amplifier sets the gain of the signal path, and feeds both the speaker and headphone amplifier (Figure 1). The speaker amplifier uses a low-EMI, Class D architecture to drive the speakers, eliminating the need for an external filter for short speaker cables.

The headphone amplifiers use Maxim's patented DirectDrive architecture eliminating the bulky output DCblocking capacitors required by traditional headphone amplifiers. A charge pump inverts the positive supply (CPV<sub>DD</sub>), creating a negative supply (CPV<sub>SS</sub>). The headphone amplifiers operate from these bipolar supplies with their outputs biased about GND (Figure 2). The

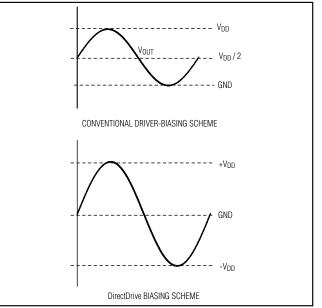


Figure 2. Traditional Amplifier Output vs. DirectDrive Output

amplifiers have almost twice the supply range compared to other single-supply amplifiers, nearly quadrupling the available output power. The benefit of the GND bias is that the amplifier outputs no longer have a DC component (typically  $V_{DD}$  / 2). This eliminates the large DC-blocking capacitors required with conventional headphone amplifiers, removing the dominant source of click and pop, conserving board space, system cost, and improving frequency response.

An undervoltage lockout prevents operation from an insufficient power supply. The amplifiers include thermal-overload and short-circuit protection, and can withstand  $\pm 8kV$  ESD strikes on the headphone amplifier outputs (IEC Air-Gap Discharge). An additional feature of the speaker amplifiers is that there is no phase inversion from input to output.

### **Class D Speaker Amplifier**

The MAX9752/MAX9753/MAX9754 feature a unique, patented spread-spectrum mode that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables. The switching frequency varies randomly by ±90kHz around the center frequency (1200kHz). Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes (Figure 3).





WHIL HAVEN

180

200

220

240

280

260

300

FREQUENCY (MHz)

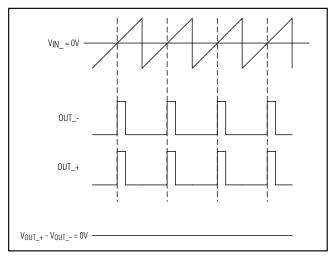
120

140

160

100

Figure 3. MAX9752/MAX9753/MAX9754 Radiated Emissions with 76mm of Speaker Cable



60

80

30 25

Figure 4. Second-Generation Class D Output Waveform with No Signal

### Filterless Modulation/Common-Mode Idle

The MAX9752/MAX9753/MAX9754 use Maxim's unique, patented modulation scheme that eliminates the LC filter required by traditional Class D amplifiers, improving efficiency, reducing component count, and conserving board space and system cost (Figure 4). With no input signal, the outputs are two low-duty-cycle pulses that are in-phase. This lowers the high-frequency energy and spectral content. In comparison, conventional Class D amplifiers output a 50% duty cycle when no input signal is present. For most applications with short speaker cables, no filtering is required.

**EFFICIENCY vs. OUTPUT POWER** 100 MAX9752 90 MAX9753 MAX9754 80 70 EFFICIENCY (%) 60 50 40 30 CLASS AB 20 10  $R_L = 8\Omega$ 0 0.5 0 1.0 1.5 20 OUTPUT POWER (W)

Figure 5. MAX9752/MAX9753/MAX9754 Class D Efficiency vs. MAX9750/MAX9751/MAX9755 Class AB Efficiency

### Efficiency

Efficiency of a Class D amplifier is attributed to the region of operation of the output stage transistors. In a Class D amplifier, the output transistors act as switches and consume negligible power. Any power loss associated with the Class D output stage is mostly due to the I<sup>2</sup>R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%. however, that efficiency is only exhibited at peak output powers. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9752/MAX9753/MAX9754 still exhibit > 80% efficiencies under the same conditions (Figure 5).

M/XI/M

### Headphone Amplifier DirectDrive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block the DC bias from the headphones.

Maxim's patented DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the MAX9752/MAX9753/MAX9754 headphone amplifier output to be biased about GND, almost doubling the dynamic range, while operating from a single supply. With no DC component, there is no need for the large DCblocking capacitors. Instead of two large capacitors (220µF, typ), the charge pump requires only two small ceramic capacitors (1µF typ), conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor values.

Previous attempts to eliminate the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raised some issues:

- The sleeve is typically grounded to the chassis. Using this biasing approach, the sleeve must be isolated from system ground, complicating product design.
- 2) During an ESD strike, the amplifier's ESD structures are the only path to system ground. The amplifier must be able to withstand the full ESD strike.

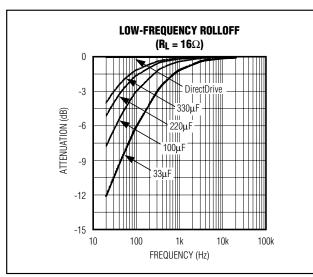


Figure 6. Low-Frequency Attenuation of Common DC-Blocking Capacitor Values

3) When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in large ground-loop current and possible damage to the amplifiers.

#### Low-Frequency Response

In addition to the cost and size disadvantages, the DCblocking capacitors limit the low-frequency response of the amplifier and distort the audio signal:

 The impedance of the headphone load and the DCblocking capacitor form a highpass filter with the -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

where  $R_L$  is the impedance of the headphone and  $C_{OUT}$  is the value of the DC-blocking capacitor.

The highpass filter is required by conventional singleended, single-supply headphone amplifiers to block the midrail DC component of the audio signal from the headphones. Depending on the -3dB point, the filter can attenuate low-frequency signals within the audio band. Larger values of C<sub>OUT</sub> reduce the attenuation, but are physically larger, more expensive capacitors. Figure 6 shows the relationship between the size of C<sub>OUT</sub> and the resulting low-frequency attenuation. Note the -3dB point for a 16 $\Omega$  headphone with a 100µF blocking capacitor is 100Hz, well within the audio band.

2) The voltage coefficient of the capacitor, the change in capacitance due to a change in the voltage across the capacitor, distorts the audio signal. At frequencies around the -3dB point, the reactance of the capacitor dominates, and the voltage coefficient appears as frequency-dependent distortion. Figure 7 shows the THD+N introduced by two different capacitor dielectrics. Note that around the -3dB point, THD+N increases dramatically.

The combination of low-frequency attenuation and frequency-dependent distortion compromises audio reproduction. DirectDrive improves low-frequency reproduction in portable audio equipment that emphasizes low-frequency effects such as multi-media laptops, MP3, CD, and DVD players.



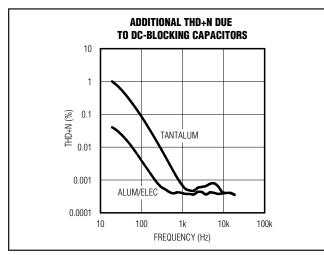


Figure 7. Distortion Contributed by DC-Blocking Capacitors

## Table 1. MAX9752 Gain Settings

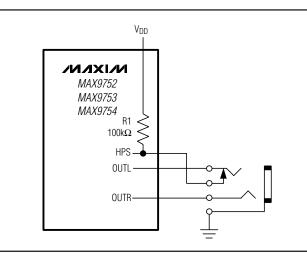


Figure 8. HPS Configuration

GAIN2	GAIN1	SPE	AKER MODE GAIN	(dB)	HEADPHONE MODE GAIN (dB)	
GAINZ	GAINT	MAX9752A	MAX9752B	MAX9752C		
0	0	9.0	15.0	6.0	0	
0	1	10.5	16.5	7.5	0	
1	0	12.0	18.0	9.0	3	
1	1	13.5	19.5	10.5	3	

### Charge Pump

The MAX9752/MAX9753/MAX9754 feature a low-noise charge pump. The 600kHz switching frequency is well beyond the audio range, and does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Limiting the switching speed of the charge pump minimizes the di/dt noise caused by the parasitic bond wire and trace inductance. Although not typically required, additional high-frequency ripple attenuation can be achieved by increasing the size of C2 (see the *Functional Diagrams*).

### Headphone Sense Input (HPS)

The headphone sense input (HPS) monitors the headphone jack, and automatically configures the device based upon the voltage applied at HPS. A voltage of less than 0.8V sets the device to speaker mode. A voltage of greater than 2V disables the speaker amplifiers and enables the headphone amplifiers.

For automatic headphone detection, connect HPS to the control pin of a 3-wire headphone jack as shown in Figure 8. With no headphone present, the output imped-

ance of the headphone amplifier pulls HPS low. When a headphone plug is inserted into the jack, the control pin is disconnected from the tip contact and HPS is pulled to  $V_{DD}$  through the internal 100k $\Omega$  pullup resistor.

### Bias

The MAX9752/MAX9753/MAX9754 feature an internally generated, power-supply-independent, common-mode bias voltage referenced to GND. BIAS provides both click-and-pop suppression and sets the DC bias level for the amplifiers. Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. No external load should be applied to BIAS.

### Gain Selection MAX9752

The MAX9752 features externally controlled gain with four pin-selectable gain ranges. GAIN1 and GAIN2 set the maximum gain of the MAX9752 speaker and head-phone amplifiers (Table 1). The voltage at VOL varies the gain of the speaker and headphone amplifiers, providing a user-adjusted volume control, see the *Analog Volume Control (VOL, MAX9752)* section.

	_	•	_
GAIN (dB)	INPUT (V <sub>RMS</sub> )	RL (Ω)	Pout (W)
MAX9752A	(11110)	(/	()
9.0	1.004	4	2.0
10.5	0.844	4 4	2.0
		4	
12.0	0.710		2.0
13.5	0.598	4	2.0
9.0	1.099	8	1.2
10.5	0.925	8	1.2
12.0	0.778	8	1.2
13.5	0.655	8	1.2
MAX9752B			
15.0	0.503	4	2.0
16.5	0.423	4	2.0
18.0	0.356	4	2.0
19.5	0.300	4	2.0
15.0	0.551	8	1.2
16.5	0.464	8	1.2
18.0	0.390	8	1.2
19.5	0.328	8	1.2
MAX9752C			
6.0	1.418	4	2.0
7.5	1.193	4	2.0
9.0	1.004	4	2.0
10.5	0.844	4	2.0
6.0	1.553	8	1.2
7.5	1.307	8	1.2
9.0	1.099	8	1.2
10.5	0.925	8	1.2

# Table 2. MAX9752 Speaker Amplifier GainSettings for Maximum Output Power

Table 2 shows the amplifier gain settings needed to attain maximum speaker output power from a given input voltage and load.

### MAX9753/MAX9754

The gain of the MAX9753/MAX9754 is set by GAIN. Drive GAIN high to set the gain of the speaker amplifiers to 9dB, and the gain of the headphone amplifiers to 0dB. Drive GAIN low to set the gain of the speaker amplifiers to 10.5dB, and the gain of the headphone amplifiers to 3dB (Table 3).

# Table 3. MAX9753/MAX9754 MaximumGain Settings

GAIN	SPEAKER MODE GAIN (dB)	HEADPHONE MODE GAIN (dB)
0	10.5	3
1	9.0	0

# Table 4. MAX9753/MAX9754 Input Voltageand Gain Settings for Maximum OutputPower

GAIN (dB)	INPUT (V <sub>RMS</sub> )	<b>RL</b> (Ω)	Роит (W)
10.5	0.844	4	2.0
9.0	1.004	4	2.0
10.5	0.925	8	1.2
9.0	1.099	8	1.2

Table 4 shows the amplifier input voltage needed to attain maximum speaker output power from a given gain setting and load.

Analog Volume Control (VOL, MAX9752) The MAX9752 features an analog volume control that varies the speaker and headphone amplifier's gain in 31 discrete steps based upon the DC voltage applied to VOL. The input range of VOL is from 0 (full volume) to 0.858 x HPVDD (full mute). Example step sizes are shown in Table 5. Control VOL with either a DAC or potentiometer as shown in Figure 9. Because the VOL input is high impedance (typically  $100M\Omega$ ), it can also be driven with an RC-filtered PWM signal. Connect the reference of the DAC or potentiometer to HPVDD. Since the volume control is ratiometric to HPVDD, any changes in HPVDD are negated. The gain step sizes are not constant, the step sizes at the upper extreme are 0.5dB/step, 2.0dB/step in the midrange, and 4.0dB/step at the lower extreme. Figure 10 shows the transfer function of the volume control for  $HPV_{DD} = 3.3V$ .

Vvoi	VVOL (V) FRACT			SPEAKER MO	DE GAIN (dB)		HEADPHONE M	IODE GAIN (dB)
V <sub>MIN</sub> *	VMAX*	OF HPV <sub>DD</sub>	GAIN1 = 0, GAIN2 = 0	GAIN1 = 1, GAIN2 = 0	GAIN1 = 0, GAIN2 = 1	GAIN1 = 1 GAIN2 = 1	GAIN1 = X, GAIN2 = 0	GAIN1 = X, GAIN2 = 1
0	0.4900	0.074	9	10.5	12	13.5	0	3
0.4900	0.5673	0.160	8	10	11.5	13	-1	2.5
0.5673	0.6447	0.183	7	9	11	12.5	-2	2
0.6447	0.7220	0.207	6	8	10.5	12	-3	1.5
0.7220	0.7994	0.230	4	7	10	11.5	-5	1
0.7994	0.8767	0.253	2	6	9	11	-7	0
0.8767	0.9541	0.277	0	4	8	10.5	-9	-1
0.9541	1.0314	0.300	-2	2	7	10	-11	-2
1.0314	1.1088	0.324	-4	0	6	9	-13	-3
1.1088	1.1861	0.347	-6	-2	4	8	-15	-5
1.1861	1.2635	0.371	-8	-4	2	7	-17	-7
1.2635	1.3408	0.394	-10	-6	0	6	-19	-9
1.3408	1.4182	0.418	-12	-8	-2	4	-21	-11
1.4182	1.4955	0.441	-14	-10	-4	2	-23	-13
1.4955	1.5728	0.464	-16	-12	-6	0	-25	-15
1.5728	1.6502	0.488	-18	-14	-8	-2	-27	-17
1.6502	1.7275	0.511	-20	-16	-10	-4	-29	-19
1.7275	1.8049	0.535	-22	-18	-12	-6	-31	-21
1.8094	1.8822	0.558	-24	-20	-14	-8	-33	-23
1.8822	1.9596	0.582	-26	-22	-16	-10	-35	-25
1.9596	2.0369	0.605	-28	-24	-18	-12	-37	-27
2.0369	2.1143	0.628	-30	-26	-20	-14	-39	-29
2.1143	2.1916	0.652	-32	-28	-22	-16	-41	-31
2.1916	2.2690	0.675	-34	-30	-24	-18	-43	-33
2.2690	2.3463	0.699	-38	-32	-26	-20	-47	-35
2.3463	2.4237	0.722	-42	-34	-28	-22	-51	-37
2.4237	2.5010	0.746	-46	-38	-30	-24	-55	-39
2.5010	2.5783	0.769	-50	-42	-32	-26	-59	-41
2.5783	2.6557	0.793	-54	-46	-34	-28	-63	-43
2.6557	2.7330	0.816	-58	-50	-38	-30	-67	-47
2.7330	2.8104	0.839	-62	-54	-42	-32	-71	-51
2.8104	3.3000	0.858	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

## Table 5a. MAX9752A Volume Levels

\*Based on HPV<sub>DD</sub> = 3.3V.

X = Don't care.

Vvoi	_ (V)	FRACTION		SPEAKER MC	DE GAIN (dB)			IODE GAIN (dB)
V <sub>MIN</sub> *	VMAX*	OF HPV <sub>DD</sub>	GAIN1 = 0, GAIN2 = 0	GAIN1 = 1, GAIN2 = 0	GAIN1 = 0, GAIN2 = 1	GAIN1 = 1 GAIN2 = 1	GAIN1 = X, GAIN2 = 0	GAIN1 = X, GAIN2 = 1
0	0.4900	0.074	15	16.5	18	19.5	0	3
0.4900	0.5673	0.160	14	16	17.5	19	-1	2.5
0.5673	0.6447	0.183	13	15	17	18.5	-2	2
0.6447	0.7220	0.207	12	14	16.5	18	-3	1.5
0.7220	0.7994	0.230	10	13	16	17.5	-5	1
0.7994	0.8767	0.253	8	12	15	17	-7	0
0.8767	0.9541	0.277	6	10	14	16.5	-9	-1
0.9541	1.0314	0.300	4	8	13	16	-11	-2
1.0314	1.1088	0.324	2	6	12	15	-13	-3
1.1088	1.1861	0.347	0	4	10	14	-15	-5
1.1861	1.2635	0.371	-2	2	8	13	-17	-7
1.2635	1.3408	0.394	-4	0	6	12	-19	-9
1.3408	1.4182	0.418	-6	-2	4	10	-21	-11
1.4182	1.4955	0.441	-8	-4	2	8	-23	-13
1.4955	1.5728	0.464	-10	-6	0	6	-25	-15
1.5728	1.6502	0.488	-12	-8	-2	4	-27	-17
1.6502	1.7275	0.511	-14	-10	-4	2	-29	-19
1.7275	1.8049	0.535	-16	-12	-6	0	-31	-21
1.8049	1.8822	0.558	-18	-14	-8	-2	-33	-23
1.8822	1.9596	0.582	-20	-16	-10	-4	-35	-25
1.9596	2.0369	0.605	-22	-18	-12	-6	-37	-27
2.0369	2.1143	0.628	-24	-20	-14	-8	-39	-29
2.1143	2.1916	0.652	-26	-22	-16	-10	-41	-31
2.1916	2.2690	0.675	-28	-24	-18	-12	-43	-33
2.2690	2.3463	0.699	-32	-26	-20	-14	-47	-35
2.3463	2.4237	0.722	-36	-28	-22	-16	-51	-37
2.4237	2.5010	0.746	-40	-32	-24	-18	-55	-39
2.5010	2.5783	0.769	-44	-36	-26	-20	-59	-41
2.5783	2.6557	0.793	-48	-40	-28	-22	-63	-43
2.6557	2.7330	0.816	-52	-44	-32	-24	-67	-47
2.7330	2.8104	0.839	-56	-48	-36	-26	-71	-51
2.8104	3.3000	0.858	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

## Table 5b. MAX9752B Volume Levels

\*Based on  $HPV_{DD} = 3.3V$ .

X = Don't care.

Vvol	_ (V)	FRACTION		SPEAKER MC		IODE GAIN (dB)		
V <sub>MIN</sub> *	V <sub>MAX</sub> *	OF HPV <sub>DD</sub>	GAIN1 = 0, GAIN2 = 0	GAIN1 = 1, GAIN2 = 0	GAIN1 = 0, GAIN2 = 1	GAIN1 = 1 GAIN2 = 1	GAIN1 = X, GAIN2 = 0	GAIN1 = X, GAIN2 = 1
0	0.4900	0.074	6	7.5	9	10.5	0	3
0.4900	0.5673	0.160	5	7	8.5	10	-1	2.5
0.5673	0.6447	0.183	4	6	8	9.5	-2	2
0.6447	0.7220	0.207	3	5	7.5	9	-3	1.5
0.7220	0.7994	0.230	1	4	7	8.5	-5	1
0.7994	0.8767	0.253	-1	3	6	8	-7	0
0.8767	0.9541	0.277	-3	1	5	7.5	-9	-1
0.9541	1.0314	0.300	-5	-1	4	7	-11	-2
1.0314	1.1088	0.324	-7	-3	3	6	-13	-3
1.1088	1.1861	0.347	-9	-5	1	5	-15	-5
1.1861	1.2635	0.371	-11	-7	-1	4	-17	-7
1.2635	1.3408	0.394	-13	-9	-3	3	-19	-9
1.3408	1.4182	0.418	-15	-11	-5	1	-21	-11
1.4182	1.4955	0.441	-17	-13	-7	-1	-23	-13
1.4955	1.5728	0.464	-19	-15	-9	-3	-25	-15
1.5728	1.6502	0.488	-21	-17	-11	-5	-27	-17
1.6502	1.7275	0.511	-23	-19	-13	-7	-29	-19
1.7275	1.8049	0.535	-25	-21	-15	-9	-31	-21
1.8049	1.8822	0.558	-27	-23	-17	-11	-33	-23
1.8822	1.9596	0.582	-29	-25	-9	-13	-35	-25
1.9596	2.0369	0.605	-31	-27	-21	-15	-37	-27
2.0369	2.1143	0.628	-33	-29	-23	-17	-39	-29
2.1143	2.1916	0.652	-35	-31	-2	-19	-41	-31
2.1916	2.2690	0.675	-37	-3	-27	-21	-43	-33
2.2690	2.3463	0.699	-41	-35	-29	-23	-47	-35
2.3463	2.4237	0.722	-45	-37	-31	-25	-51	-37
2.4237	2.5010	0.746	-48	-41	-33	-27	-55	-39
2.5010	2.5783	0.769	-53	-45	-35	-29	-59	-41
2.5783	2.6557	0.793	-57	-49	-37	-31	-63	-43
2.6557	2.7330	0.816	-61	-53	-41	-33	-67	-47
2.7330	2.8104	0.839	-65	-57	-45	-35	-71	-51
2.8104	3.3000	0.858	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

## Table 5c. MAX9752C Volume Levels

\*Based on  $HPV_{DD} = 3.3V$ . X = Don't care.

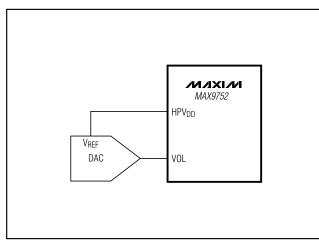


Figure 9. MAX9752 Volume-Control Circuit

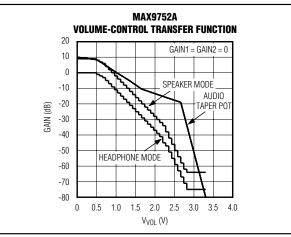


Figure 10a. MAX9752A Volume-Control Transfer Functions

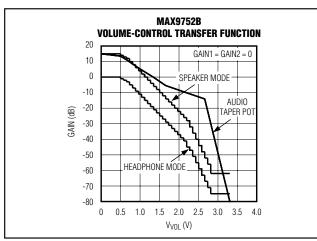


Figure 10b. MAX9752B Volume-Control Transfer Functions

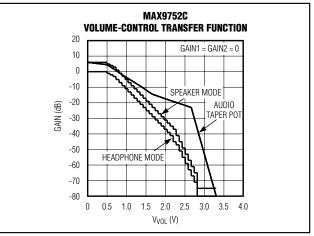


Figure 10c. MAX9752C Volume-Control Transfer Functions

### **Beep Input (MAX9752)**

The MAX9752 features an audible alert beep input (BEEP). BEEP serves as the alert signal detector and the alert input to the amplifiers. AC-couple the alert output of a µC to BEEP. The MAX9752 monitors the signal at BEEP. When a signal exceeding 400mVP-P with a frequency greater than 300Hz is detected at BEEP, the MAX9752 connects the signal to the amplifiers after eight periods of the input signal. In speaker mode, the alert signal appears at both speaker outputs, mixed with any audio that may be present. In headphone mode, the alert signal appears at the headphone outputs, mixed with any audio that may be present. A signal with less than eight input periods is ignored. Multiple BEEP signals can be summed as shown in Figure 11. Adding external resistors in series with BEEP increase the minimum voltage amplitude sensitivity.

## Input Mux (MAX9753)

The MAX9753 features a 2:1 input multiplexer on each amplifier, allowing input selection between two stereo sources. The logic input IN1/2 controls both multiplexers. A logic-high selects input IN\_1 and a logic-low selects input IN\_2. The unselected inputs are high impedance.

### Shutdown

The MAX9752/MAX9753/MAX9754 feature an 8µA, lowpower shutdown mode reducing quiescent current consumption and extending battery life. Driving SHDN low disables the drive amplifiers, bias circuitry, charge pump, and sets the headphone amplifier output impedance to 1k $\Omega$ , and drives BIAS to GND. Connect SHDN to V<sub>DD</sub> for normal operation.

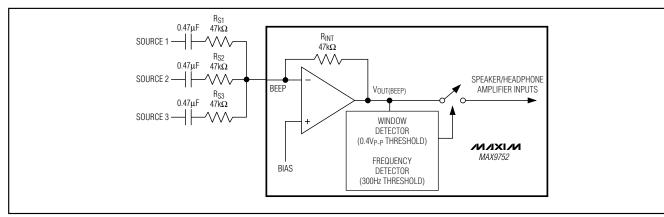


Figure 11. MAX9752 Beep Summing Circuit

### **Click-and-Pop Suppression**

The MAX9752/MAX9753/MAX9754 feature Maxim's comprehensive, industry-leading click-and-pop suppression eliminating audible transients at startup. The Turn-On and Turn-Off Response waveforms in the *Typical Operating Characteristics* show that there are minimal spectral components in the audible range at the output upon startup and shutdown.

## \_Applications Information

### Compatibility with MAX9750/MAX9751/MAX9755

The MAX9752/MAX9753/MAX9754 provide a high-efficiency, Class D speaker driver with very low EMI (see the *Typical Operating Characteristics*). If a Class AB output is desired, the MAX9750/MAX9751/MAX9755 can be substituted. The MAX9750, MAX9751, and MAX9755 are pin-for-pin compatible with the MAX9752, MAX9753, and MAX9754, respectively.

## Filterless Operation

The MAX9752/MAX9753/MAX9754 do not require an output filter in most applications. The devices rely on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Voice coil movement due to the square-wave frequency is very small because the switching frequency is well beyond the bandwidth of speakers. Although this movement is small, a speaker not designed to handle the additional power can be damaged. Use a speaker with a series inductance >  $30\mu$ H for optimum results. Typical  $8\Omega$  speakers exhibit series inductances in the  $30\mu$ H to  $100\mu$ H range. Highest efficiency is achieved with speaker inductances >  $60\mu$ H.

## **Power Dissipation and Heat Sinking**

Because the MAX9752/MAX9753/MAX9754 have highefficiency, Class D speaker drivers, the intrinsic package power dissipation capabilities are sufficient for cooling. No special heatsinking is needed in normal operating conditions.

## **Headphone Amplifier Output Power**

The headphone amplifiers have been specified for the worst-case scenario—when both inputs are in-phase. Under this condition, the drivers simultaneously draw current from the charge pump, leading to a slight loss in headroom of V<sub>SS</sub>. In typical stereo audio applications, the left and right signals have differences in both magnitude and phase, subsequently leading to an increase in the maximum attainable output power. Figure 12 shows the two cases for in- and out-of-phase. In reality, the available power lies between these extremes.

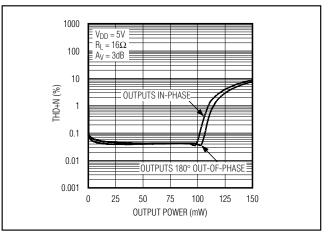


Figure 12. THD+N vs. POUT with Headphone Output Signals In- and Out-of-Phase



**Power Supplies** The MAX9752/MAX9753/MAX9754 have different supplies for each portion of the device allowing for the optimum combination of headroom, power dissipation, and noise immunity. The speaker amplifiers are powered from PVDD. PVDD ranges from 4.5V to 5.5V. The headphone amplifiers are powered from HPVDD and VSS. HPVDD is the positive supply of the headphone amplifiers and ranges from 3V to 5.5V. VSS is the negative supply input for the headphone amplifiers. Connect VSS to CPVSS. The charge pump is powered by CPVDD, which ranges from 3V to 5.5V. CPVDD should be the same potential as HPVDD. The charge pump inverts the voltage at CPVDD, and the resulting voltage appears at CPVSS. The remainder of the device is powered by VDD.

### Component Selection Input Filtering

The input capacitor (C<sub>IN</sub>), in conjunction with the amplifier input resistance (R<sub>IN</sub>), forms a highpass filter that removes the DC bias from an incoming signal (see the *Functional Diagrams*). The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN}C_{IN}}$$

 $R_{IN}$  is the amplifier's internal input resistance value given in the *Electrical Characteristics* table. Choose  $C_{IN}$  so  $f_{\rm -3dB}$  is well below the lowest frequency of interest. Setting  $f_{\rm -3dB}$  too high affects the amplifier's low-frequency response. Use capacitors with low-voltage coefficient dielectrics, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

### **Optional Output Filtering**

In most applications, the low-EMI, Class D outputs do not require output filters. The device passes FCC emissions standards with 76mm of unshielded speaker cables. Output filtering can be used if lower EMI is desired. Use a ferrite bead filter when radiated frequencies above 10MHz are of concern. Use an LC filter when radiated frequencies below 10MHz are of concern, or when long leads (> 76mm) connect the amplifier to the speaker.

### **BIAS Capacitor**

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor, C<sub>BIAS</sub>, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, startup/shutdown, DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 1 $\mu$ F capacitor to GND.

### **Charge-Pump Capacitor Selection**

Use capacitors with less than 100m  $\Omega$  of equivalent series resistance (ESR). Low-ESR ceramic capacitors minimize the output impedance of the charge pump. Capacitors with an X7R dielectric provide the best performance over the extended temperature range.

### Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the load regulation and output resistance of the charge pump. Choosing C1 too small degrades the ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*. Above 2.2µF, the on-resistance of the switches and the ESR of C1 and C2 dominate. The recommended range of capacitors is from  $0.33\mu$ F to  $3.3\mu$ F.

### Output Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at CPV<sub>SS</sub>. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low, maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*. C2 must be greater than or equal to C1. The recommended range of capacitors is from 0.33µF to 3.3µF.

### CPV<sub>DD</sub> Bypass Capacitor

The CPV<sub>DD</sub> bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the charge-pump switching transients on the headphone driver outputs. Bypass CPV<sub>DD</sub> with C3, the same value as C1, and place it physically close to CPV<sub>DD</sub> and PGND.

### Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect CPGND, PGND, and GND together at a single point on the PC board. Route CPGND, PGND, and all traces that carry switching transients away from GND and the traces and components in the audio signal path.



Connect all components associated with the charge pump (C2 and C3) to CPGND. Connect V<sub>SS</sub> and CPV<sub>SS</sub> together at C2. Place the charge-pump capacitors (C1, C2, and C3) as close to the device as possible. Bypass HPV<sub>DD</sub> with 1 $\mu$ F to GND. Bypass PV<sub>DD</sub> with a 0.1 $\mu$ F capacitor and a 100 $\mu$ F capacitor to PGND. Place the bypass capacitors as close to the device as possible.

Use large, low-resistance output traces. Current drawn from the outputs increases as load impedance decreases. High-output-trace resistance decreases the power delivered to the load. For example, when compared to a  $0\Omega$  trace, a  $100m\Omega$  trace reduces the power delivered to a  $4\Omega$  load from 2.1W to 2.0W. Large output, supply, and GND traces allow more heat to move from the MAX9752/MAX9753/MAX9754 to the air, reducing the thermal impedance of the system.

The MAX9752/MAX9753/MAX9754 thin QFN packages feature exposed pads on their undersides. Connect the exposed pad to GND with a large copper pad and multiple vias to the ground plane.

### Measuring Class D Outputs with an Analog Analyzer

Filterless Class D amplifiers use the loudspeaker's coil inductance to filter out switching energy. Additionally, the loudspeaker does not respond to the switching frequency of Class D amplifiers, nor could human ears hear these frequencies. However, audio analyzers and oscilloscopes can detect these signals. On an oscilloscope,

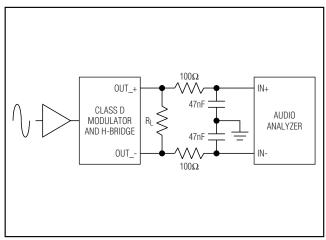
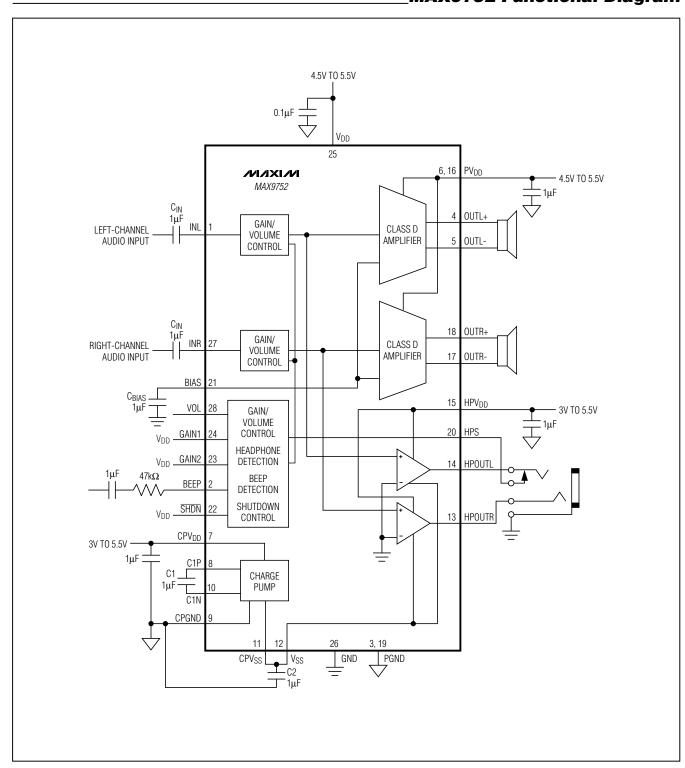


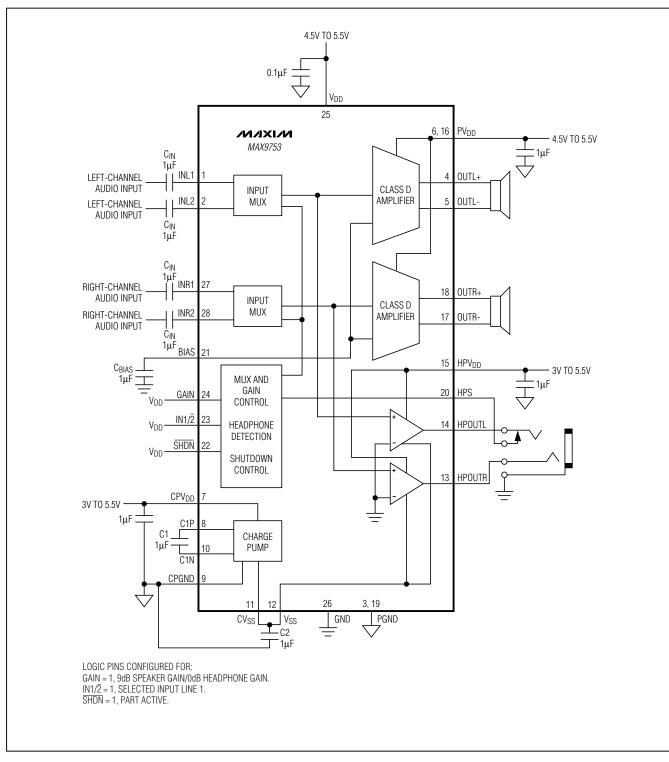
Figure 13. Connecting a Class D Output to an Analog Analyzer

the switching components obscure the audio signal. On an audio analyzer they overload the input signal, degrading the measurement from the true audio performance of the amplifier. A simple RC filter can be used (Figure 13) to aid in evaluation of Class D amplifiers in the lab. This circuit provides a single-pole response at 34kHz, with a minimal insertion loss. More complex designs such as L-C filters can provide more performance, but must be verified to ensure they do not add their own distortion signature to the amplifier's output.

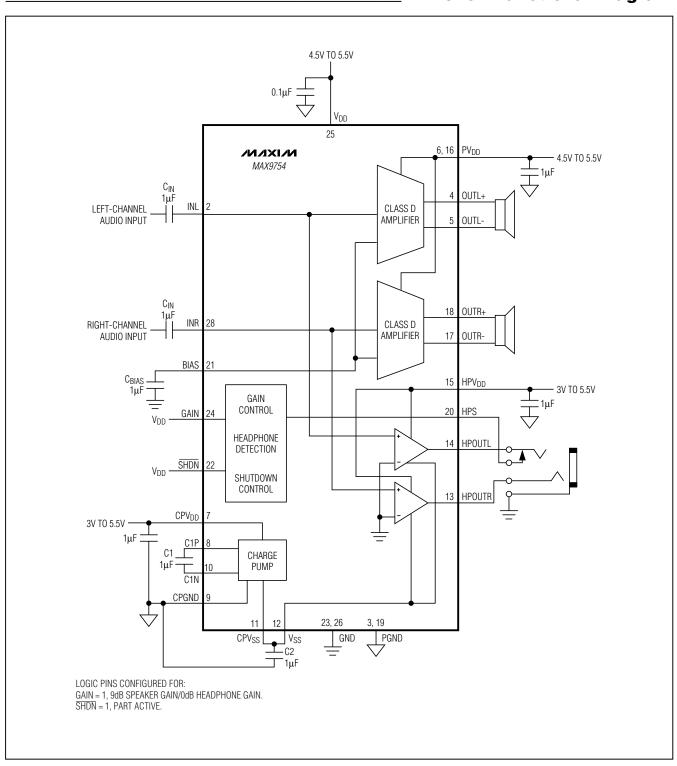


MAX9752/MAX9753/MAX9754

## MAX9753 Functional Diagram

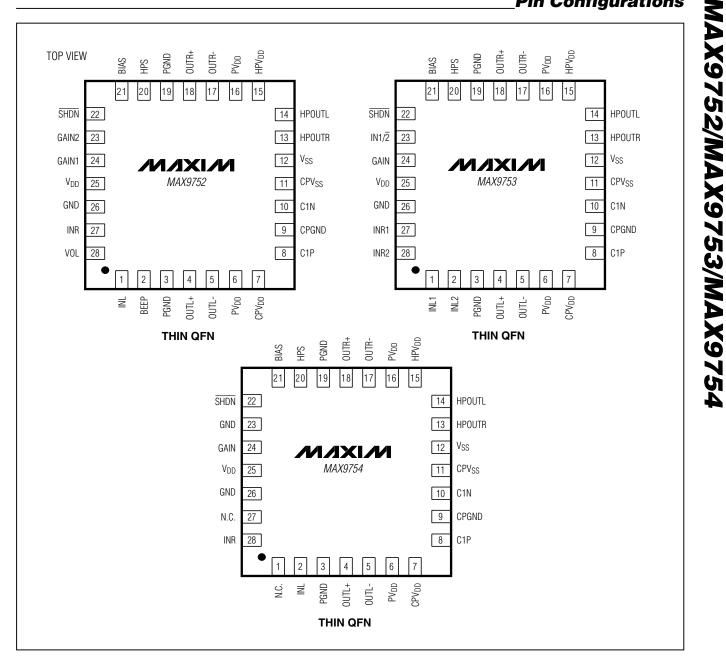


MAX9752/MAX9753/MAX9754



MAX9754 Functional Diagram





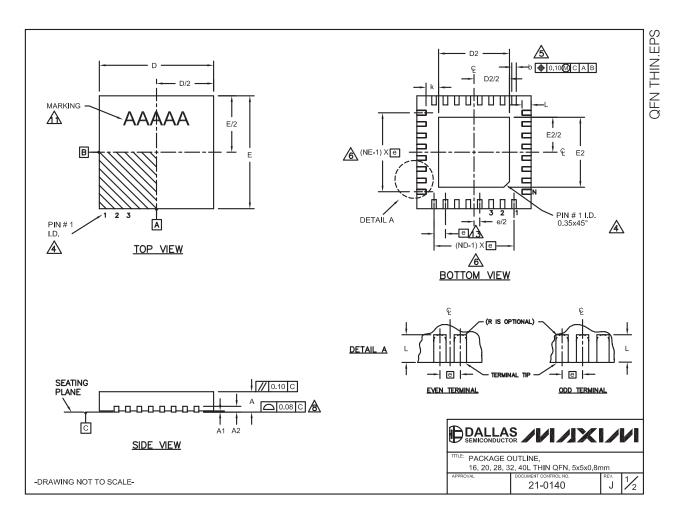
## **Chip Information**

MAX9752 TRANSISTOR COUNT: 12,263 MAX9753/MAX9754 TRANSISTOR COUNT: 12,137 PROCESS: BICMOS

M/X/M

## **Package Information**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to <u>www.maxim-ic.com/packages</u>.)



## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

DIKO		CO	MMON DIM	ENSIO	NS									EXF	POSE		VAR		IS		
PKG.	16L 5x	;	20L 5x5		28L 5x5		32L	5x5		40L 5>	:5	PKG.			D2			E2		1	
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A	0.70 0.75	0.80 0	.70 0.75 0	80 0.7	0 0.75 0	0.880	.70 0.7	75 0.8	0 0.7	0 0.75	0.80	T1655	-2	3.00	3.10	3.20	3.00	3.10	3.20	1	
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b	0.25 0.30											T2055	-3	3.00	3.10	3.20	3.00	3.10	3.20	1	
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ND	4	+	5	-	7	+	8		+	10		T2855	-6	3.15	3.25	3.35	3.15	3.25	3.35	1	
NE	4		5		7		8	3	+	10		T2855	-7	2.60	2.70	2.80	2.60	2.70	2.80	1	
JEDEC	WHHE		WHHC		WHHD-	1	WH	HD-2				T2855	-8	3.15	3.25	3.35	3.15	3.25	3.35	1	
												T2855	N-1	3.15	3.25	3.35	3.15	3.25	3.35	1	
												T3255	-3	3.00	3.10	3.20	3.00	3.10	3.20	1	
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