ASSP
USB3.0-SATA Bridge LSI
MB86C31

● DESCRIPTION

MB86C31 is USB3.0 external storage solution that complies with Universal Serial Bus 3.0 Specification, Revision 1.0, Universal Serial Bus Specification, Revision 2.0 and Serial ATA Specification Revision 2.6. MB86C31 integrates USB3.0 / USB2.0 / SATA Links and PHYs and 32bit RISC processor to respond to the requests from USB host.
This product offers four different lineups of MB86C311A and MB86C311B whose PKG are LQFP-64 and QFN-48. MB86C311A includes an encryption function and MB86C311B does not have an encryption function.

● APPLICATION

USB3.0 External storage

- HDD, SSD, Blu-ray and DVD

● FEATURES

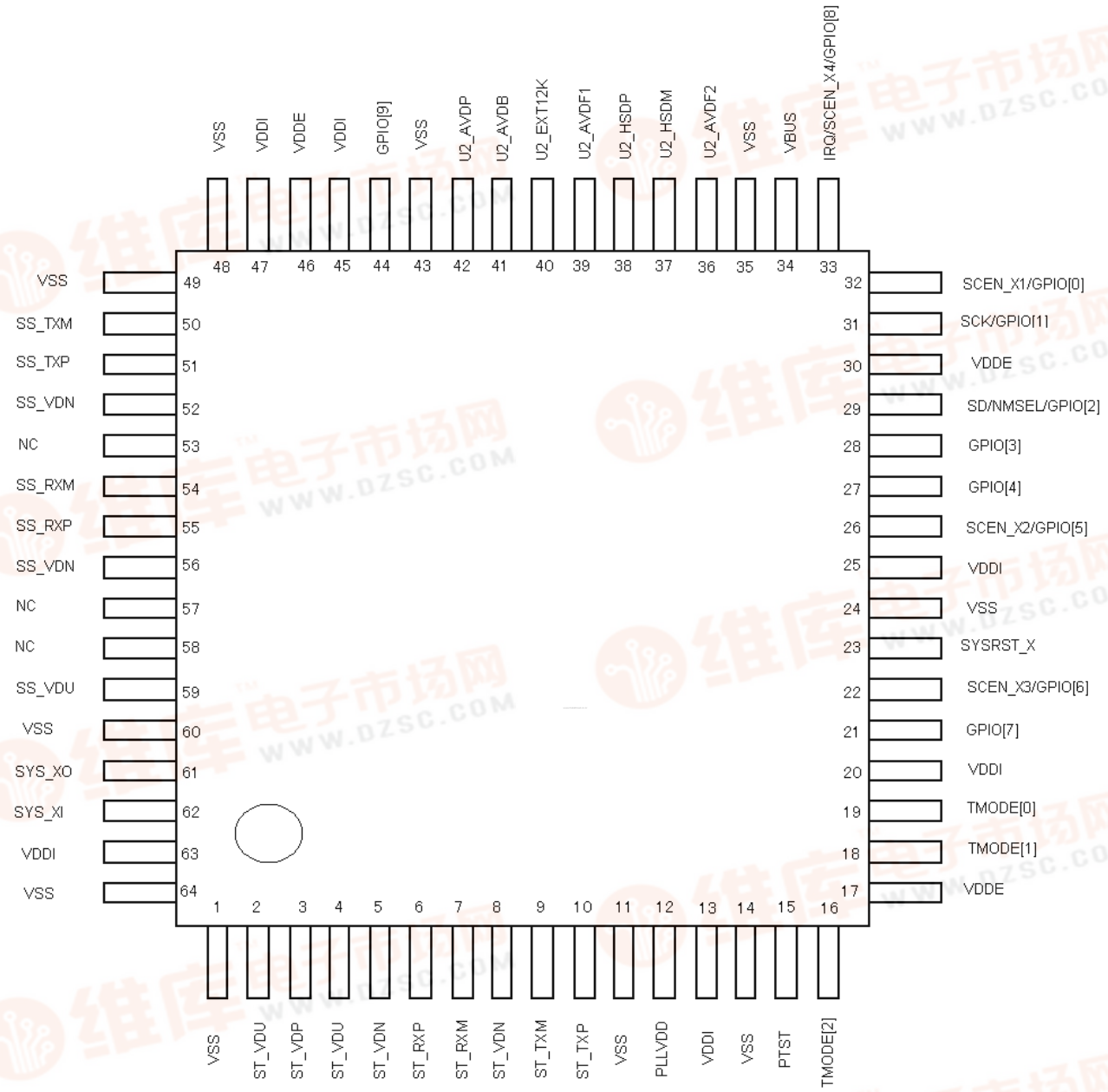
- SuperSpeed (5 Gbps) / high-speed (480 Mbps) / full-speed (12 Mbps)
  Compliant to Universal Serial Bus 3.0 Specification, Revision 1.0
  Compliant to Universal Serial Bus Specification, Revision 2.0
- UAS Protocol Transport
- Mass Storage Class Bulk-Only Transport
  Compliant to Mass Storage Class Bulk-Only Transport, Revision 1.0
- NCQ function
- HID Class (Option)
- SATA Gen2i (3 Gbps) & Gen1i (1.5 Gbps)
  Compliant to Serial ATA Specification Revision 2.6
- Supports both ATA and ATAPI device
- Supports Hot-plugging of ATA device
- Supports port multiplier device (Option)
- ATA command pass through function
- Supports over 2TB over HDD & 4K sector HDD
- An Integrated a high performance 32bit RISC MPU
- Several customized function, VID / PID and etc.
- An Integrated high speed encryption block
- IEEE1667 (Option)
- GPIO function including PWM: LQFP package 10 pins, QFN package 9 pins
- SPI for Serial Flash ROM & plural SPI devices
- Embedded SSCG for SuperSpeed USB
- One external crystal (25MHz)
- LQFP-64 & QFN-48 package

ARM™

FUJITSU

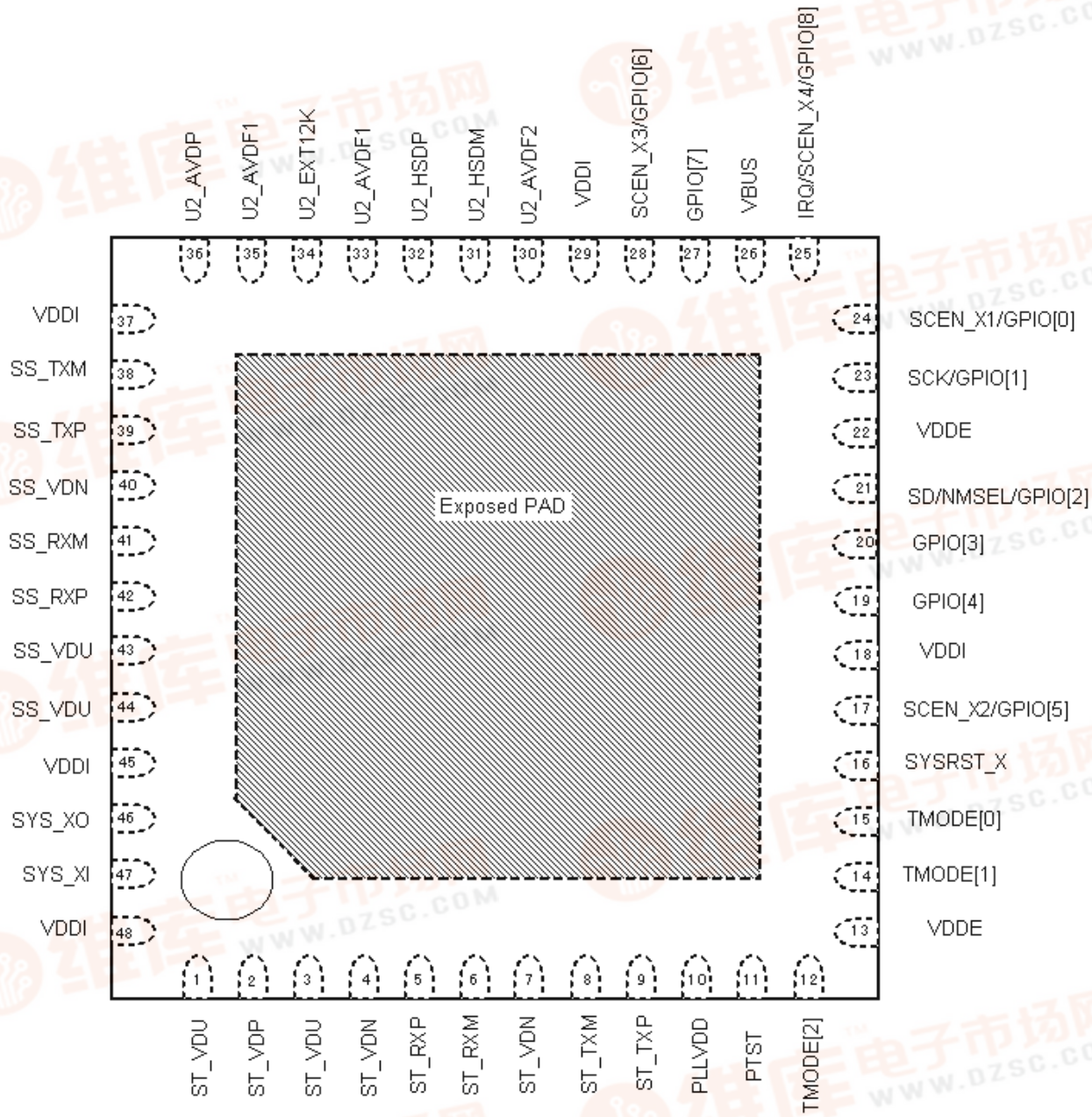
PIN ASSIGNMENTS(LQFP-64)

TOP VIEW



• PIN ASSIGNMENTS(QFN - 48)

TOP VIEW



PIN ASSIGNMENTS TABLE**(LQFP-64)**

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VSS	23	SYSRST_X	45	VDDI
2	ST_VDU	24	VSS	46	VDDE
3	ST_VDP	25	VDDI	47	VDDI
4	ST_VDU	26	SCEN_X2 /GPIO[5]	48	VSS
5	ST_VDN	27	GPIO[4]	49	VSS
6	ST_RXP	28	GPIO[3]	50	SS_TXM
7	ST_RXM	29	SD /NMSEL /GPIO[2]	51	SS_TXP
8	ST_VDN	30	VDDE	52	SS_VDN
9	ST_TXM	31	SCK /GPIO[1]	53	NC
10	ST_TXP	32	SCEN_X1 /GPIO[0]	54	SS_RXM
11	VSS	33	IRQ /SCEN_X4 /GPIO[8]	55	SS_RXP
12	PLLVDD	34	VBUS	56	SS_VDN
13	VDDI	35	VSS	57	NC
14	VSS	36	U2_AVDF2	58	NC
15	PTST	37	U2_HSDM	59	SS_VDU
16	TMODE_2	38	U2_HSDP	60	VSS
17	VDDE	39	U2_AVDF1	61	SYS_XO
18	TMODE_1	40	U2_EXT12K	62	SYS_XI
19	TMODE_0	41	U2_AVDB	63	VDDI
20	VDDI	42	U2_AVDP	64	VSS
21	GPIO_7	43	VSS		
22	SCEN_X3 /GPIO[6]	44	GPIO_9		

PIN ASSIGNMENTS TABLE**(QFN-48)**

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	ST_VDU	17	SCEN_X2 /GPIO[5]	33	U2_AVDF1
2	ST_VDP	18	VDDI	34	U2_EXT12K
3	ST_VDU	19	GPIO[4]	35	U2_AVDF1
4	ST_VDN	20	GPIO[3]	36	U2_AVDP
5	ST_RXP	21	SD /NMSEL /GPIO[2]	37	VDDI
6	ST_RXM	22	VDDE	38	SS_TXM
7	ST_VDN	23	SCK /GPIO[1]	39	SS_TXP
8	ST_TXM	24	SCEN_X1 /GPIO[0]	40	SS_VDN
9	ST_TXP	25	IRQ /SCEN_X4 /GPIO[8]	41	SS_RXM
10	PLLVDD	26	VBUS	42	SS_RXP
11	PTST	27	GPIO[7]	43	SS_VDU
12	TMODE[2]	28	SCEN_X3 /GPIO[6]	44	SS_VDU
13	VDDE	29	VDDI	45	VDDI
14	TMODE[1]	30	U2_AVDF2	46	SYS_XO
15	TMODE[0]	31	U2_HSDM	47	SYS_XI
16	SYSRST_X	32	U2_HSDP	48	VDDI

PIN DESCRIPTOIN(LQFP - 64)

1. System Interface of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
SYS_XI	I	-	-	1	25MHz crystal Input.
SYS_XO	IO	-	-	1	25MHz crystal Input and output.
SYSRST_X	I	L	PU	1	System reset.

2. USB3.0 Interface of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
SS_TXP	O	-	-	1	SuperSpeed TX+ (Differential signal).
SS_TXM	O	-	-	1	SuperSpeed TX- (Differential signal).
SS_RXP	I	-	-	1	SuperSpeed RX+ (Differential signal).
SS_RXM	I	-	-	1	SuperSpeed RX- (Differential signal).
SS_VDN	-	-	-	2	1.2V Analog power supply.
SS_VDU	-	-	-	1	1.2V Analog power supply for PLL.

3. USB2.0 Interface of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
U2_EXT12K	O	-	-	1	External resistance pin for internal fixed current circuit.12KΩ±1%.
U2_HSDP	IO	-	-	1	USB D+.
U2_HSDM	IO	-	-	1	USB D-.
U2_AVDP	-	-	-	1	1.2V Analog power supply for PLL.
U2_AVDB	-	-	-	1	3.3V Analog power supply for USB driver receiver.
U2_AVDF1	-	-	-	1	
U2_AVDF2	-	-	-	1	1.2V Analog power supply for USB driver receiver.

4. SATA Interface of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
ST_TXP	O	-	-	1	SATA TX+ (Differential signal).
ST_TXM	O	-	-	1	SATA TX- (Differential signal).
ST_RXP	I	-	-	1	SATA RX+ (Differential signal).
ST_RXM	I	-	-	1	SATA RX- (Differential signal).
ST_VDP	-	-	-	1	3.3V Analog power supply.
ST_VDN	-	-	-	2	1.2V Analog power supply.
ST_VDU	-	-	-	2	Analog power supply for 1.2V PLL.

5. Peripheral Interface of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
SCEN_X1/ GPIO[0]	IO	L	-	1	Serial Flash ROM chip enable or General Purpose IO port [0] including PWM.
SCK/ GPIO[1]	IO	-	-	1	Serial Flash ROM clock or General Purpose IO port [1] including PWM.
SD /NMSEL /GPIO[2]	IO	-	PU	1	Serial Flash ROM data, selecting normal mode/maintenance mode or General Purpose IO port [2] including PWM*. Note: This pin must not be fixed to PD.
GPIO[3]	IO	-	PD	1	General Purpose IO port [3] including PWM.
GPIO[4]	IO	-	PU	1	General Purpose IO port [4] including PWM.
SCEN_X2 GPIO[5]	IO	-	PU	1	Serial Flash ROM chip enable for expansion or General Purpose IO port [5] including PWM.
SCEN_X3/ GPIO[6]	IO	-	PU	1	Serial Flash ROM chip enable for expansion or General Purpose IO port [6] including PWM.
GPIO[7]	IO	-	-	1	General Purpose IO port [7] including PWM.
IRQ/ SCEN_X4/ GPIO[8]	IO	-	PD	1	External interruption inputting, Serial Flash ROM chip enable for expansion or General Purpose IO port [8] including PWM. Note: When GPIO[8] is used as Serial Flash ROM chip enable, set pull-up resistor on the board. If MB86C31 is turned on without setting pull-up, data might collide. Because enable-signal is asserted by pull-down of internal IO. Refer to VIH(minimum) of the SPI flash used about the pull-up resistor value..
GPIO[9]	IO	-	PD	1	General Purpose IO port [9] including PWM.
VBUS	I	H	-	1	VBUS monitor.

6. MODE SELECT INTERFACE of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
PTST	I	H	PD	1	“No connect”. or “connect to 0”
TMODE[0]	I	-	PU	1	connect to 1 *
TMODE[1]	I	-	PD	1	connect to 0.*
TMODE[2]	I	-	PD	1	“No connect”. or “connect to 0”

*: Note that TMODE[1] should be connected to 0 and TMODE[0] should be connected to 1.

7. POWER/GND of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
PLLVDD	-	-	-	1	1.2V Analog power supply for PLL.
VDDE	-	-	-	3	3.3V power supply for external IO.
VDDI	-	-	-	6	1.2V power supply for Internal core.
VSS	-	-	-	10	GND.

8. OTHERS of LQFP - 64

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
NC	-	-	-	3	No connect.

• PIN DESCRIPTOIN(QFN - 48)

1. System Interface of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
SYS_XI	I	-	-	1	25MHz crystal Input.
SYS_XO	IO	-	-	1	25MHz crystal Input and output.
SYSRST_X	I	L	PU	1	System reset.

2. USB3.0 Interface of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
SS_TXP	O	-	-	1	SuperSpeed TX+ (Differential signal).
SS_TXM	O	-	-	1	SuperSpeed TX- (Differential signal).
SS_RXP	I	-	-	1	SuperSpeed RX+ (Differential signal).
SS_RXM	I	-	-	1	SuperSpeed RX- (Differential signal).
SS_VDN	-	-	-	1	1.2V Analog power supply.
SS_VDU	-	-	-	2	1.2V Analog power supply for PLL.

3. USB2.0 Interface of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
U2_EXT12K	O	-	-	1	External resistance pin for internal fixed current circuit.12KΩ±1%.
U2_HSDP	IO	-	-	1	USB D+.
U2_HSDM	IO	-	-	1	USB D-.
U2_AVDP	-	-	-	1	1.2V Analog power supply for PLL.
U2_AVDF1	-	-	-	2	3.3V Analog power supply for USB driver receiver.
U2_AVDF2	-	-	-	1	1.2V Analog power supply for USB driver receiver.

4. SATA Interface of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
ST_TXP	O	-	-	1	SATA TX+ (Differential signal).
ST_TXM	O	-	-	1	SATA TX- (Differential signal).
ST_RXP	I	-	-	1	SATA RX+ (Differential signal).
ST_RXM	I	-	-	1	SATA RX- (Differential signal).
ST_VDP	-	-	-	1	3.3V Analog power supply.
ST_VDN	-	-	-	2	1.2V Analog power supply.
ST_VDU	-	-	-	2	Analog power supply for 1.2V PLL.

5. Peripheral Interface of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
SCEN_X1/ GPIO[0]	IO	L	-	1	Serial Flash ROM chip enable or General Purpose IO port [0] including PWM.
SCK/ GPIO[1]	IO	-	-	1	Serial Flash ROM clock or General Purpose IO port [1] including PWM.
SD /NMSEL /GPIO[2]	IO	-	PU	1	Serial Flash ROM data, selecting normal mode/maintenance mode or General Purpose IO port [2] including PWM. Note: This pin must not be fixed to PD.
GPIO[3]	IO	-	PD	1	General Purpose IO port [3] including PWM.
GPIO[4]	IO	-	PU	1	General Purpose IO port [4] including PWM.
SCEN_X2 GPIO[5]	IO	-	PU	1	Serial Flash ROM chip enable for expansion or General Purpose IO port [5] including PWM.
SCEN_X3/ GPIO[6]	IO	-	PU	1	Serial Flash ROM chip enable for expansion or General Purpose IO port [6] including PWM.
GPIO[7]	IO	-	-	1	General Purpose IO port [7] including PWM.
IRQ/ SCEN_X4/ GPIO[8]	IO	-	PD	1	External interruption inputting, Serial Flash ROM chip enable for expansion or General Purpose IO port [8] including PWM*. Note: When GPIO[8] is used as Serial Flash ROM chip enable, set pull-up resistor on the board. If MB86C31 is turned on without setting pull-up, data might collide. Because enable-signal is asserted by pull-down of internal IO. Refer to VIH(minimum) of the SPI flash used about the pull-up resistor value..
VBUS	I	H	-	1	VBUS monitor.

6. MODE SELECT INTERFACE of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
PTST	I	H	PD	1	“No connect”. or “connect to 0”
TMODE[0]	I	-	PU	1	connect to 1 *
TMODE[1]	I	-	PD	1	connect to 0.*
TMODE[2]	I	-	PD	1	“No connect”. or “connect to 0”

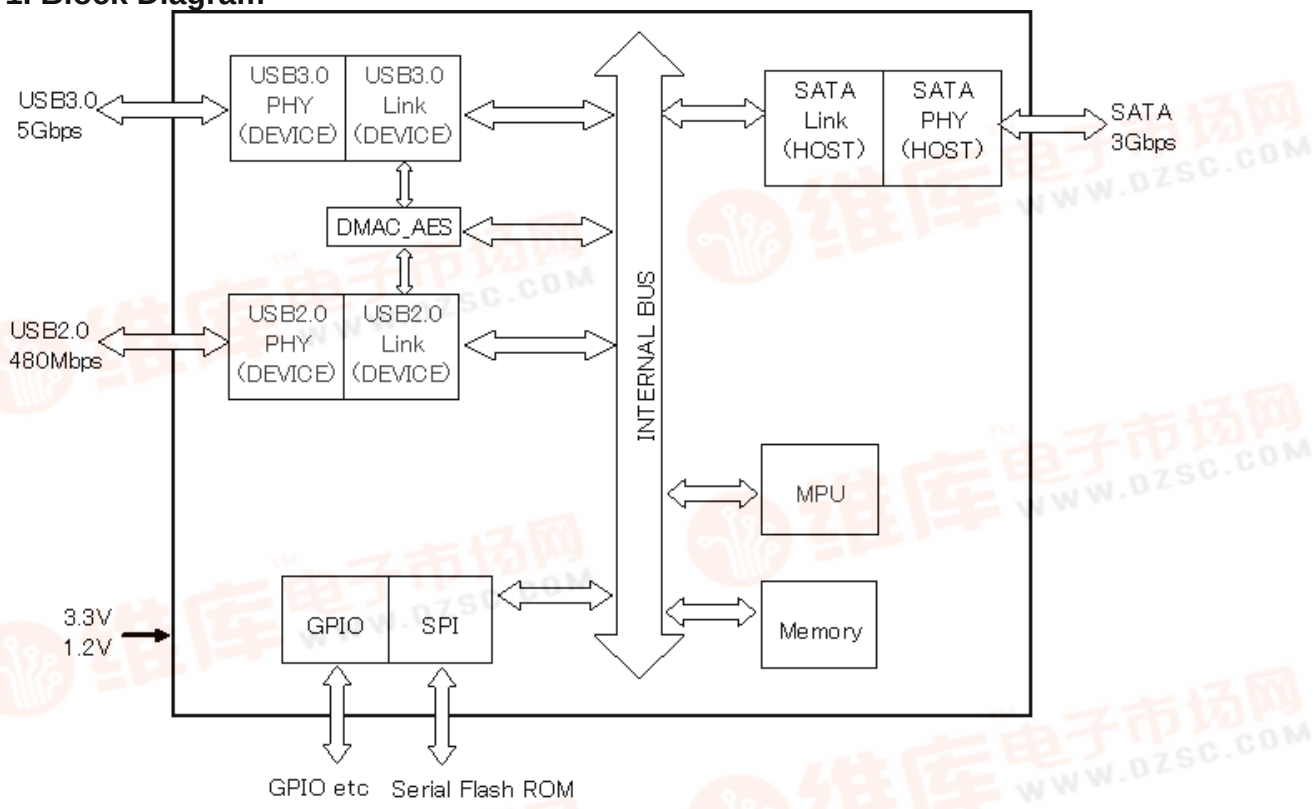
***:** Note that TMODE[1] should be connected to 0 and TMODE[0] should be connected to 1.

7. POWER/GND of QFN - 48

Pin name	I/O	Active	PU/PD	Pin count	Function explanation
PLLVDD	-	-	-	1	1.2V Analog power supply for PLL.
VDDE	-	-	-	2	3.3V power supply for external IO.
VDDI	-	-	-	5	1.2V power supply for Internal core.
Exposed PAD	-	-	-	1	GND.

BLOCK DIAGRAM

1. Block Diagram



2. USB3.0 PHY

PHY layer of USB3.0. It transfers the data between host and USB3.0_LINK.

3. USB3.0 LINK

Link layer of USB3.0. It transfers the data between USB3.0_PHY and Internal bus.

4. USB2.0 PHY

PHY layer of USB2.0. It transfers the data between host and USB2.0_LINK.

5. USB2.0 LINK

Link layer of USB2.0. It transfers the data between USB2.0_PHY and Initial bus.

6. SATA PHY

PHY layer of SATA. It transfers the data between external SATA device and SATA_LINK.

7. SATA LINK

Link layer of SATA. It transfers the data between SATA_PHY and Internal bus.

8. DMAC_AES

A DMA controller with high speed encryption engine. The AES encryption hardware encrypts and decrypts the data if you select to use the MB86C311A. XTS-AES are supported.

Key length : 128bit + 128bit / 256bit + 256bit
Throughput : ≥300 MB/s

9. MPU

High performance ARM™ 32bit RISC processor, Cortex-M3™.

*: ARM and Cortex-M3 are the trademark of ARM Limited in the EU and other countries.

10. MEMORY

Internal RAM used by firmware which is connected with the local bus.

11. SPI

Interface for Serial Flash ROM. Supports ROM devices complied with SPI standard. The firmware and the configuration data are stored in Serial Flash ROM.

12. GPIOs

General Purpose I/O that can be used for the LED control and the switch, etc. All GPIOs have PWM function and it is pssible to set arbitrary Duty.

Cycle time of PWM
MIN: 53nsec
MAX: 114sec

ELECTRICAL SPECIFICATION

1. Absolute maximum rating

Item	Sign	Ratings value		Unit
		min	max	
Power-supply voltage	1.2V power supply *1	-0.5	1.8	V
	3.3V power supply *2	-0.5	4.6	V
Input voltage	VI	-0.5	3.3 V power supply voltage + 0.5 V (≤ 4.6 V)	V
Output voltage	VO	-0.5	3.3 V power supply voltage + 0.5 V (≤ 4.6 V)	V
Storage temperature	Tst	-55	+125	°C

*1: SS_VDN, SS_VDU, U2_AVDP, U2_AVDF2, ST_VDN, ST_VDU, PLLVDD, VDDI

*2: U2_AVDB, U2_AVDF1, ST_VDP, VDDE

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended operating conditions

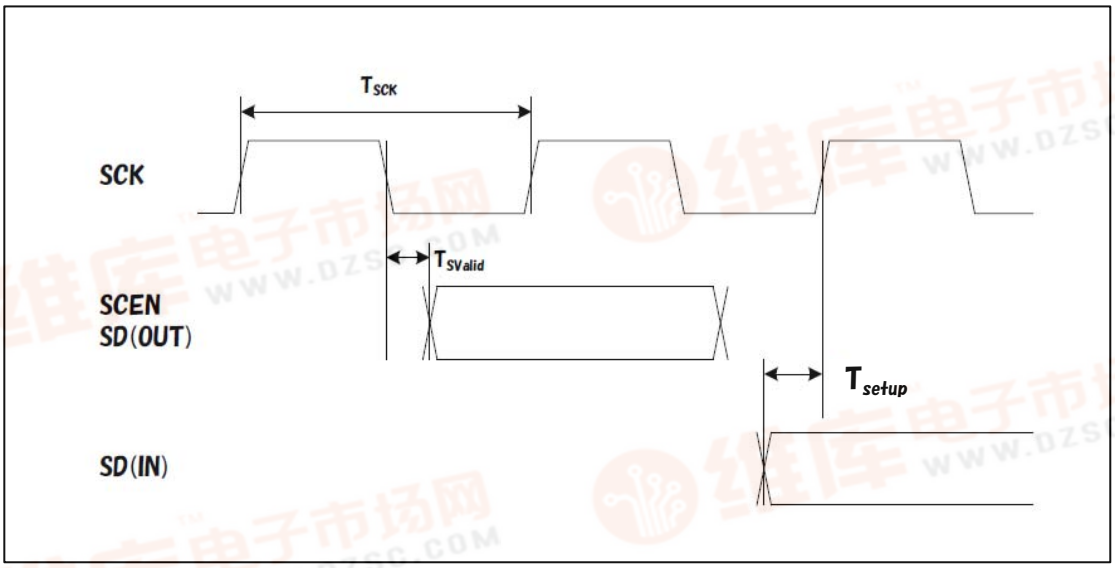
Parameter	sign	min	typ	max	unit
Internal Power	1.2V power supply	1.1	1.2	1.3	V
I/O Power	3.3V power supply	3.0	3.3	3.6	V
Operating Temperature	Ta	0	-	70	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC SPECIFICATION

Parameter	Symbol	Power supply	Value			Unit
			Min	Typ	Max	
At activation	IDD	1.2 V power supply	-	230	320	mA
		3.3 V power supply	-	7	9	
When USB2.0 is used		1.2 V power supply	-	270	360	mA
		3.3 V power supply	-	26	39	
When USB2.0 is used suspend state		1.2 V power supply	-	230	320	mA
		3.3 V power supply	-	7	9	
When USB3.0 is used (U0 state)		1.2 V power supply	-	300	440	mA
		3.3 V power supply	-	7	9	
USB3.0 U1 state		1.2 V power supply	-	250	360	mA
		3.3 V power supply	-	7	9	
USB3.0 U2 state		1.2 V power supply	-	170	240	mA
		3.3 V power supply	-	7	9	
USB3.0 U3 state		1.2 V power supply	-	150	210	mA
		3.3 V power supply	-	7	9	
Input High Voltage	VIH	-	2.1	-	VDDE+0.3	V
Input Low Voltage	Vil	-	-0.3	-	0.7	V
Output High Voltage 3.3 V output current = − 0.1 mA	Voh	-	VDDE–0.2	-	VDDE	V
Output Low Voltage 3.3 V output current = 0.1 mA	Vol	-	0	-	0.2	V
Pull-up / Pull-down resistance (GPIO)	RUP	-	15	33	70	kΩ
Input Leak Current (GPIO)	Il	-	-10	-	10	μA
Input Capacitor (GPIO)	Cin	-	-	10	16	pF

4.SPI interface AC specification



Parameter	Min.	Max.	Unit	Description
T_{SCK}	53.3	-	ns	SCK cycle time
T_{SValid}	-1.5	0.5	ns	SCK negative edge to data valid time for SCEN, SD (OUT)
T_{Setup}	13.5	-	ns	Required input setup time to SCK for SD (IN)

C=25pF

● ORDERING INFORMATION

Part number	Package	Encryption function
MB86C311APMC-GE1	64-pin Plastic LQFP (FPT-64P-M25)	supported
MB86C311BPMC-GE1	64-pin Plastic LQFP (FPT-64P-M25)	Non supported
MB86C311AWQN-GE1	48-pin Plastic QFN	supported
MB86C311BWQN-GE1	48-pin Plastic QFN	Non supported

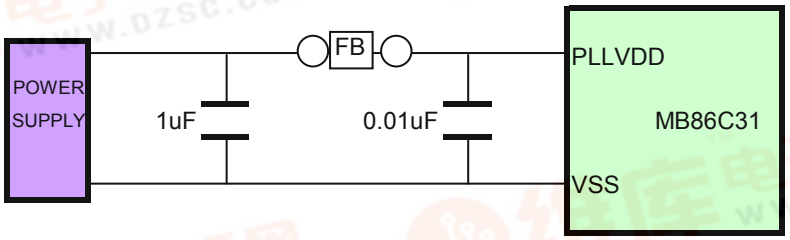
● POWER SUPPLY CIRCUIT

1. DISPLAY CONDENSER

Between power supply and GND, we recommend you to connect 4-8Chip laminated ceramic capacitor respectively. You arrange the chip laminated ceramic capacitor as much as possible near LSI. Between power supply and GND, we recommend you connect tantalum capacitor or electrolytic capacitor of about 10uF respectively.

2. PLL POWER SUPPLY WIRING

We recommend less noise than 100 mVpp for the power supply of PLL.
The figure below shows the example for reducing the noise, where FB indicates a ferrite bead inductor and the values are reference values.



● ABOUT TURNING ON THE POWER SUPPLY

1. Initialization reset

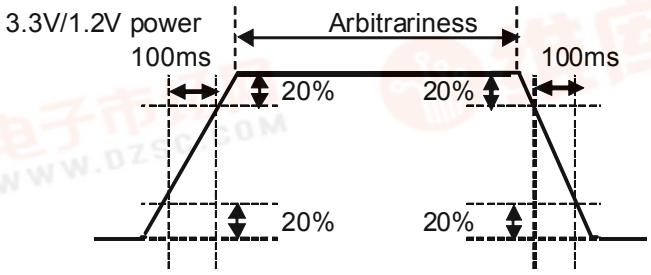
You must put power-on reset to SYSRST_X when you turn on the power supply. Moreover, please put SYSRST_X into the state of Low until the input clock is steady.
Set up time is 100 usec. So, negate SYSRST_X after waiting 100 usec.

2. Irregular output

There is a possibility that the output terminal becomes irregular until an internal power supply is steady whenpower supply is turned on.

3. Turning on/off the power supply

item	Regulator		Pin	min	Max	unit
Turning on/ off the power supply	3.3V Power supply	Digital power supply for external IO	VDDE	-	100	ms
		SATA 3.3V analog power supply	ST_VDP	-	100	ms
		USB2.0 3.3V analog power supply	U2_AVDF1, U2_AVDB	-	100	ms
Turning on/off the power supply	1.2V Power supply	Analog power supply for PLL	PLLVDD	-	100	ms
		Digital power supply for internal core	VDDI	-	100	ms
		SATA 1.2V analog power supply	ST_VD, ST_VDU	-	100	ms
		USB3.0 1.2V analog power supply	SS_VDN、SS_VDU	-	100	ms
		USB2.0 1.2V analog power supply	U2_AVDF2, U2_AVDP	-	100	ms



Turning on/off the power supply

4. Note of turning on/ off the power supply

We recommend the following order for turning on/off the power supply.

turning on: 1.2V power source → 3.3V source → signal
turning of: signal → 3.3V power source → 1.2Vpower Source

Input the signal after the input clock and the power supply stabilizes.

5. Note of PLL power supply

Power supply (PLLVDD, U2_AVDP) for analog PLL must not rise more than VDDI when you turn on/off the power supply.

6. Normal mode / Maintenance mode

Select either maintenance mode or normal mode with GPIO[2] under the below conditions at power on.

(1) Normal mode : GPIO[2] is High
(2) Maintenance mode : GPIO[2] keeps low for 1 to 5 seconds, then turns High.
(3) Error : Others

*: The maintenance mode is the mode used for the farm wear debug, and is normally unnecessary. See the USERS MANUAL for details on the Maintenance mode.

● RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of Fujitsu Microelectronics with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) .
A product whose part number has trailing characters “E1” is RoHS compliant.

• Notes when board is designed

1. Common notes of differential signal

1. Please shorten the wiring of D + /D − to cable connector as much as possible.
2. Please adjacently wire D + and D − . Please keep constantly the line-space and stroke width from the edge to the edge.
3. Please make wiring a big R bend of 45° or less. 90° bend is a prohibition.
4. Please make shields and avoid other signals which are adjoining for avoiding crosstalk noise from the same layer.
5. Please avoid Via. Because, Via is one of the reasons for reflection.

2. USB2.0

1. Wire the same length for below lines. Suppress the tolerance to 1.5 mm or less. Make them to equal length as much as possible without making them to the meander wiring.
   U2_HSDP and U2_HSDM
2. It is necessary to take the impedance match of the wiring for the board. Each impedance property is as follows. USB2.0 impedance property : Differential impedance : 90 Ω ± 7%.
   :Single ended impedance: 45 Ω ± 7% (reference).
3. The efficiency of a common mode chalk filter depends on an external condition. It may be effective or not effective. Beforehand, we recommend that you design the board which can be inserted and non-inserted common mode chalk filter.

3. USB3.0

1. Wire the same length for below lines. Suppress the tolerance to 1.0 mm or less. Make them to equal length as much as possible without making them to the meander wiring.
   SS_TXP and SS_TXM
   SS_RXP and SS_RXM
2. It is necessary to take the impedance match of the wiring for the board.
   Each impedance property is as follows.
   USB3.0 impedance property: Differential impedance : 90 Ω ± 7%.
   : Single ended impedance: 45 Ω ± 7% (reference).
3. Using a common mode chalk filter is depending to an external condition. It might be effective or not effective. Beforehand, we recommend that you design the board which can be inserted and non-inserted common mode chalk filter.

4. SATA

1. Wire the same length for below lines. Suppress the tolerance to 1.0 mm or less. Make them to equal length as much as possible without making them to the meander wiring.
   ST_TXP and ST_TXM
   ST_RXP and ST_RXM

2. It is necessary to take the impedance match of the wiring for the board.
   Each impedance property is as follows.
   SATA impedance property : Differential impedance : 100 Ω ± 7%.
   : Common mode impedance: 35 Ω ± 7% (reference).

5. U2_EXT12K

1. U2_EXT12K connects GND (VSS) through the external resistance element 12 kΩ.
2. Arrange resistive element External 12 kΩ near the terminal.
   Shorten wiring from the pin to resistance as much as possible.
3. Use the resistive element External 12 kΩ whose precision is 12 kΩ ± 1%.
4. When cross talk noise is propagated to U2_EXT12K, the influence appears in all operations for USB2.0. We forbid other signal wires are adjacent to wiring from U2_EXT12K to resistive element External 12 kΩ. We forbid other signal wires cross to wiring from U2_EXT12K to resistive element External 12 kΩ.
   It is a prohibition that two or more kinds cross the wiring, even if it is GND and power supply.
5. To intercept the noise from other signal wires, it is recommended to shield all sides by the GND.
6. Adjust the capacity added to the U2_EXT12K to 10 pF or less. The value is including parasitic capacitance of wiring with the board and PKG.
7. Suppress the amount of the noise in the U2_EXT12K pin to 50 mV or less by the peak to peak.
8. Measure the noise amount under the below conditions for measuring the noise of U2_EXT12K pin.Location of measurement: pin and GND. Or, it is the vicinity of both ends of resistive element External 12 kΩ.

   Input resistance: 1 MΩ or more.
   Input capacitance: 1 pF or less.
   Band: 1.5 GHz or more.

6. About crystal

1. We recommend accuracy of the crystal is 50 ppm or less.
2. Influences from other signal wirings such as cross talk noise on crystal oscillator will affect the operation, for example jitter would occur. Countermeasures are necessary such that distance from the signal wire is to be ensured on board or crystal is to be shielded with the stable power supply line.
3. The best circuit constant changes by the specification and the ambient surrounding (parasitic capacitance etc. of an external substrate) of the crystal. We recommend you request the investigation (matching investigation) to crystal manufacturer about optimization of circuit constant by product substrate.

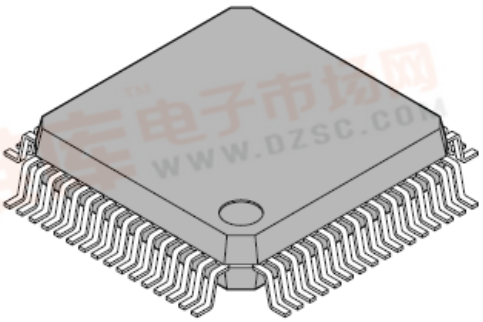
7. About power supply / GND

1. We recommend you make U2_AVDF1, U2_AVDF2, U2_AVDB, and U2_AVDP to be power supplies which are the exclusive uses of them. We recommend being separated from other power supplies.
2. We recommend you make ST_VDN, ST_VDP, and ST_VDU to be power supplies which are the exclusive uses of them. We recommend being separated from other power supplies.
3. We recommend you make SS_VDN, and SS_VDU to be power supplies which are the exclusive uses of them. We recommend being separated from other power supplies.
4. We recommend you make PLLVDD to be power supplies which are the exclusive uses of them. We recommend being separated from other power supplies.
5. There is an influence in operation and the characteristic when the noise is caused in a power supply or an analog GND. Please widen the area to the pattern of the power supply and the GND as much aspossible. Especially, please make the GND low impedance. For example, you make the GND to be a plane.
6. We recommend the change of an analogue system power supply and a GND are 30 mV or less.

• PACKAGE

1. LQFP Package

64-pin plastic LQFP

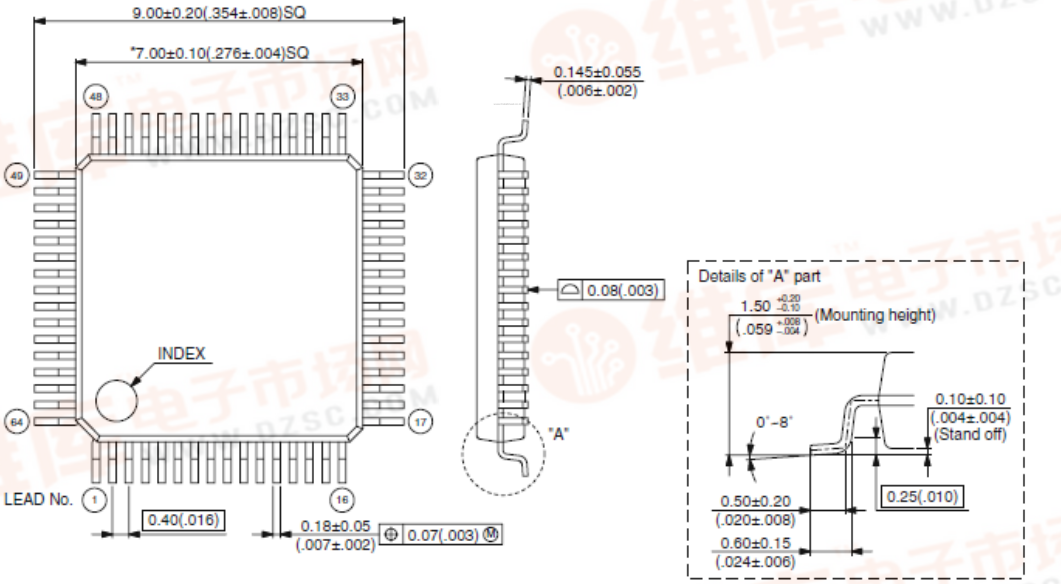


(FPT-64P-M25)

Lead pitch	0.40 mm
Package width × package length	7.0 mm × 7.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm Max
Code (Reference)	P-LFQFP64-7×7-0.40

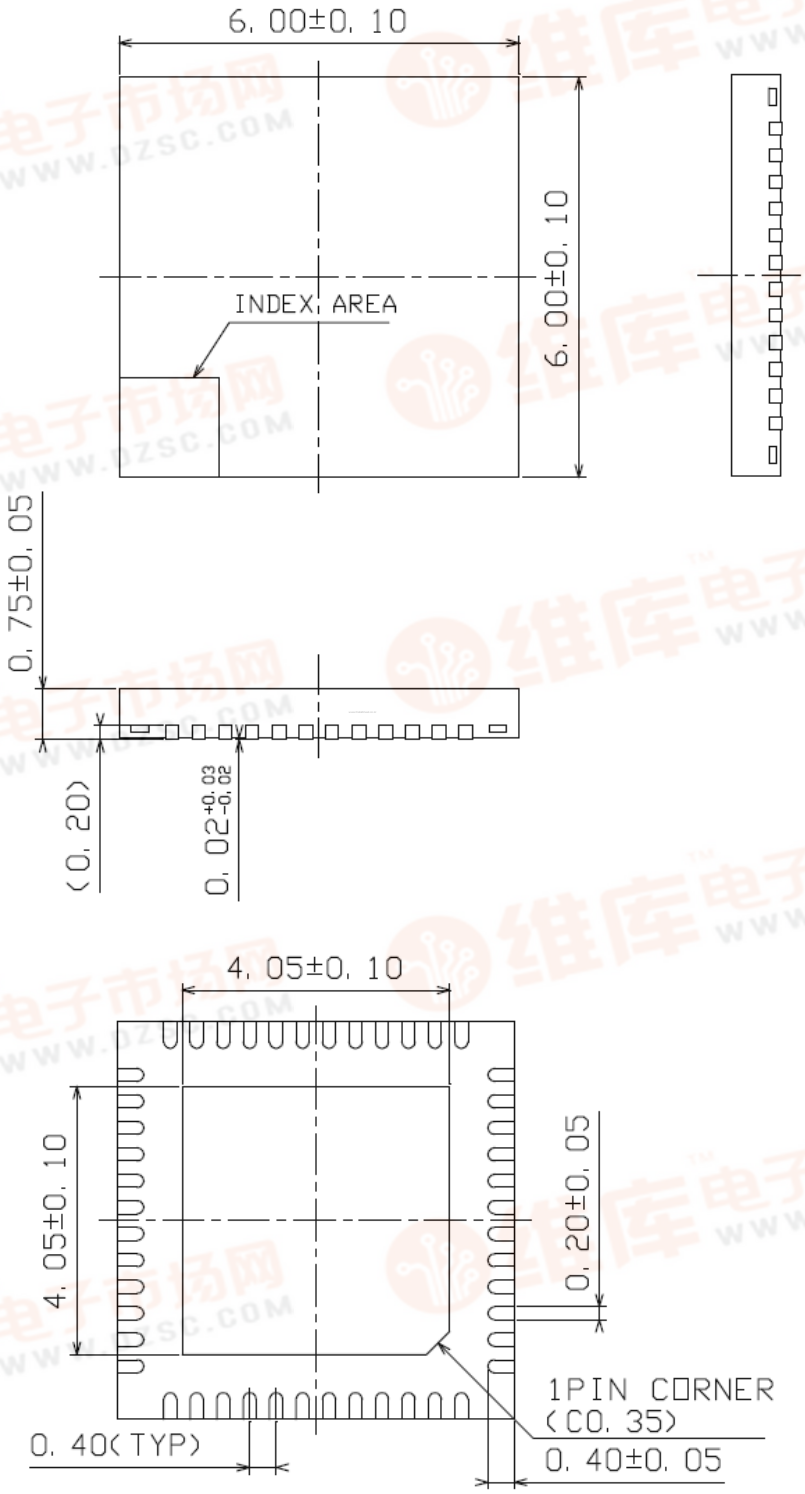
64-pin plastic LQFP
(FPT-64P-M25)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

2. QFN - 48 Package



Specifications are subject to change without notice. For further information please contact each office.