June 2004

RMWD24001

21–26.5 GHz Driver amplifier MMIC

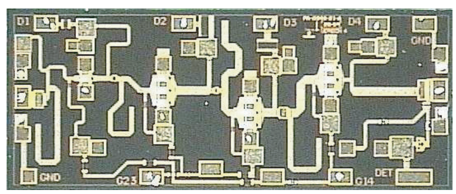
General Description

The RMWD24001 is a 4-stage GaAs MMIC amplifier designed as a 21 to 26.5 GHz Driver Amplifier for use in point to point and point to multi-point radios, and various communications applications. In conjunction with other Fairchild Semiconductor amplifiers, multipliers and mixers it forms part of a complete 23 and 26 GHz transmit/receive chipset. The RMWD24001 utilizes our 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of driver amplifier applications.

Features

- 4 mil substrate
- Small-signal gain 23dB (typ.)
- 1dB compressed Pout 17dBm (typ.)
- Voltage detector included to monitor Pout
- Chip size 2.85mm x 1.2mm

Device



Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Positive DC Voltage (+4V Typical)	+6	V
Vg	Negative DC Voltage	-2	V
Vdg	Simultaneous (Vd–Vg)	8	V
I_D	Positive DC Current	345	mA
P_{IN}	RF Input Power (from 50Ω source)	+8	dBm
T_C	Operating Baseplate Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C
R_{JC}	Thermal Resistance (Channel to Backside)	42	°C/W

Electrical Characteristics (At 25°C), 50 Ω system, Vd = +4V, Quiescent current Idq = 240 mA

Parameter	Min	Typ	Max	Units
Frequency Range	21		26.5	GHz
Gate Supply Voltage[1] (Vg)		0.4		V
Gain Small Signal at Pin = -12 dBm	20	23		dB
GainVariation vs Frequency		3		dB
Gain at 1 dBm Compression		22		dB
Power Output at P1 dB (Pin = -6 dBm)	13	17		dB
Drain Current at Pin = -12 dBm		240		dBm
Drain Current at 1dB Compression		265		mA
Input Return Loss (Pin = -12 dBm)		10		dB
Output Return Loss (Pin = -12 dBm)		12		dB
OIP3		TBD		dBm
Noise Figure		TBD		dB
Detector Voltage		TBD		V

Note:
1: Typical range of negative gate voltage is -0.7 to -0.1V to set typical Idq of 240 mA

Application Information

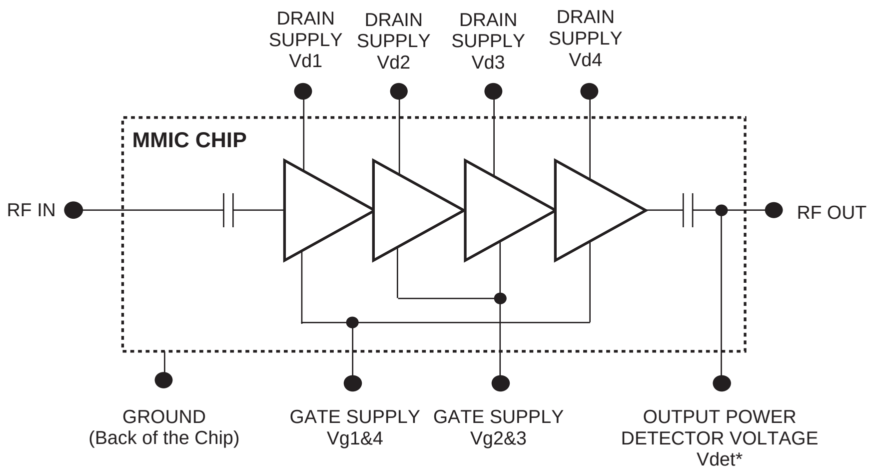
CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

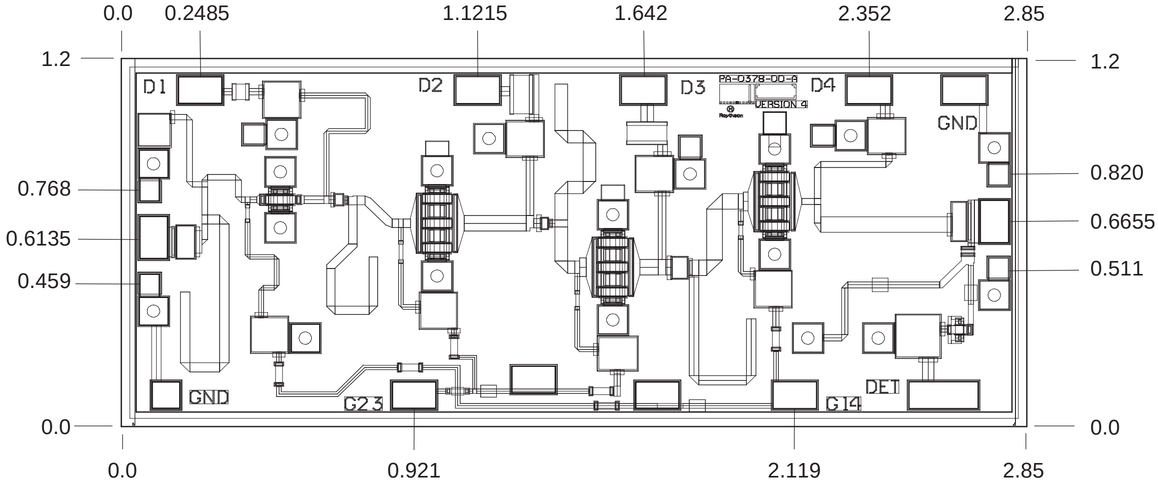
These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.



Note:
Detector delivers 0.1V DC into 3kΩ load resistor for > +7dBm output power. If output level detection is not desired, do not make connection to detector bond pad.

Figure 1. Functional Block Diagram



Dimensions in MM

Figure 2. Chip Layout and Bond Pad Locations
(Chip Size is 2.85mm x 1.2mm. Back of chip is RF and DC Ground)

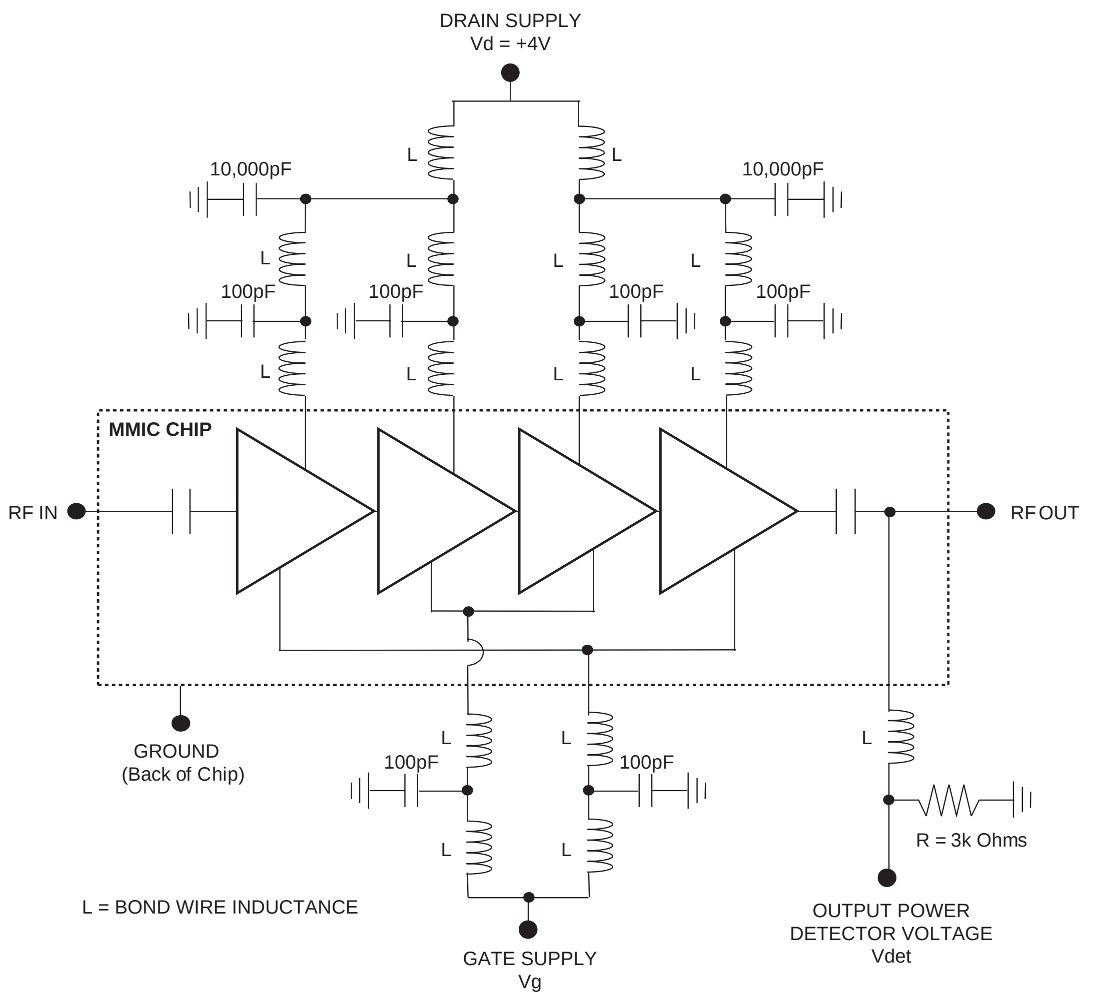
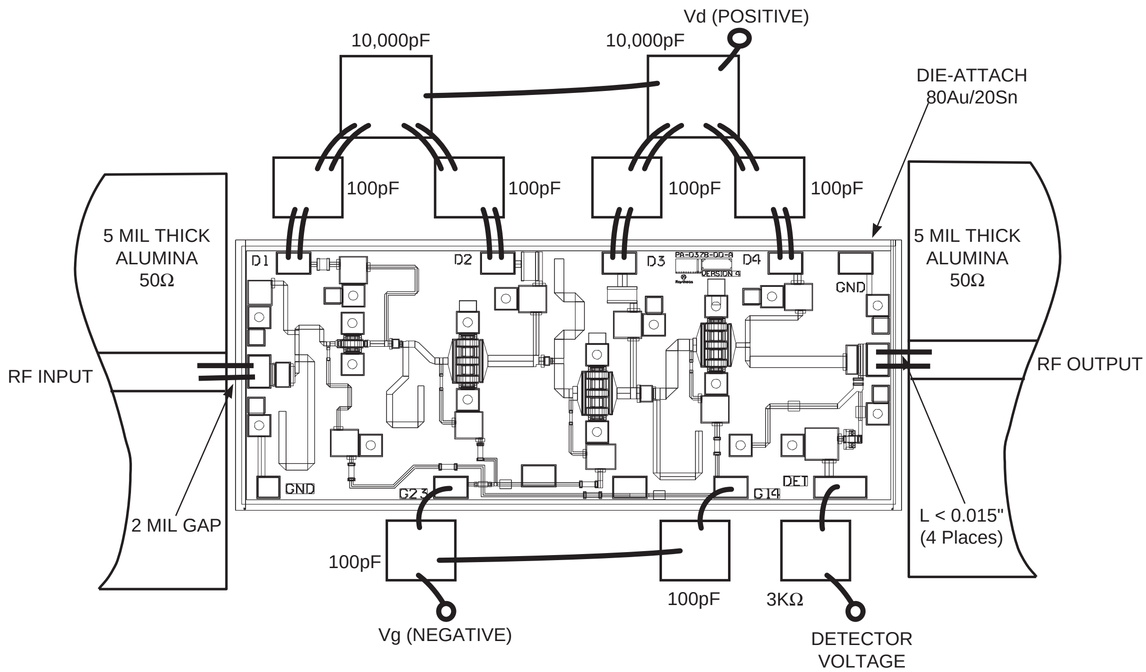


Figure 3. Recommended Application Schematic Circuit Diagram



Note:
Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

Figure 4. Recommended Assembly Diagram

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +5V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 240mA.

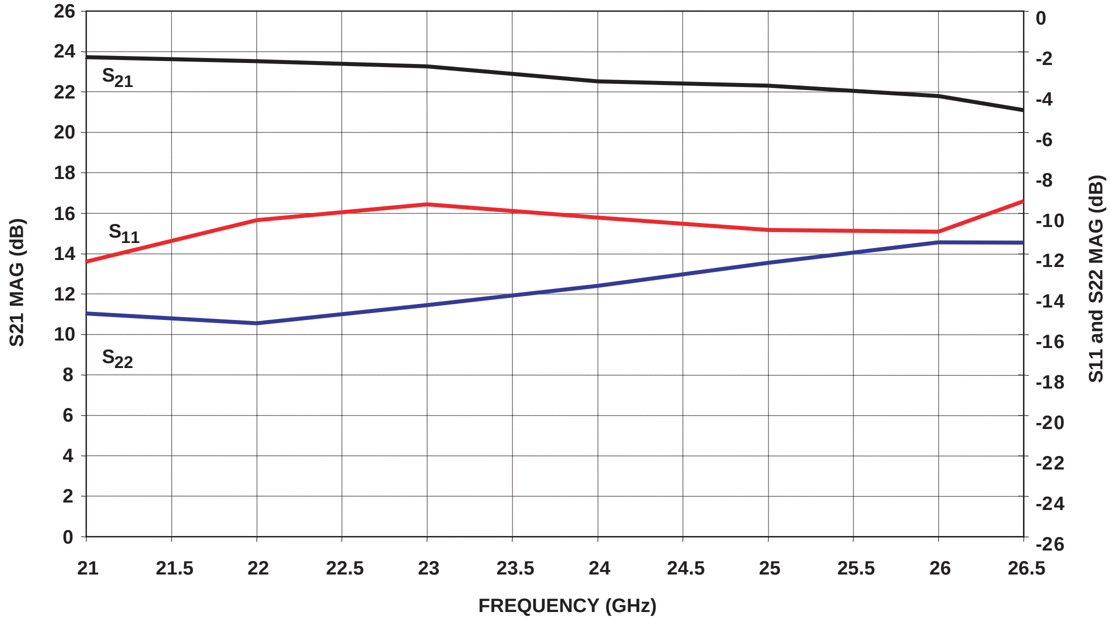
Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

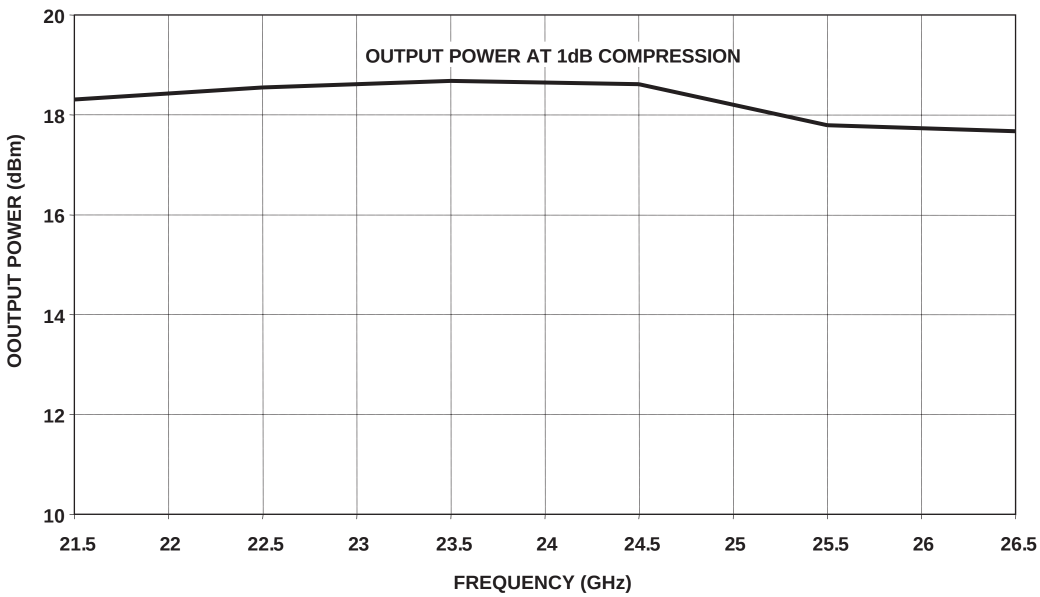
(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

Typical Characteristics

RMWD24001 26 GHz Driver Amplifier
Typical On-Wafer Performance I_{DQ} = 210mA, V_{DD} = 4V

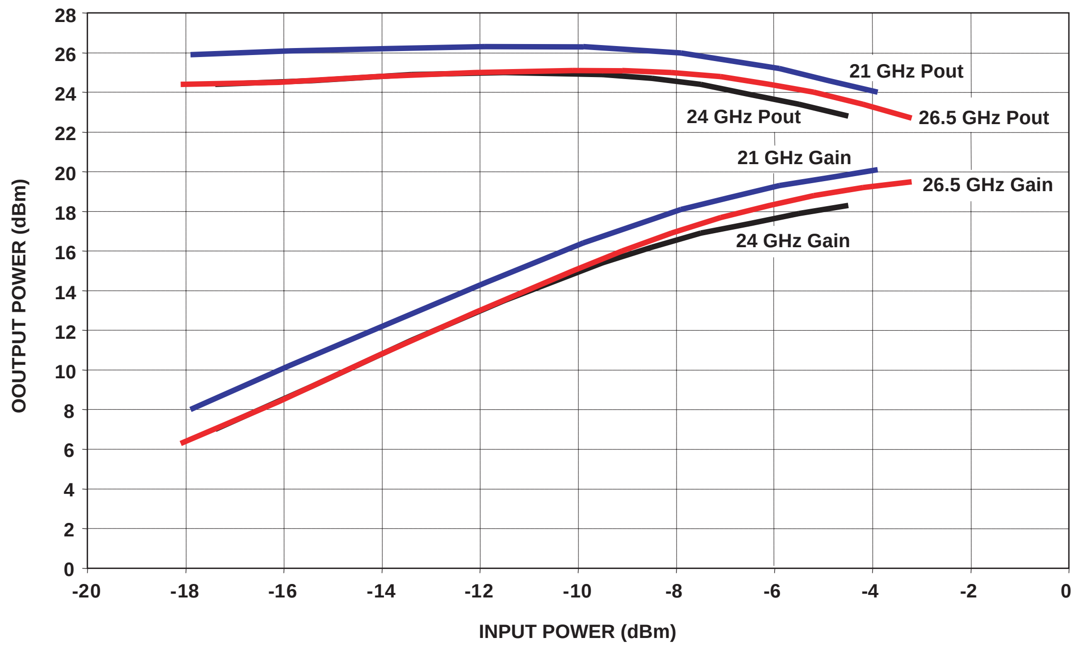


RMWD24001 26 GHz Driver Typical Output Power at 1 dB Gain Compression
Measured On-Wafer I_{DQ} = 240mA, V_{DD} = 4V

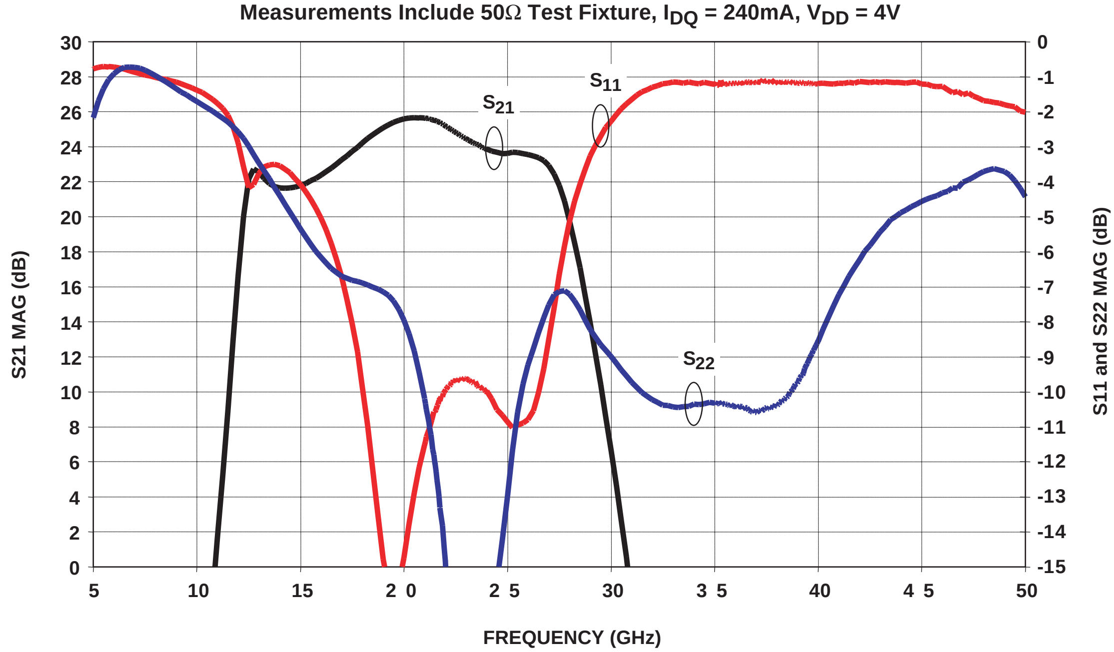


Typical Characteristics (Continued)

RMWD24001 Typical Power Saturation Curves
Measurements Include 50Ω Test Figure, I_{DQ} = 240mA, V_{DD} = 4V



RMWD24001 Driver Amplifer Typical WideBand S-Parameters
Measurements Include 50Ω Test Fixture, I_{DQ} = 240mA, V_{DD} = 4V



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