

TOSHIBA CCD LINEAR IMAGE SENSOR CCD (Charge Coupled Device)

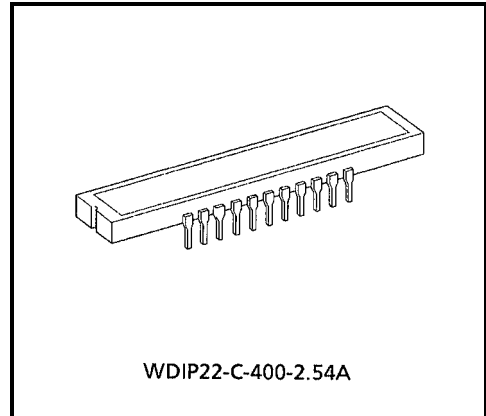
TCD2301C

The TCD2301C which includes sample-and-hold circuit and clamp circuit is a high sensitive and low dark current 3648 elements × 3 lines CCD color image sensor. The sensor is designed for color scanner.

The device contains a row of 3648 element × 3 lines photodiodes which provide a 16 lines / mm across a A4 size paper. The device is operated by 5V pulse, and 12V power supply.

FEATURES

- Number of Image Sensing Elements : 3648 elements × 3 lines
- Image Sensing Element Size : 8 μm by 8 μm on 8 μm centers
- Photo Sensing Region : High sensitive pn photodiode
- Distance Between Photodiode Array : 96 μm (12 Lines)
- Clock : 2 phase (5V)
- Internal Circuit : Sample & Hold circuit, Clamp circuit
- Package : 22 pin DIP
- Color Filter : Red, Green, Blue



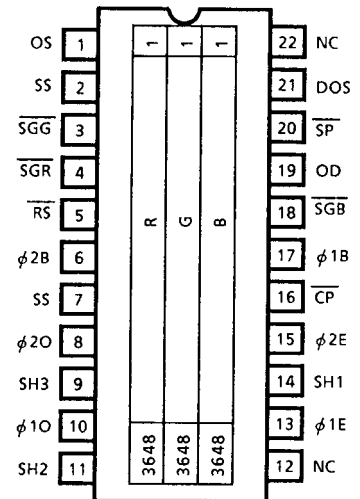
Weight: 4.8g (Typ.)

MAXIMUM RATINGS (Note 1)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|-------------------------------|---------------------|---------|------|
| Clock Pulse Voltage | V_{ϕ} | -0.3~8 | V |
| Shift Pulse Voltage | VSH | | |
| Reset Pulse Voltage | $\overline{V_{RS}}$ | | |
| Sample and Hold Pulse Voltage | $\overline{V_{SP}}$ | | |
| Switch Pulse Voltage | $\overline{V_{SG}}$ | | |
| Clamp Pulse Voltage | $\overline{V_{CP}}$ | | |
| Power Supply Voltage | V_{OD} | -0.3~15 | V |
| Operating Temperature | T_{opr} | 0~60 | °C |
| Storage Temperature | T_{stg} | -25~85 | °C |

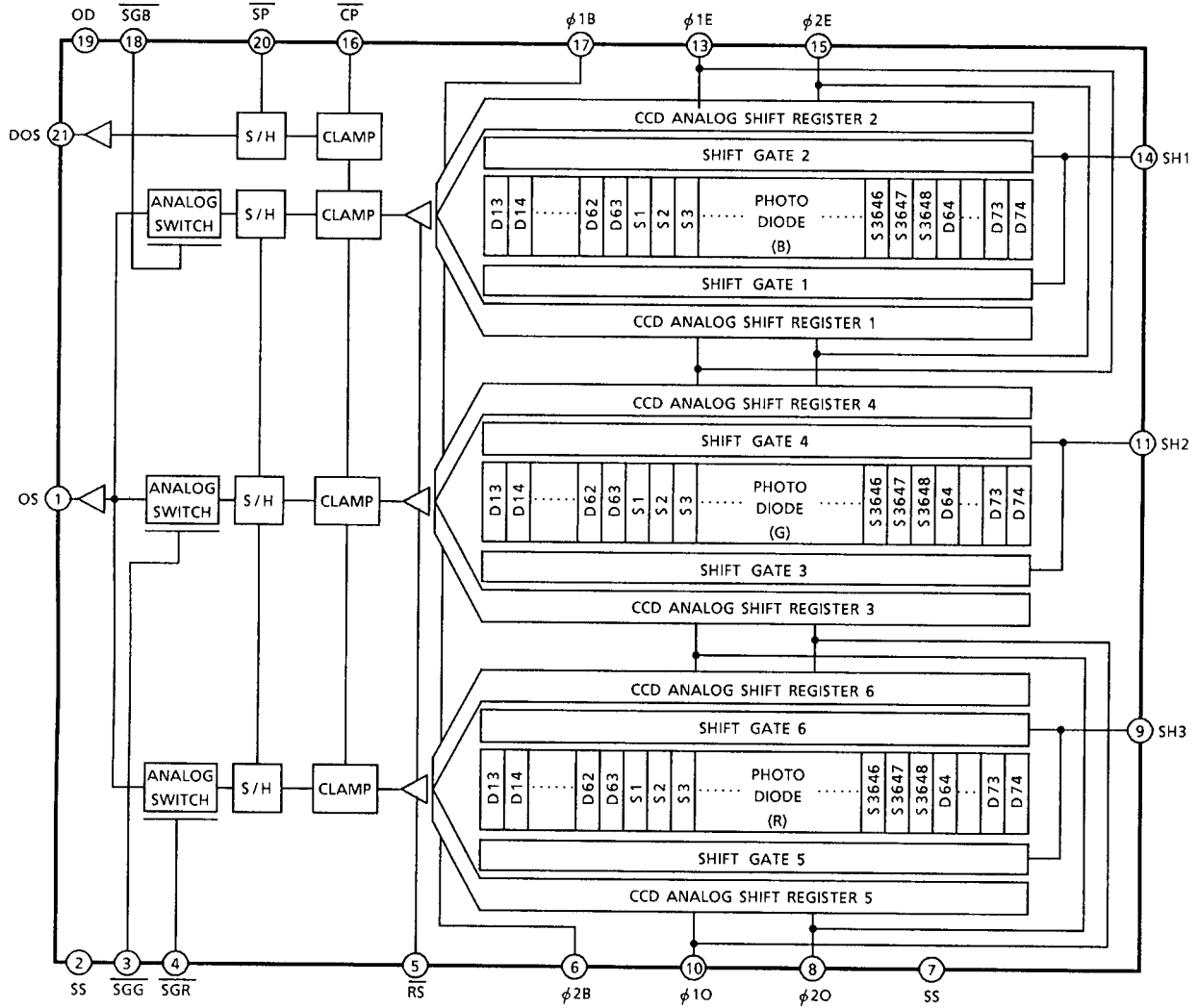
Note 1: All voltage are with respect to SS terminals (Ground).

PIN CONNECTION



(TOP VIEW)

CIRCUIT DIAGRAM



PIN NAMES

| | | | |
|-----------|-----------------------------|------------------|----------------------|
| Φ 1E | Clock 1 (Phase 1) | SH3 | Shift Gate 3 |
| Φ 2E | Clock 2 (Phase 2) | \overline{RS} | Reset Gate |
| Φ 10 | Clock 1 (Phase 1) | \overline{SP} | Sample and Hold Gate |
| Φ 20 | Clock 2 (Phase 2) | \overline{SGR} | R Switch |
| Φ 1B | Final Stage Clock (Phase 1) | \overline{SGG} | G Switch |
| Φ 2B | Final Stage Clock (Phase 2) | \overline{SGB} | B Switch |
| SS | Ground | \overline{CP} | Clamp Gate |
| OD | Power | OS | Signal Output |
| SH1 | Shift Gate 1 | DOS | Compensation Output |
| SH2 | Shift Gate 2 | NC | Non Connection |

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12 V, V_φ = V_{RS} = V_{SH} = V_{CP} = 5 V (Pulse), f_φ = 0.51 MHz, f_{RS} = 1.0 MHz, Load Resistance = 100 kΩ, t_{INT} (Integration Time) = 10 ms, Light Source = A Light Source + CM500 Filter (t = 1.0 mm))

| CHARACTERISTIC | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|--------------------------------|-------------------------------------|-----|------|-----|----------|-----------|
| Sensitivity (Red) | RR | — | 1.1 | — | V / lx·s | (Note 2) |
| Sensitivity (Green) | RG | — | 1.4 | — | V / lx·s | (Note 2) |
| Sensitivity (Blue) | RB | — | 0.5 | — | V / lx·s | (Note 2) |
| Photo Response Non Uniformity | PRNU (1) | — | 10 | 20 | % | (Note 3) |
| | PRNU (3) | — | 3 | 12 | mV | (Note 4) |
| Register Imbalance | RI | — | — | 3 | % | (Note 5) |
| Saturation Output Voltage | V _{SAT} | 1.0 | 1.5 | — | V | (Note 6) |
| Saturation Exposure | SE | — | 1.07 | — | lx·s | (Note 7) |
| Dark Signal Voltage | V _{DRK} | — | — | 2.0 | mV | (Note 8) |
| Dark Signal Non Uniformity | DSNU | — | — | 3.0 | mV | (Note 9) |
| Total Transfer Efficiency | TTE | 92 | — | — | % | |
| Output Impedance | Z _O | — | 0.5 | 1.0 | kΩ | |
| DC Power Dissipation | P _D | — | 500 | 750 | mW | |
| DC Offset Voltage | V _{OS} | — | 6.0 | — | V | (Note 10) |
| DC Compensation Output Voltage | V _{DOS} | — | 6.0 | — | V | (Note 10) |
| DC Mismatch Voltage | V _{DOS} - V _{DOS} | — | 100 | 300 | mV | (Note 10) |

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$PRNU(1) = \frac{\Delta\bar{\chi}}{\bar{\chi}} \times 100(\%)$$

When $\bar{\chi}$ is average of total signal output and $\Delta\bar{\chi}$ is the maximum deviation from $\bar{\chi}$. The amount of incident light is shown below.

$$\text{Red} = \frac{1}{2} \text{SE}$$

$$\text{Green} = \frac{1}{2} \text{SE}$$

$$\text{Bule} = \frac{1}{4} \text{SE}$$

Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (TYP.).

Note 5: RI is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$RI = \frac{\sum_{n=1}^{3647} |\chi_n - \chi_{n+1}|}{3647 \times \bar{\chi}} \times 100(\%)$$

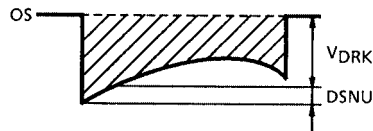
Where χ_n and χ_{n+1} are signal outputs of each pixel. $\bar{\chi}$ is average of total signal outputs.

Note 6: V_{SAT} is defined as minimum saturation output of all effective pixels.

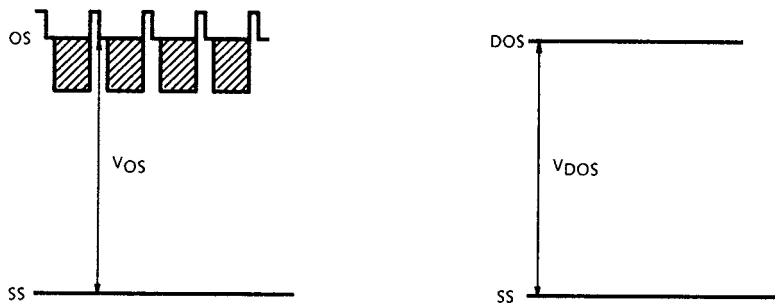
Note 7: Definition of SE: $SE = \frac{V_{SAT}}{R_G}$

Note 8: V_{DRK} is defined as average dark signal voltage of all effective pixels.

Note 9: DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark voltage.



Note 10: DC Signal Output Voltage and DC Compensation Output Voltage are defined as follows:



OPERATING CONDITION

| CHARACTERISTIC | | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---------------------------------|-----------|---------------------|---------------------------------|-----------------------------|-----------------------------|------|-----------|
| Clock Pulse Voltage | "H" Level | $V_{\phi 0, E}$ | 4.5 | 5.0 | 5.5 | V | |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| Final Stage Clock Pulse Voltage | "H" Level | $V_{\phi B}$ | 4.5 | 5.0 | 5.5 | V | |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| Shift Pulse Voltage | "H" Level | V_{SH} | $V_{\phi 0, E} \text{ "H"} - 1$ | $V_{\phi 0, E} \text{ "H"}$ | $V_{\phi 0, E} \text{ "H"}$ | V | (Note 11) |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| Reset Pulse Voltage | "H" Level | $\overline{V_{RS}}$ | 4.5 | 5.0 | 5.5 | V | |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| Sample and Hold Pulse Voltage | "H" Level | $\overline{V_{SP}}$ | 4.5 | 5.0 | 5.5 | V | (Note 12) |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| RGB Switch Pulse Voltage | "H" Level | $\overline{V_{SG}}$ | 4.5 | 5.0 | 5.5 | V | |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| Clamp Pulse Voltage | "H" Level | $\overline{V_{CP}}$ | 4.5 | 5.0 | 5.5 | V | (Note 13) |
| | "L" Level | | 0.0 | 0.2 | 0.5 | | |
| Power Supply Voltage | | V_{DD} | 11.4 | 12.0 | 13.0 | V | |

Note 11: $V_{\phi 0, E}$ "H" means the high level voltage of $V_{\phi 0}$ and $V_{\phi E}$ when SH pulse is high level.

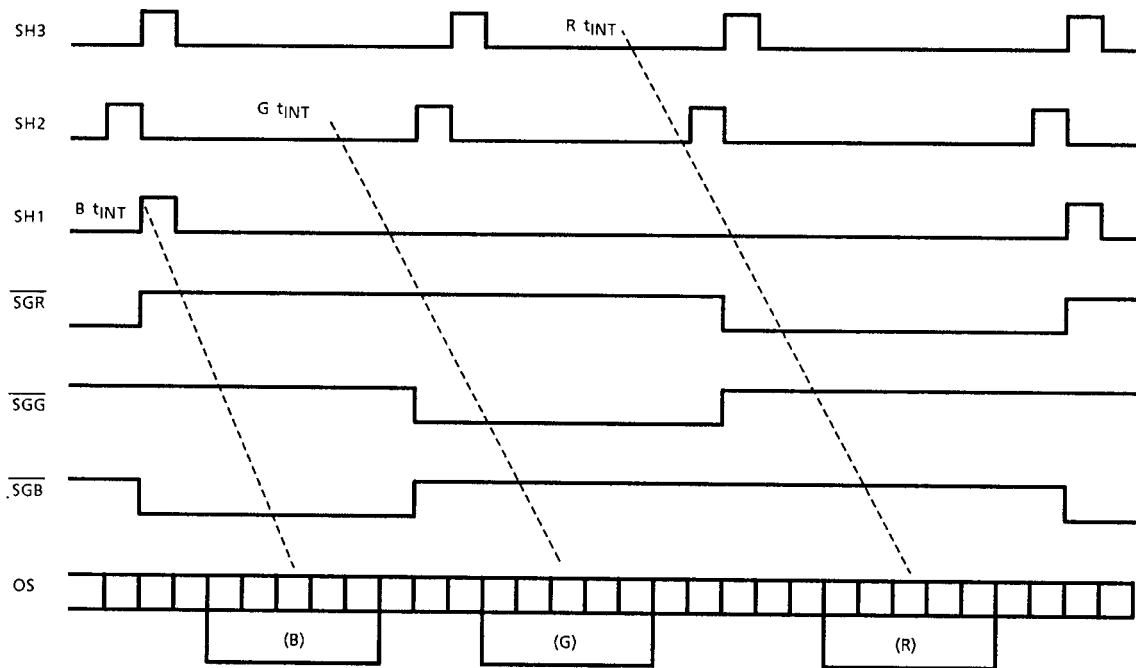
Note 12: Supply "L" level to \overline{SP} terminal when sample-and-hold circuit is not used.

Note 13: Supply \overline{SH} (inversed pulse of SH) to \overline{CP} terminal when clamp circuit is not used.

CLOCK CHARACTERISTICS (Ta = 25°C)

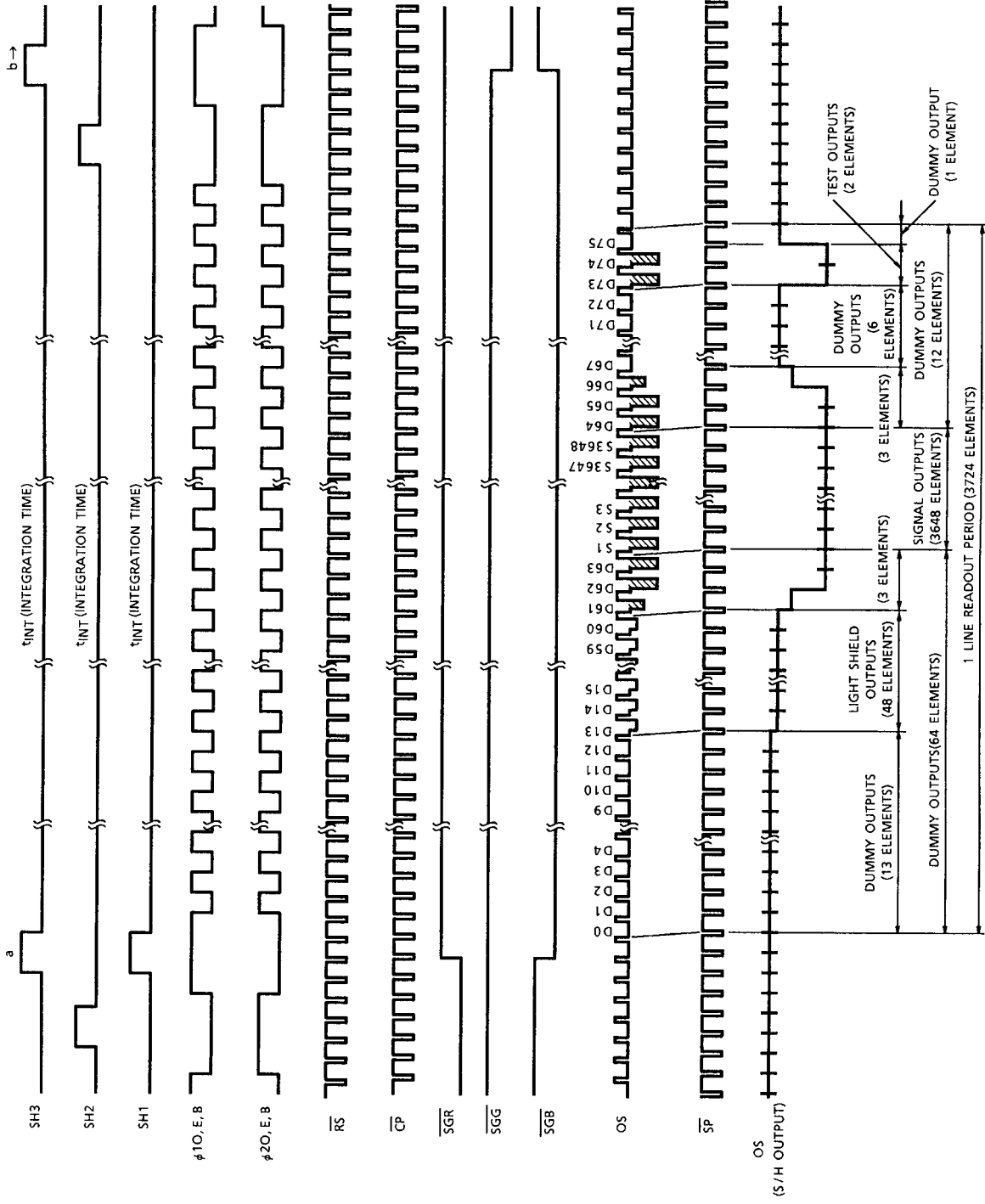
| CHARACTERISTIC | SYMBOL | MIN | TYP. | MAX | UNIT |
|----------------------------------|---------------------|-----|------|-----|------|
| Clock Pulse Frequency | f_{ϕ} | — | 0.5 | 2.0 | MHz |
| Reset Pulse Frequency | $\overline{f_{RS}}$ | — | 1.0 | 4.0 | MHz |
| Sample and Hold Pulse Frequency | $\overline{f_{SP}}$ | — | 1.0 | 4.0 | MHz |
| Clamp Pulse Frequency | $\overline{f_{CP}}$ | — | 1.0 | 4.0 | MHz |
| Clock Capacitance | $C_{\phi 0, E}$ | — | 500 | — | pF |
| Final Stage Clock Capacitance | $C_{\phi B}$ | — | 10 | — | pF |
| Shift Gate Capacitance | C_{SH} | — | 200 | — | pF |
| Reset Gate Capacitance | $\overline{C_{RS}}$ | — | 10 | — | pF |
| Sample and Hold Gate Capacitance | $\overline{C_{SP}}$ | — | 10 | — | pF |
| RGB Switch Pulse Capacitance | $\overline{C_{SG}}$ | — | 10 | — | pF |
| Clamp Gate Capacitance | $\overline{C_{CP}}$ | — | 10 | — | pF |

APPLICATION NOTE

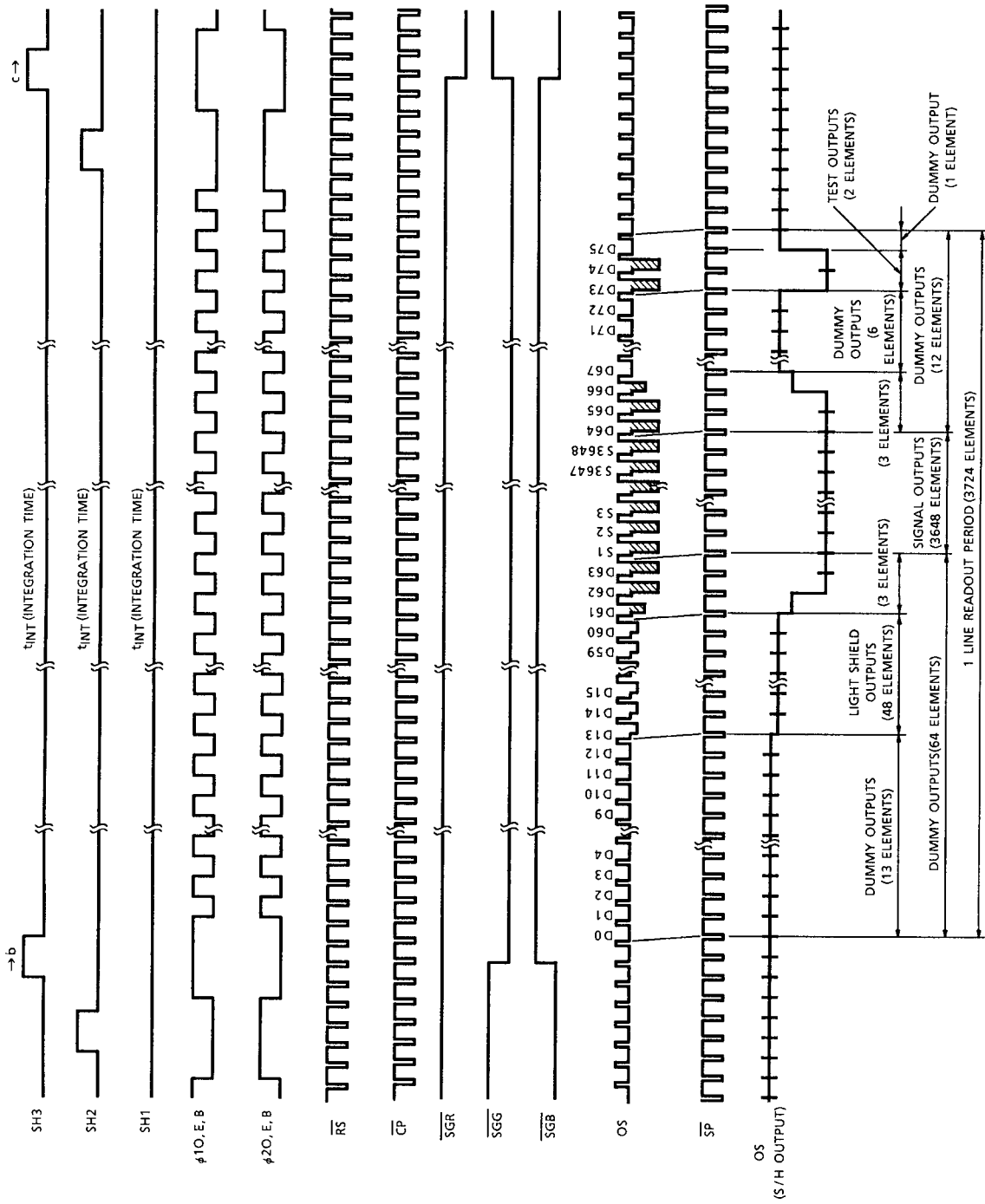


- a) You drive TCD2301C by above timing, so you can get the three output signal of nearly equal level.
- b) In switching “SGR”, “SGG” and “SGB”, asynchronous switching operation with clock pulse, shift pulse or any other input pulses timing, is possible. (It is not necessary to switch above timing shown in figure.) But care should be taken not to make more than two switches to “L” level at the same time.

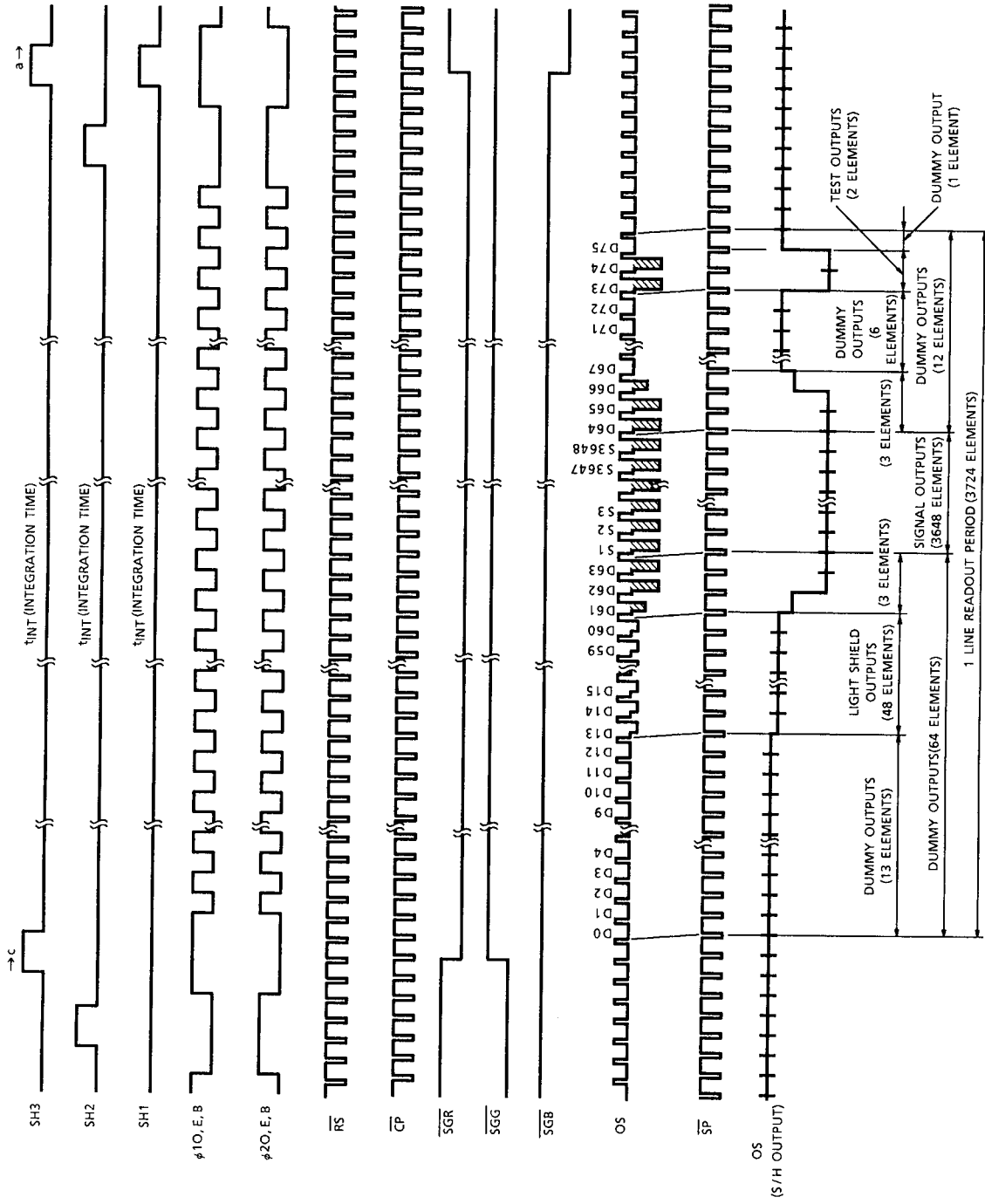
TIMING CHART 1



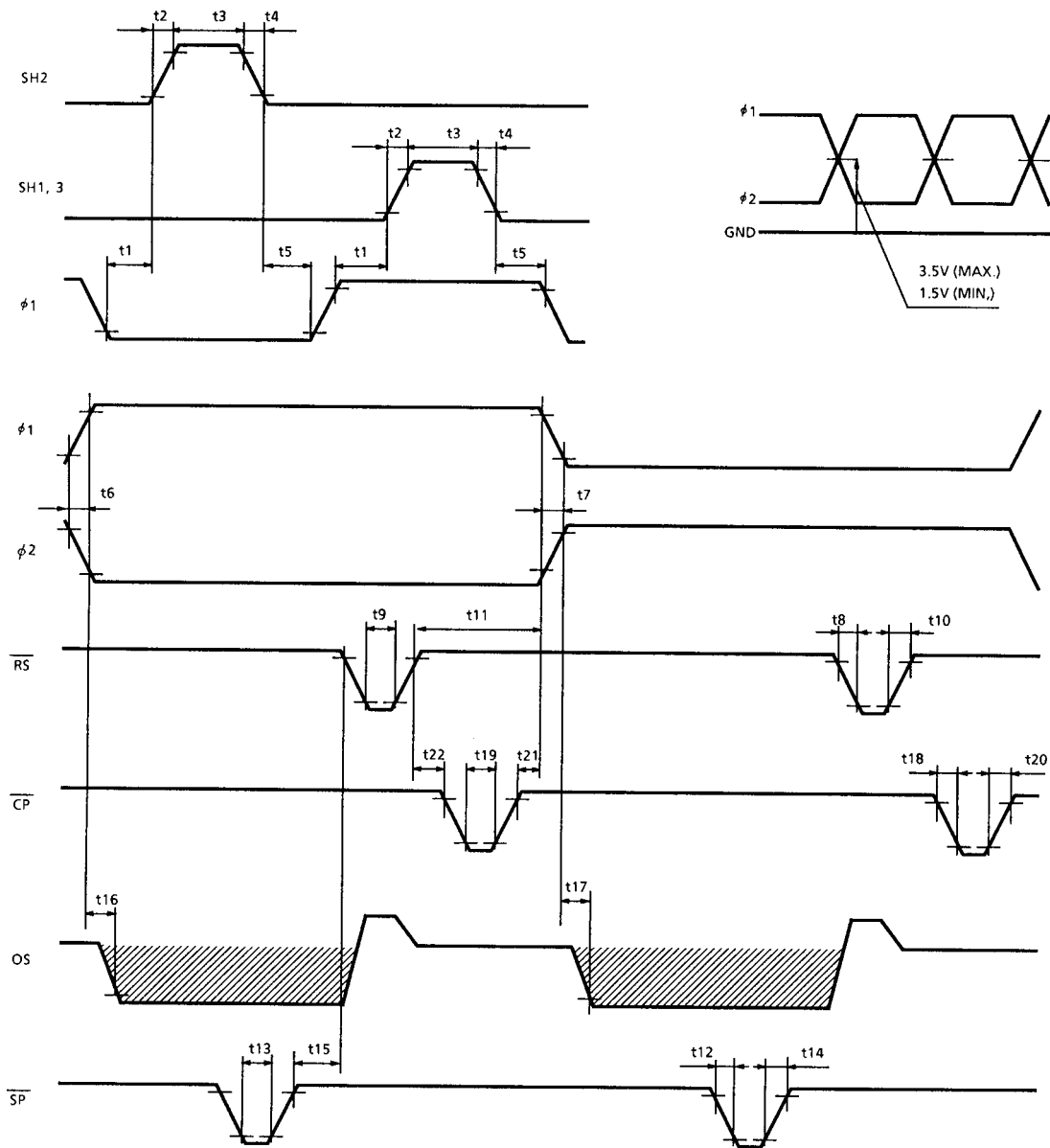
TIMING CHART 2



TIMING CHART 3



TIMING REQUIREMENTS



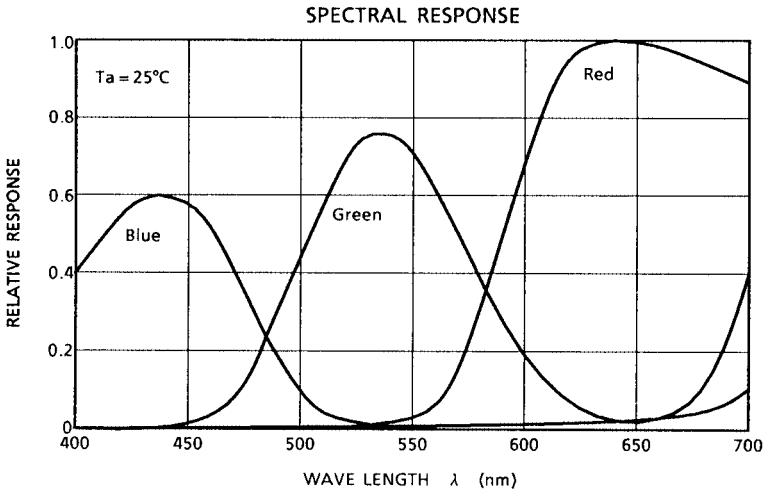
TIMING REQUIREMENTS (Cont.)

| CHARACTERISTIC | SYMBOL | MIN | TYP. (Note 14) | MAX | UNIT |
|--|----------|-----|-------------------|-----|------|
| Pulse Timing of SH and $\phi_{1,0}$ | t1, t5 | 0 | 1000 | — | ns |
| SH Pulse Rise Time, Fall Time | t2, t4 | 0 | 50 | — | ns |
| SH Pulse Width | t3 | 500 | 1000 | — | ns |
| ϕ_1, ϕ_2 Pulse Rise Time, Fall Time | t6, t7 | 0 | 50 | — | ns |
| \overline{RS} Pulse Rise Time, Fall Time | t8, t10 | 0 | 20 | — | ns |
| \overline{RS} Pulse Width | t9 | 40 | 250 | — | ns |
| Pulse Timing of ϕ_{1B}, ϕ_{2B} and \overline{RS} | t11 | 120 | 300 | — | ns |
| \overline{SP} Pulse Rise Time, Fall Time | t12, t14 | 0 | 20 | — | ns |
| \overline{SP} Pulse Width | t13 | 70 | 100 | — | ns |
| Pulse Timing of \overline{SP} and \overline{RS} | t15 | 0 | 50 | — | ns |
| Video Data Delay Time (Note 15) | t16, t17 | — | 70 | — | ns |
| \overline{CP} Pulse Rise Time, Fall Time | t18, t20 | 0 | 20 | — | ns |
| \overline{CP} Pulse Width | t19 | 100 | 200 | — | ns |
| Pulse Timing of ϕ_{1B}, ϕ_{2B} and \overline{CP} | t21 | 20 | 50 | — | ns |
| Pulse Timing of \overline{RS} and \overline{CP} | t22 | 0 | 50 | — | ns |

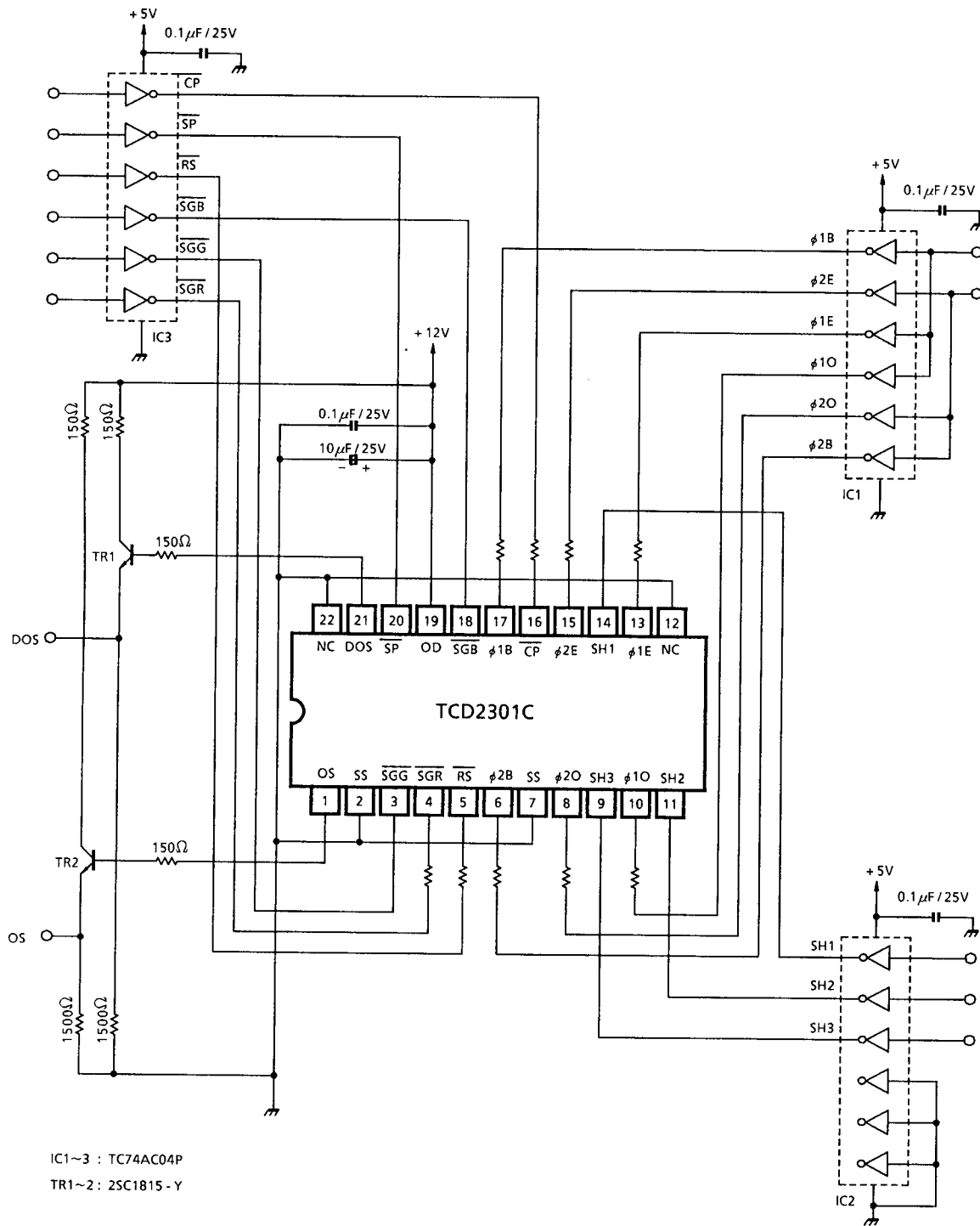
Note 14: TYP. is the case of $f_{\overline{RS}} = 1.0\text{MHz}$

Note 15: Load resistance is 100k Ω

TYPICAL SPECTRAL RESPONSE



TYPICAL DRIVE CIRCUIT



CAUTION**1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but interior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting pliers or pincer.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.

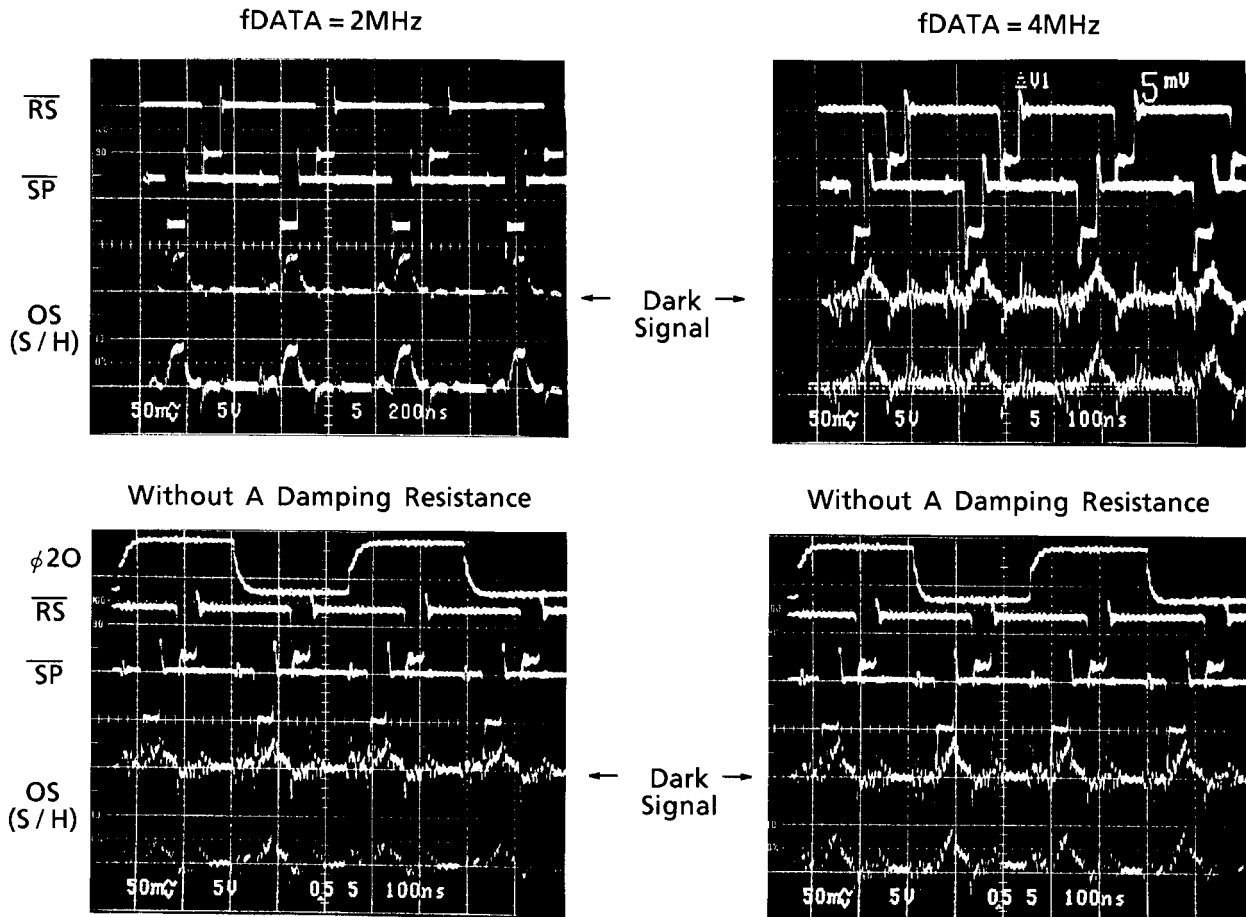
Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

<Application note>

EVEN-ODD UNBALANCE

When High-speed driving standard level of odd-even bits is often unbalanced. For that reason when high-speed driving CCD you should put a damping resistance in input ϕ pin.

1. WAVEFORM (Sample and Hold ON)



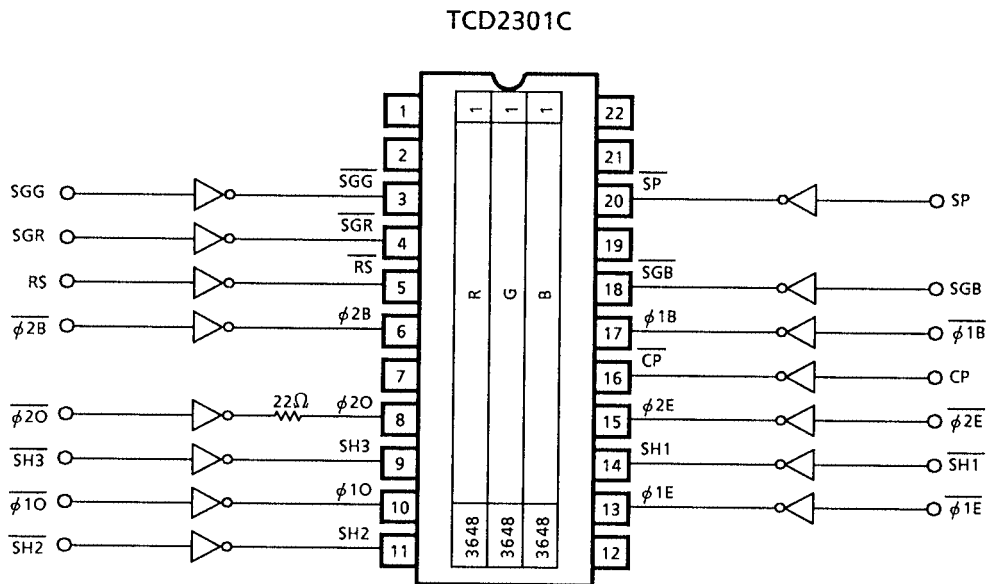
2. MEASUREMENT CONDITION

$T_a=25^\circ\text{C}$, $V_{AD}=V_{DD}=12\text{V}$,
 $V_{\phi 1E}=V_{\phi 10}=V_{\phi 1B}=V_{\phi 2E}=V_{\phi 20}=V_{\phi 2B}=V_{\overline{RS}}=V_{\overline{CP}}=V_{\overline{SP}}=V_{SH1}=V_{SH2}=V_{SH3}=5\text{V}$ (Pulse),
 Light Source=Daylight Fluorescent Lamp.

| | | |
|--------------|-----------|----------------|
| Oscilloscope | Tektronix | 2465A (400MHz) |
| Probe | P6136 | 10.8pF |

3. DRIVE CIRCUIT (with a damping resistance)

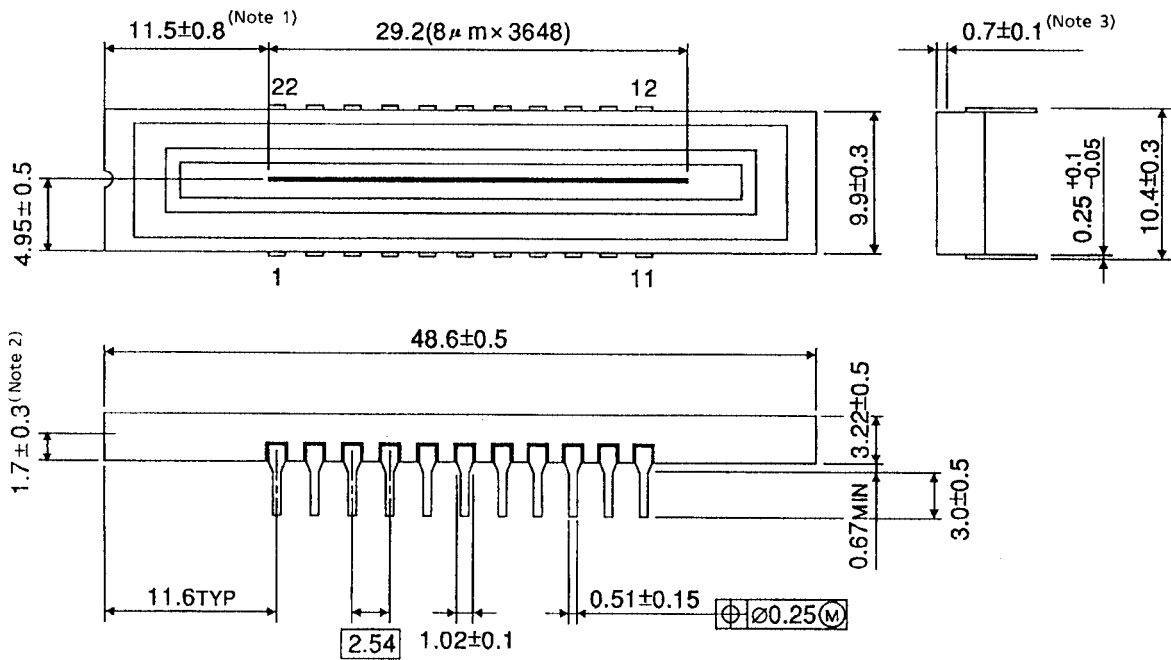
Please put a damping resistance in input $\phi 20$ (22Ω).



PACKAGE DIMENSIONS

WDIP22-C-400-2.54A (C)

Unit : mm



Note 1: No.1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.

Note 2: TOP OF CHIP TO BOTTOM OF PACKAGE.

Note 3: GLASS THICKNESS (n=1.5)

Weight: 4.8g (Typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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