1GB – 128Mx72 DDR SDRAM REGISTERED w/PLL, FBGA

FEATURES

- Double-data-rate architecture
- DDR266 and DDR333
  - JEDEC design specifications
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2,5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power Supply:
  - V_{CC} = V_{CCQ} = +2.5V ±0.2V (100, 133 and 166MHz)
- 184 pin DIMM package
- PCB height:
  - D3: 29.97mm (1.18")

NOTE: Consult factory for availability of:
- Lead-Free Products
- Vendor source control options
- Industrial temperature options

DESCRIPTION

The WV3EG128M72EFSR is a 128Mx72 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of eighteen 64Mx8 DDR components in FBGA packages mounted on a 184 Pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lenths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-t_{RCD}-t_{RP}	2.5-3-3	2-2-2	2.5-3-3

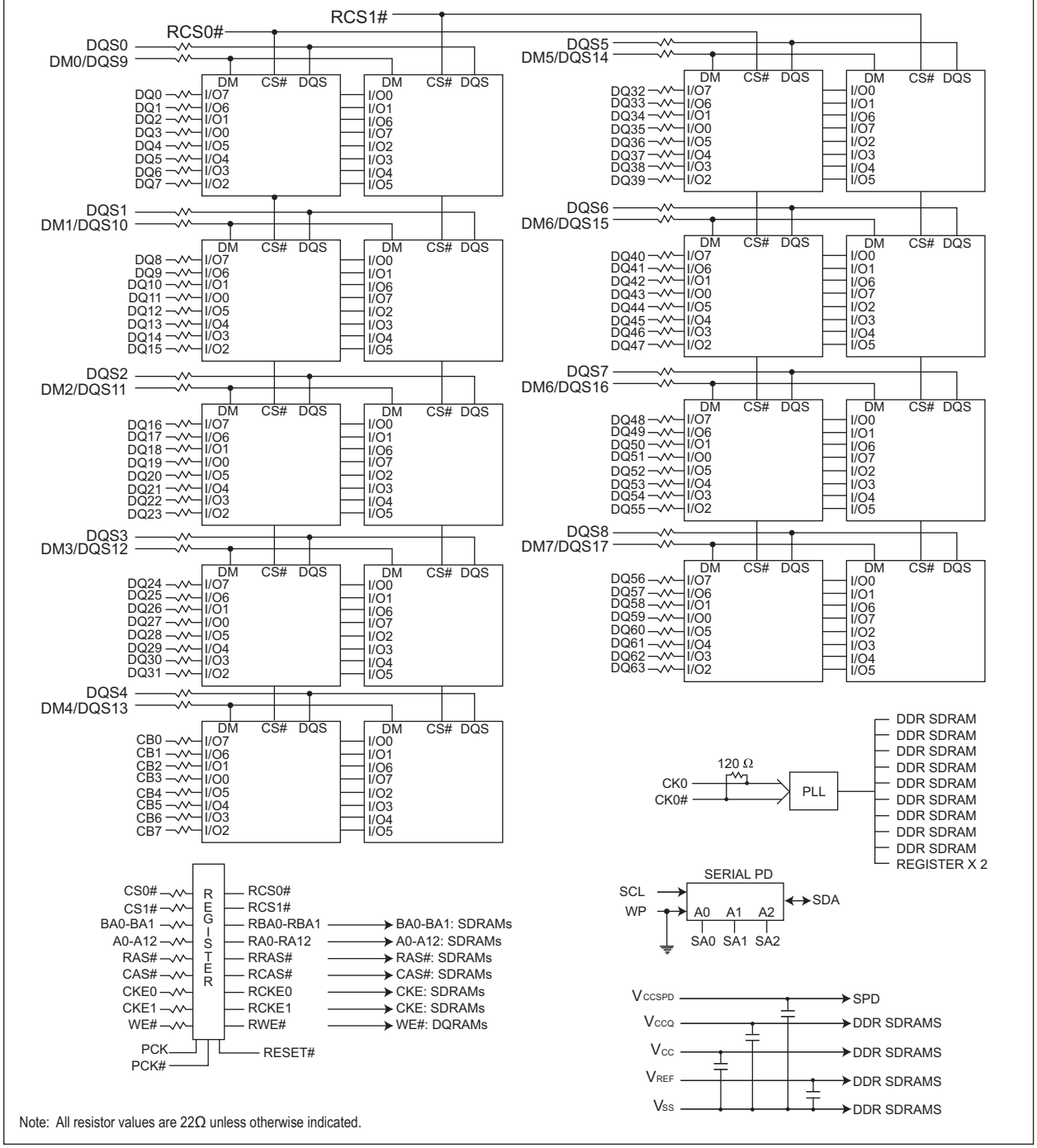
PIN CONFIGURATION

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DM8/DQS17
3	V_{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	CB6
5	DQS0	51	CB3	97	DM0/DQS9	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	RESET#	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	56	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DM1/DQS10	153	DQ44
16	NC	62	V_{CCQ}	108	V_{CC}	154	RAS#
17	NC	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	CS1#
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V_{CCQ}	76	NC	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	V_{CCQ}
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	NC	136	V_{CCQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	CK0#	184	V_{CCSPD}

PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check bits
DQS0-DQS8	Data Strobe Input/Output
CK0	Clock Input
CK0#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
DM0-DM8	Data-in Mask
WE#	Write Enable
V_{CC}	Power Supply
V_{CCQ}	Power Supply for DQS
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V_{CCID}	V_{CC} Indentification Flag
NC	No Connect
RESET#	Reset Enable

FUNCTIONAL BLOCK DIAGRAM



Note: All resistor values are 22Ω unless otherwise indicated.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 to 3.6	V
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	18	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC CHARACTERISTICS

$0°C \leq T_A \leq 70°C$, $V_{CC} = 2.5V \pm 0.2V$

Parameter	Symbol	Min	Max	Unit
Supply Voltage (for device with nominal V_{CC} of 2.5V)	V_{CC}	2.3	2.3	V
I/O Supply Voltage	V_{CCQ}	2.3	2.3	V
I/O Reference Voltage	V_{REF}	V_{CCQ}/2-50mV	V_{CCQ}/2+50mV	V
I/O Termination Voltage (systems)	V_{TT}	V_{REF} -0.04	V_{REF} +0.04	V
Input Logic High Voltage	V_{IH}(DC)	V_{REF} +0.15	V_{CCQ} +0.3	V
Input Logic Low Voltage	V_{IL}(DC)	-0.3	V_{REF} -0.15	V
Input Voltage Level, CK and CK# inputs	V_{IN}(DC)	-0.3	V_{CCQ} +0.3	V
Input Differential Voltage, CK and CK# inputs	V_{ID}(DC)	0.3	V_{CCQ} +0.6	V
Input Crossing Point Voltage, CK and CK# inputs	V_{IX}(DC)	1.15	1.35	V
Input Leakage Current	I_L	-2	2	uA
Output Leakage Current	I_{OZ}	-5	5	uA
Output High Current (Normal strength driver); $V_{OUT} = V_{TT}$ + 0.84V	I_{OH}	-16.8		mA
Output High Current (Normal strength driver); $V_{OUT} = V_{TT}$ - 0.84V	I_{OL}	16.8		mA
Output High Current (Half strength driver); $V_{OUT} = V_{TT}$ + 0.45V	I_{OH}	-9		mA
Output High Current (Half strength driver); $V_{OUT} = V_{TT}$ - 0.45V	I_{OL}	9		mA

Notes:

1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5*V_{CCQ} of the transmitting device and must track variations in the dc level of the same.
6. These charactericteristics obey the SSTL-2 class II standards.

CAPACITANCE

$T_A = 25°C$. f = 1MHz, $V_{CC} = 2.5V$

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	11	pF
Input Capacitance (RAS#, CAS#, WE#)	C_{IN2}	11	pF
Input Capacitance (CKE0, CKE1)	C_{IN3}	11	pF
Input Capacitance (CK0#, CK0)	C_{IN4}	12	pF
Input Capacitance (CS0#, CS1#)	C_{IN5}	11	pF
Input Capacitance (DQM0-DQM8)	C_{IN6}	15	pF
Input Capacitance (BA0-BA1)	C_{IN7}	11	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C_{OUT}	15	pF
Data input/output capacitance (CB0-CB7)	C_{OUT}	15	pF

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Recommended operating conditions, 0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V

Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR333@ CL=2.5 Max	DDR266@ CL=2 Max	DDR266@ CL=2.5 Max	Units
Operating Current	I_{DD0}	One device bank; Active - Precharge; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	4140	4140	4140	mA
Operating Current	I_{DD1}	One device bank; Active-Read-Precharge Burst = 2; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle.	4680	4680	4680	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device banks idle; Power-down mode; t_{CK}=t_{CK} (MIN); CKE=(low)	180	180	180	rnA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; t_{CK}=t_{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM.	1620	1620	1620	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-Down mode; t_{CK} (MIN); CKE=(low)	1260	1260	1260	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS} (MAX); t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	1800	1800	1800	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T_{CK}= T_{CK} (MIN); I_{OUT} = 0mA.	4770	4770	4770	mA
Operating Current	I_{DD4W}	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle.	4590	4590	4590	rnA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RC} (MIN)	7020	7020	7020	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	180	180	180	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	9090	9000	9000	mA

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Recommended operating conditions, 0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V

Includes PLL and register power

Parameter	Symbol	Conditions	DDR333@ CL=2.5 Max	DDR266@ CL=2 Max	DDR266@ CL=2.5 Max	Units
Operating Current	I_{DD0}	One device bank; Active - Precharge; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	4725	4725	4725	mA
Operating Current	I_{DD1}	One device bank; Active-Read-Precharge Burst = 2; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle.	5265	5265	5265	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device banks idle; Power-down mode; t_{CK}=t_{CK} (MIN); CKE=(low)	180	180	180	mA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; t_{CK}=t_{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM.	1930	1930	1930	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-Down mode; t_{CK} (MIN); CKE=(low)	1260	1260	1260	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS} (MAX); t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	2110	2110	2110	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T_{CK}= T_{CK} (MIN); I_{OUT} = 0mA.	5355	5355	5355	mA
Operating Current	I_{DD4W}	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle.	5535	5175	5175	mA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RC} (MIN)	7640	7605	7605	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	455	455	455	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	9675	9585	9585	mA

DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{RAS}=7*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout=0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
     Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend:

A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

0°C ≤ T_A ≤ +70°C; V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

AC Characteristics			335		262		265			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Access window of DQs from CK, CK#		t_{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	16
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	16
Clock cycle time	CL=3	t_{CK} (3)	6	13	7.5	13	7.5	13	ns	22
	CL=2.5	t_{CK} (2.5)	6	12	7.5	12	7.5	12	ns	22
	CL=2	t_{CK} (2)	7.5	12	7.5	12	10	12	ns	22
DQ and DM input hold time relative to DQS		t_{DH}	0.45		0.5		0.5		ns	14,17
DQ and DM input setup time relative to DQS		t_{DS}	0.45		0.5		0.5		ns	14,17
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		1.75		ns	17
Access window of DQS from CK, CK#		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.4		0.5		0.5	ns	13,14
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}	
Half clock period		t_{HP}	t_{CH}, t_{CL}		t_{CH}, t_{CL}		t_{CH}, t_{CL}		ns	18
Data-out high-impedance window from CK, CK#		t_{HZ}		+0.7		+0.75		+0.75	ns	8,19
Data-out low-impedance window from CK, CK#		t_{LZ}	-0.7		-0.75		-0.75		ns	8,20
Address and control input hold time (fast slew rate)		t_{IHf}	0.75		0.90		0.90		ns	6
Address and control input set-up time (fast slew rate)		t_{ISf}	0.75		0.90		0.90		ns	6
Address and control input hold time (slow slew rate)		t_{IHs}	0.8		1		1		ns	6
Address and control input setup time (slow slew rate)		t_{ISs}	0.8		1		1		ns	6
Address and control input pulse width (for each input)		t_{IPW}	2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time		t_{MRD}	12		15		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	13,14
Data hold skew factor		t_{QHS}		0.55		0.75		0.75	ns	
ACTIVE to PRECHARGE command		t_{RAS}	42	70,000	45	120,000	45	120,000	ns	15
ACTIVE to READ with Auto precharge command		t_{RAP}	18		15		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		t_{RC}	60		60		65		ns	
AUTO REFRESH command period		t_{RFC}	72		75		75		ns	21

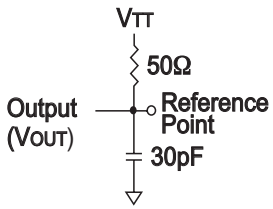
DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

Notes 1-5, 7; notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

AC Characteristics		335		262		265			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
ACTIVE to READ or WRITE delay	t_{RCD}	18		20		20		ns	
PRECHARGE command period	t_{RP}	18		20		20		ns	
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	19
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	12		15		15		ns	
DQS write preamble	t_{WPRE}	0.25		0.25		0.25		t_{CK}	
DQS write preamble setup time	t_{WPRES}	0		0		0		ns	10,11
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	9
Write recovery time	t_{WR}	15		15		15		ns	
Internal WRITE to READ command delay	t_{WTR}	1		1		1		t_{CK}	
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8	µs	12
Exit SELF REFRESH to non-READ command	t_{XSNR}	75		75		75		ns	
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		t_{CK}	

Notes

1. All voltages referenced to V_{SS}
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at normal reference / supply voltage levels, but the related specifications and device operations are guaranteed for the full voltage range specified.
3. Outputs are measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are defined in the SSTL_2 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [high] level).
6. Command/Address input slew rate = 0.5V/ns. For -75 with slew rates 1V/ns and faster, t_{IS} and t_{IH} are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. t_{IH} has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
7. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x V_{CCQ} is recognized as LOW.
8. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) and begins driving (LZ).
9. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
10. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
11. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be high during this time, depending on t_{DQSS}.
12. The refresh period is 64ms. This equates to an average refresh rate of 15.625µs (256Mb component) or 7.8125µs (512 Mb component). However, an AUTO REFRESH command must be asserted at least once every 140.6µs (256 Mb component) or 70.3µs (512Mb component); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
13. The valid data window is derived by achieving other specifications - t_{HP} ($t_{CK/2}$), t_{DQSQ}, and t_{QH} (t_{QH} = t_{HP} - t_{QHS}). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycled variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
14. Referenced to each output group: x4 = DQS with DQ0-DQ4.
15. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS} (MIN) can be satisfied prior to the internal precharge command being issued.
16. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
17. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100mV/ns reduction in slew rate. If slew rates exceed 4V/ns, functionality is uncertain.
18. t_{HP} min is the lesser of t_{CL} min and t_{CH} min actually applied to the device CK and CK# inputs, collectively during bank active.
19. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for t_{HZ} (MAX) and last DVW. t_{HZ} (MAX) will prevail over the t_{DQSCK} (MAX) + t_{RPST} (MAX) condition. t_{LZ} (MIN) will prevail over t_{DQSCK} (MIN) + PRE (MAX) condition.
20. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
21. CKE must be active (High) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{REF} later.
22. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).

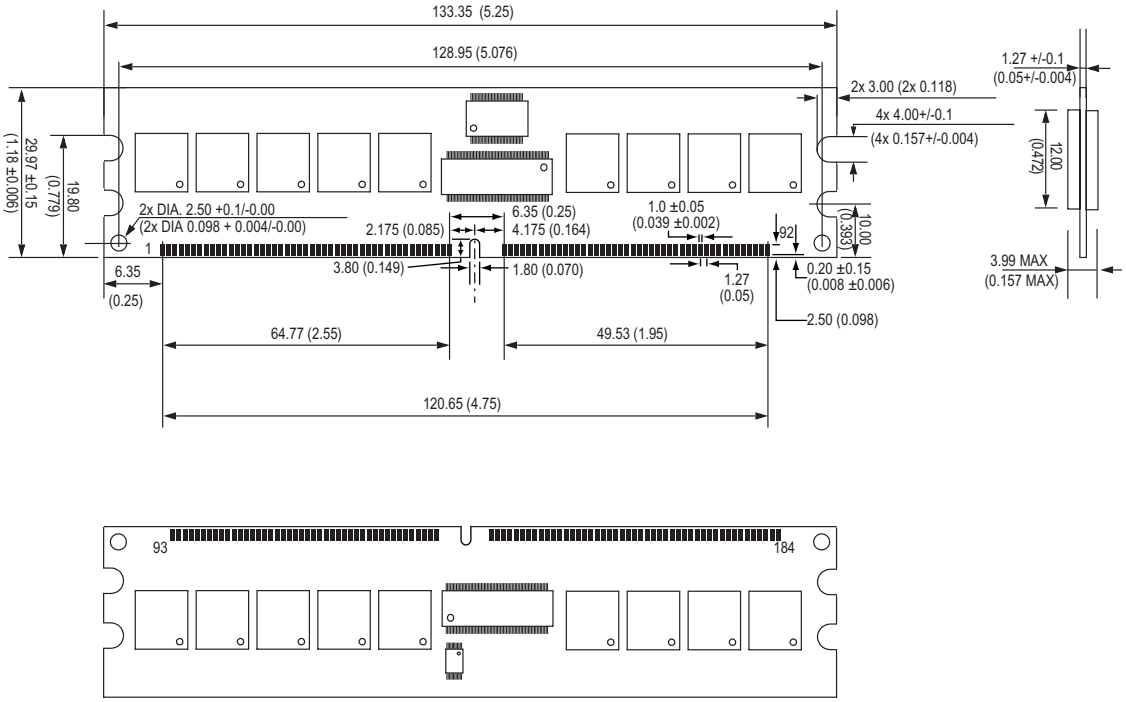
ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3EG128M72EFSR335D3	166MHz/333Mb/s	2.5	3	3	29.97 (1.18")
WV3EG128M72EFSR262D3	133MHz/266Mb/s	2	2	2	29.97 (1.18")
WV3EG128M72EFSR265D3	133MHz/266Mb/s	2.5	3	3	29.97 (1.18")

NOTES:

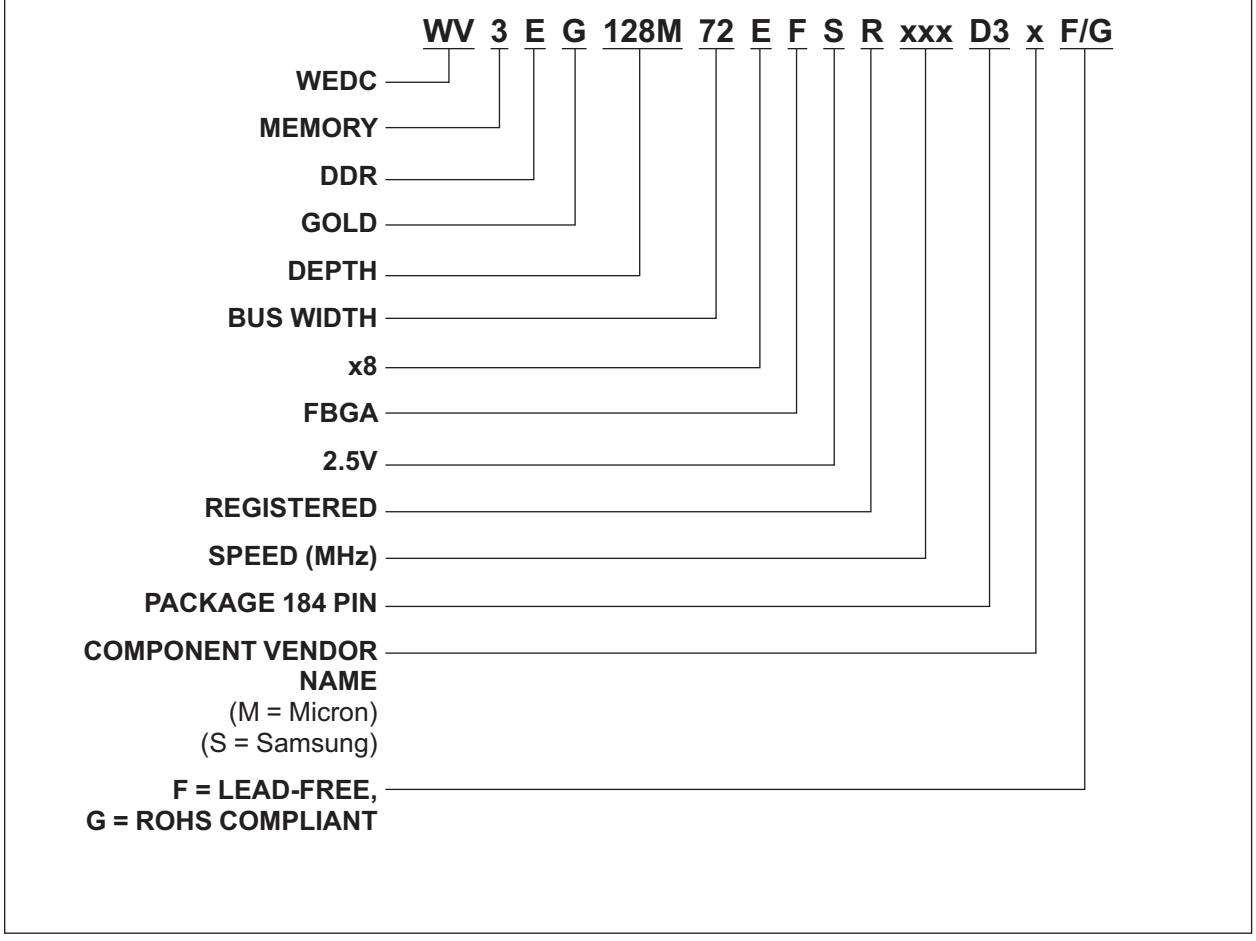
- Consult Factory for availability of Lead-Free products. (F = Lead-Free, G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

1GB - 128Mx72 DDR SDRAM REGISTERED w/PLL, FBGA

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	3-05	Advanced