N-Ch 600V Fast Switching MOSFETs

General Description

The UI(D)4N60 is the highest performance trench P-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The UI(D)4N60 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

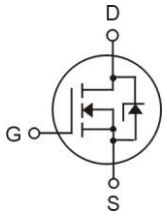
Product Summery

BV_{DSS}	$R_{DS(ON)}$	ID
600V	2.25Ω	3.2A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

TO-251/TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter		TO-251/TO-252	Unites
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current –Continuous(T_C = 25℃)		3.2	A
	–Continuous(T_C = 100℃)		1.9	A
I_{DM}	Drain Current –Pulsed	(Note1)	12.8	A
V_{GSS}	Gate-Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note2)	63	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25℃)		57	W
	-Derate above 25℃		0.45	W/℃
T_{J1} T_{STG}	Operating and Storage Temperature Range		-55 to + 150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8” from case for 5 seconds		300	℃

Thermal Data

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.2	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	50	℃/W

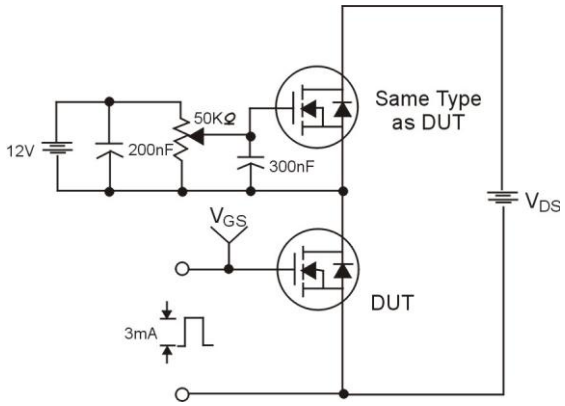
Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

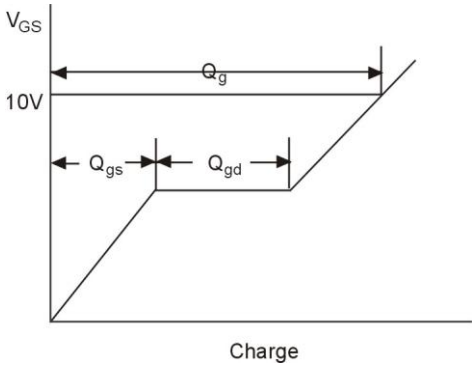
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250μA	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μ A, Referenced to 25℃	--	0.6	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V (T_C = 25℃)	--	--	10	μA
		V_{DS} = 480 V, V_{GS} = 0 V (T_C = 125℃)	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain-Source On-resistance	V_{GS} = 10 V, I_D = 1.6A	--	2.25	2.81	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 1.6 A (Note 4)	--	2.6	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHZ	--	500	650	pF
C_{oss}	Output Capacitance		--	53.2	69	pF
C_{rss}	Reverse Transfer Capacitance		--	7.0	9.1	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 3.2A, R_G = 25 Ω (Note 4, 5)	--	11	27	ns
t_r	Turn-On Rise Time		--	20	48	ns
$t_{d(off)}$	Turn-Off Delay Time		--	30	72	ns
t_f	Turn-Off Fall Time		--	19	46	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 3.2A, V_{GS} = 10 V (Note 4, 5)	--	14.5	20	nC
Q_{gs}	Gate-Source Charge		--	3.4	--	nC
Q_{gd}	Gate-Drain Charge		--	7.0	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.2	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.2A	--	1.13	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS}= 0 V,I_S = 3.2A, dI_F/dt = 100 A/μ s (Note 4)	--	561	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.8	--	μ C

Notes:

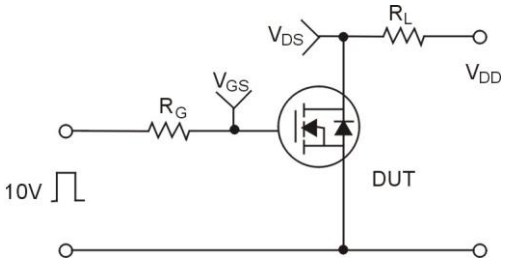
1. Repetitive Rating：Pulse width limited by maximum junction temperature
2. L = 10mH, I_{AS} = 3.4A, V_{DD} = 50V, R_G =25Ω, Starting T_J = 25℃
3. I_{SD} ≤ 3.2A, di/dt ≤ 200A/μS, V_{DD} ≤ BV_{DSS}, Starting T_J = 25℃
4. Pulse Test：Pulse width ≤ 300μS, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

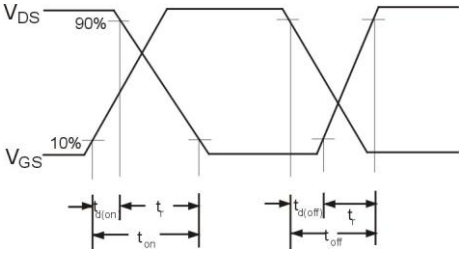
Gate Charge Test Circuit & Waveform



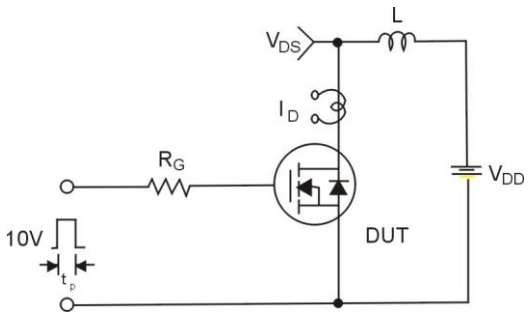


Resistive Switching Test Circuit & Waveforms

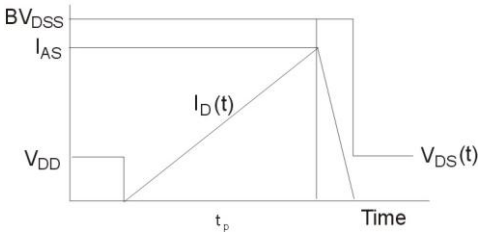




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms