N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
240V	6.0Ω	1.0A	VN2406L
240V	10Ω	1.0A	VN2410L

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

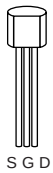
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor controls
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Package Options



S G D

TO-92

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	0.9A	5.0A	1.0W	125	170	0.18A	1.7A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage		240			V	V_{GS} = 0V, I_D = 0.1mA
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = 20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0V, V_{DS} = 120V
					500		V_{GS} = 0V, V_{DS} = 120V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.0			A	V_{GS} = -10V, V_{DS} = 15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	All			10	Ω	V_{GS} = 2.5V, I_D = 0.1A
		VN2410			10		V_{GS} = 10V, I_D = 0.5A
		VN2406			6		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	1.4	%/°C	V_{GS} = 10V, I_D = 0.55A
G_{FS}	Forward Transconductance		300			m℧	V_{DS} = 10V, I_D = 0.5A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0V, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				20		
$t_{d(ON)}$	Turn-ON Delay Time				8	ns	V_{DD} = 60V I_D = 0.4A R_{GEN} = 25Ω
t_r	Rise Time				8		
$t_{d(OFF)}$	Turn-OFF Delay Time				23		
t_f	Fall Time				24		
V_{SD}	Diode Forward Voltage Drop	VN2410		1.2		V	V_{GS} = 0V, I_{SD} = 0.19A
		VN2406		1.2		V	V_{GS} = 0V, I_{SD} = 0.8A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit