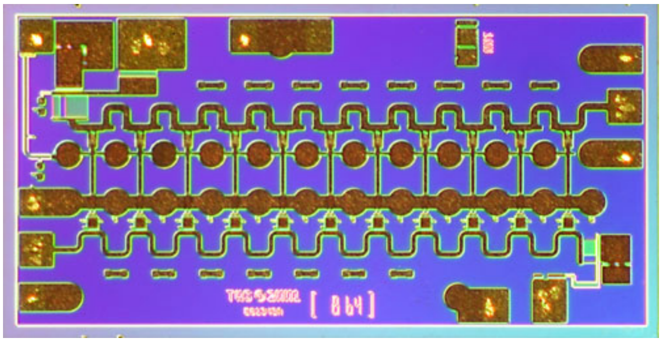
TriQuint SEMICONDUCTOR

TGA4803

DC to >50 GHz MPA with AGC

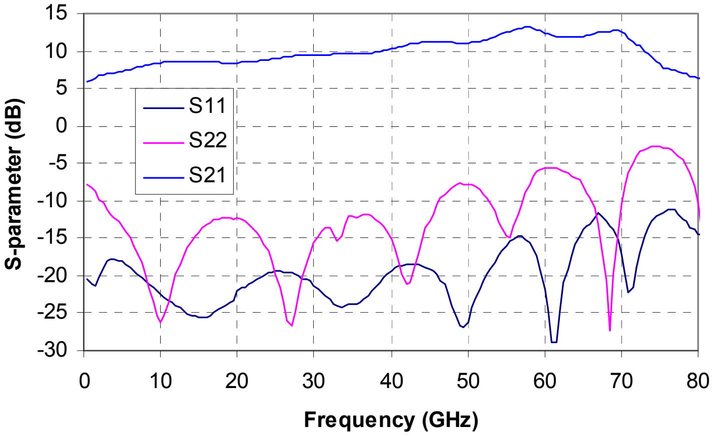


Key Features and Performance

- 0.15um pHEMT Technology
- DC to >50GHz Linear BW
- 8dB Gain, 14dBm @ P1dB
- Group Delay Ripple +/- 6ps to 50 GHz
- <10ps Edge Rates (20/80)
- 3.5Vpp 43Gb/s NRZ PRBS
- Bias: Vd=6.5V, 100mA
- Chip Size: 1.90 x 1.09 x 0.10 mm

Primary Applications

- Test Equipment
- Ultra Wideband
- 43Gb/s OC768 EAM Driver
- 43Gb/s OC768 Gain Stage:



Description

The TriQuint TGA4803 is a medium power wideband AGC amplifier that typically provides 8dB small signal gain with 3dB AGC range. Typical input and output return loss is >10dB. Typical Noise Figure is 5dB at 3GHz. Typical saturated output power is 17dBm. Small signal 3dB BW is >50GHz. RF ports are DC coupled enabling the user to customize system corner frequencies.

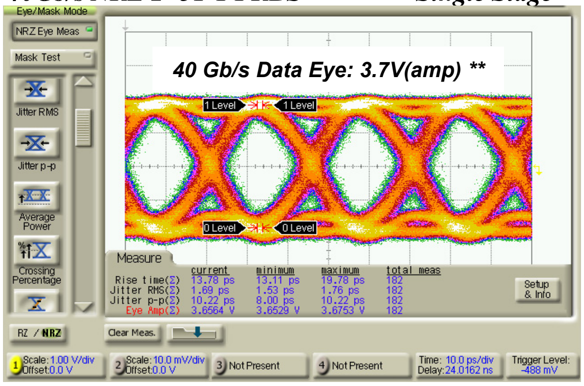
The TGA4803 is an excellent choice for 43Gb/s NRZ applications. The TGA4803 is capable of driving a single Electro-Absorptive optical Modulator (EAM) with electrical Non-Return to Zero (NRZ) data. In addition, the TGA4803 may also be used as a transmit predriver or a receive gain block.

Drain bias may be applied through the output port for best efficiency or through the on-chip drain termination. Three stages in cascade demonstrated 3.8Vpp output voltage swing with 350mV at the input when stimulated with 43Gb/s 2^31-1prbs NRZ data.

The TGA4803 requires off-chip decoupling and blocking components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in die form.

Lead-free and RoHS compliant

40Gb/s NRZ 2^31-1 PRBS *Single Stage*



**** Input 40Gb/s data stream generated using an Anritsu MUX. Vin=1.8Vpp.***

Datasheet subject to change without notice

MAXIMUM RATINGS 7/

SYMBOL	PARAMETER 6/	VALUE	NOTES
	POSITIVE SUPPLY VOLTAGE		
V^+	Biased thru On-chip Drain Termination	10 V	1/
Vd(fet)	Biased thru the RF Output Port using a Bias Tee	8 V	
	POSITIVE SUPPLY CURRENT		1/
I^+	Biased thru On-chip Drain Termination	125 mA	
Id	Biased thru the RF Output Port using a Bias Tee	125 mA	
P_D	POWER DISSIPATION	1.5 W	2/
	NEGATIVE GATE		
Vg	Voltage	+1V to -3V	
Ig	Gate Current	5 mA	
	CONTROL GATE		
Vctl	Voltage	Vd/2 to -3V	3/
Ictl	Gate Current	5 mA	
	RF INPUT		
P_{IN}	Sinusoidal Continuous Wave Power	18 dBm	
Vin	43Gb/s PRBS Input Voltage Peak to Peak	4 Vpp	
T_{CH}	OPERATING CHANNEL TEMPERATURE	200 °C	4/ 5/
	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T_{STG}	STORAGE TEMPERATURE	-65 to 150 °C	

Notes:

1/ Assure Vd - Vctl <6V. Compute Vd as follows, Vd=V+ - Id*25.
2/ Assure the combination of Vd and Id does not exceed maximum power dissipation rating.
3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is 1.4E4 hours
4/ Assure Vctl never exceeds Vd during bias up and down sequences. Also, assure Vctl never exceeds 4V during normal operation.
5/ These ratings apply to each individual FET.
6/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
7/ These ratings represent the maximum operable values for the device.

RF SPECIFICATIONS
(T_A = 25°C ± 5°C)

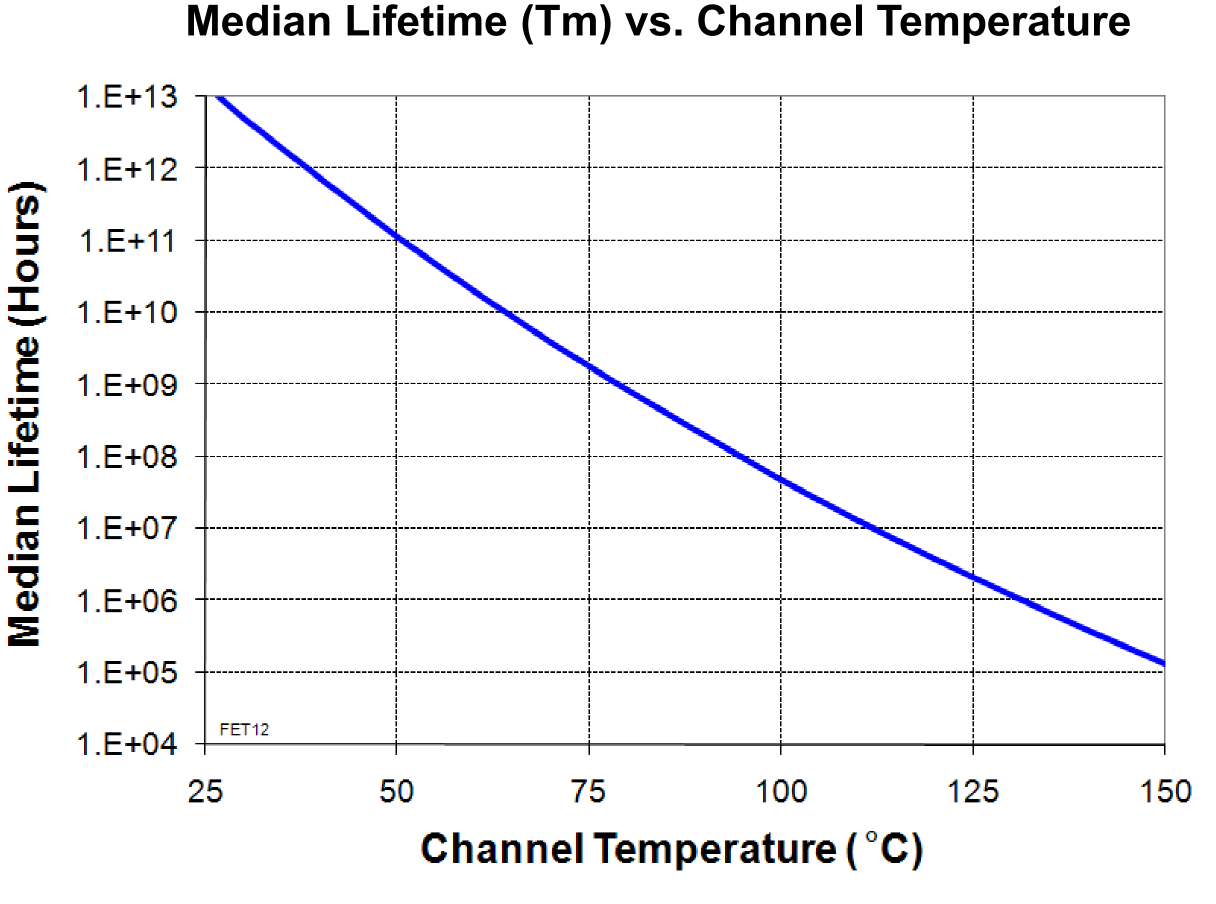
NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			>50		GHz
1/	SMALL-SIGNAL GAIN MAGNITUDE	2.5GHz		8		dB
	AGC RANGE	Midband		3		dB
	NOISE FIGURE	14 GHz		6		dB
	SATURATED OUTPUT VOLTAGE (EYE AMPLITUDE)	43Gb/s with Vin=2Vpp		3.5		V
1/	P1dB	DC-20GHz		TBD		dBm
1/	INPUT RETURN LOSS MAGNITUDE	DC-50GHz		-10		dB
1/	OUTPUT RETURN LOSS MAGNITUDE	DC-50GHz		-10		dB
	GROUP DELAY	DC-50GHz		+/- 20		ps
	RISE TIME	20/80%		10		ps

Notes:
1/ Verified at RF on-wafer probe.

THERMAL INFORMATION

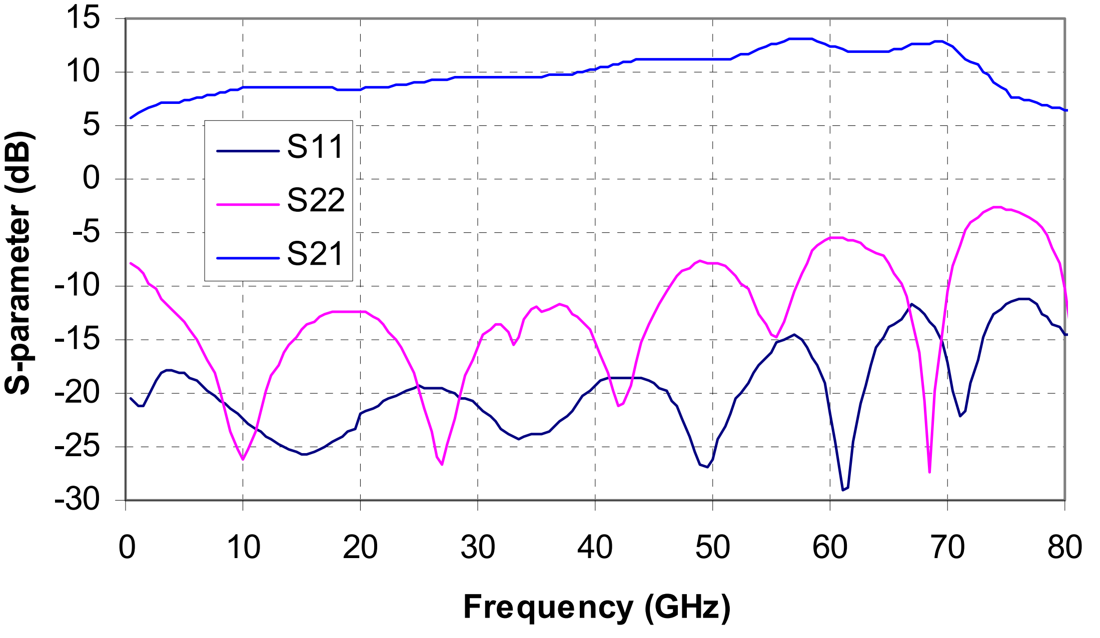
Parameter	Test Condition	T_{CH} (°C)	θ_{JC} (°C/W)	Tm (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vd = 6V, V_{ctrl} = 3 V, I_D = 100mA	109	65	2.3E6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

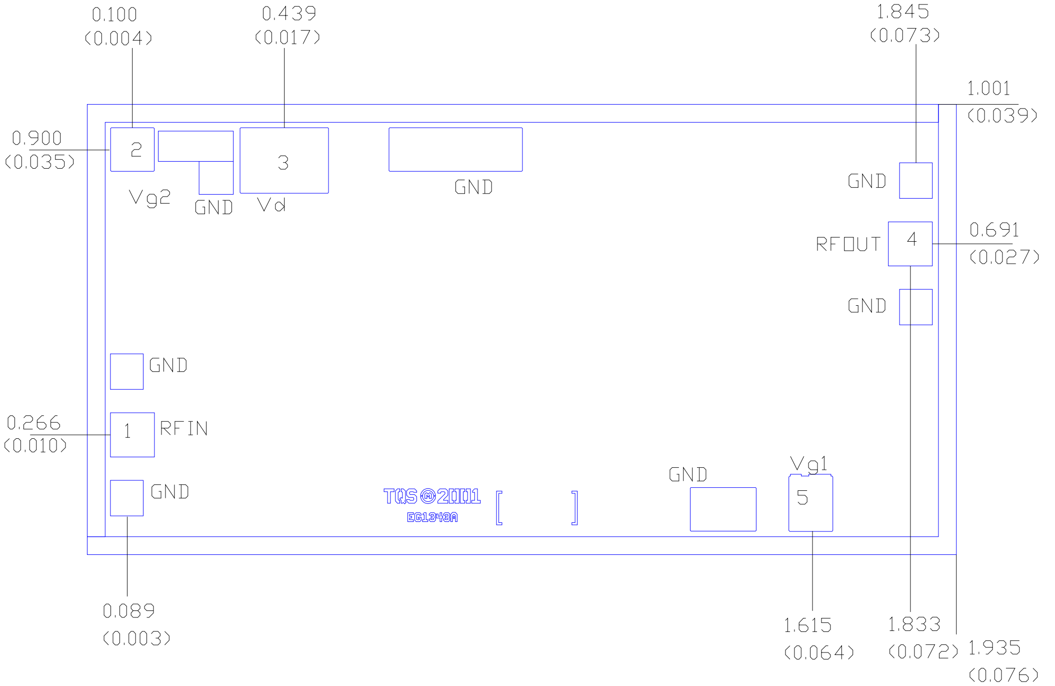


Measured Performance

Bias Conditions: Vd = 10 V, Idq = 82 mA, Vg2=3-3.2V
@ Room Temperature

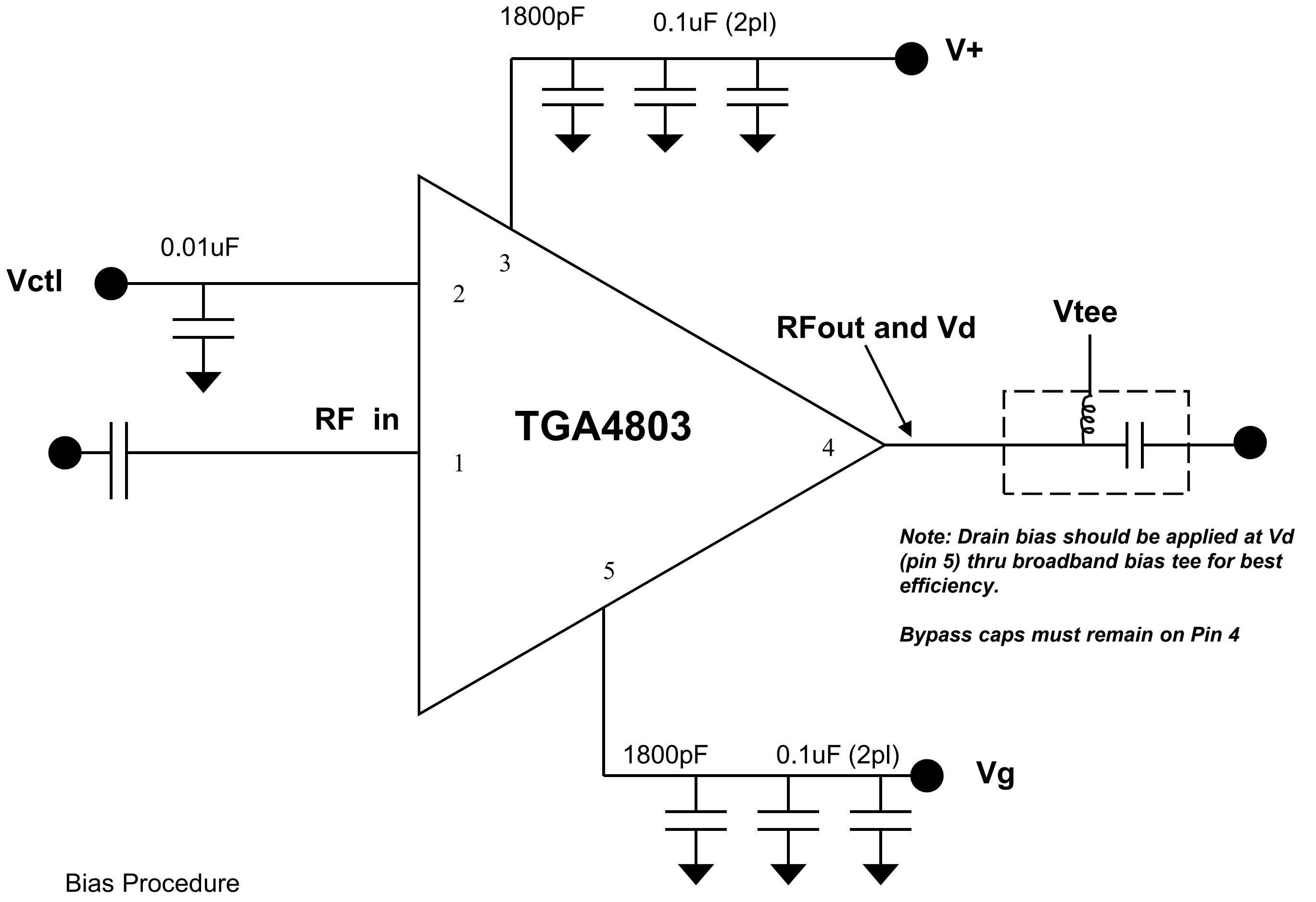


Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/-0.051 (0.002)
GND is back of MMIC

Bond pad #1	RFIN	0.098x0.098	(0.004x0.004)
Bond pad #2	Vg2	0.097x0.097	(0.004x0.004)
Bond pad #4	RFOUT	0.098x0.098	(0.004x0.004)
Bond pad #3	Vd	0.197x0.145	(0.008x0.006)
Bond pad #5	Vg1	0.098x0.123	(0.004x0.005)

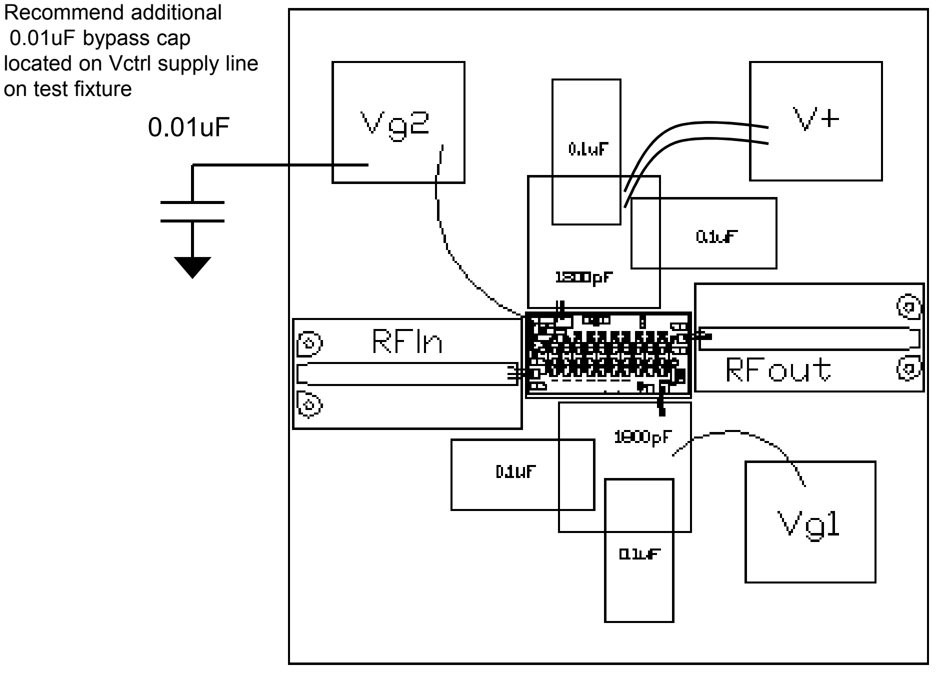


Bias Procedure

A. For applying drain bias thru Vd
   1. Make sure no RF power is applied to the device before continuing.
   2. Set Vg=0 Set Vctl=0.
   3. Raise Vd to 6V while monitoring drain current. Id should be near 20mA.
   4. Raise Vctl to +2.5V (no greater than 3.5V).
   5. Adjust Vg more positive until drain current reaches 100mA.
   6. Apply Vin=1.8V(amplitude) NRZ 40Gb/s

B. For applying drain bias thru V+
   1. Make sure no RF power is applied to the device before continuing.
   2. Set Vg=0 Set Vctl=0.
   3. Raise V+ to 5V while monitoring drain current. I+ should be near 20mA.
   4. Raise Vctl to 2.5V (no greater than 3.5V)
   5. Raise Vg more positive until drain current is 80mA
   6. Raise V+ to 8V
   7. Adjust Vg for Id=100mA
   8. Apply Vin=1.8V(amplitude) NRZ 40Gb/s

CAUTION:
1. Assure Vd - Vctl < 6V. When biasing thru V+, compute Vd as follows, Vd=V+ - Id*30.
2. Assure Vctl never exceeds Vd during bias up and down sequences. Also, assure Vctl never exceeds 4V during normal operation.



Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200°C

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300^{0}C (30 seconds max).
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- No fluxes should be utilized.
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- Devices must be stored in a dry nitrogen atmosphere.

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