PRELIMINARY | Data Sheet | June 24, 2004 | FN7425

xDSL Differential Line Driver

The EL1517 is a dual operational amplifier designed for VDSL and ADSL line driving in DMT based solutions. This device features a high drive capability of 250mA while consuming only 7mA of supply current per amplifier and operating from a single 5V to 12V supply. This driver achieves a typical distortion of -80dBc, at 150kHz into a 25Ω load. The EL1517 is available in the industry standard 8-pin SO as well as the thermally-enhanced 16-pin QFN package. Both are specified for operation over the full -40°C to +85°C temperature range. The 16-pin QFN package option (EL1517IL) has control pins C_0 and C_1 for controlling the bias and enable/disable of the outputs. These controls allow for lowering the power to fit the performance/power ratio for the application.

The EL1517 is ideal for ADSL, SDSL, HDSL2 and VDSL line driving applications.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL1517IS	8-Pin SO	-	MDP0027
EL1517IS-T7	8-Pin SO	7”	MDP0027
EL1517IS-T13	8-Pin SO	13”	MDP0027
EL1517IL	16-Pin QFN	-	MDP0046
EL1517IL-T7	16-Pin QFN	7”	MDP0046
EL1517IL-T13	16-Pin QFN	13”	MDP0046

Features

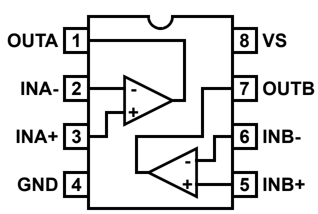
- Drives up to 250mA from a +12V supply
- 18V_{P-P} differential output drive into 50Ω
- 20V_{P-P} differential output drive into 100Ω
- -80dBc typical driver output distortion at full output at 150kHz
- -75dBc typical driver output distortion at 3.75MHz
- -60dBc typical driver output distortion at 8MHz
- -50dBc typical driver output distortion at 16MHz
- Low quiescent current of 7mA per amplifier
- 200MHz bandwidth

Applications

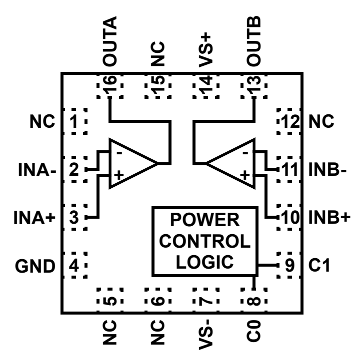
- VDSL line drivers
- ADSL full rate CPE line driving
- G.SHDSL, HDSL2 line drivers
- HomePlug networking drivers

Pinouts

EL1517
(8-PIN SO)
TOP VIEW



EL1517
(16-PIN QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_S+ Voltage to Ground . . . . -0.3V to +13.2V
V_{IN}+ Voltage . . . . GND to V_S+
Current into any Input 8mA
Continuous Output Current 75mA
Ambient Operating Temperature Range . . . . -40°C to +85°C
Storage Temperature Range . . . . -60°C to +150°C
Operating Junction Temperature . . . . +150°C
Power Dissipation . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 12V, R_F = 750Ω, R_L = 100Ω connected to mid supply, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	R_F = 453Ω, A_V = +2		200		MHz
		A_V = +4		150		MHz
HD	Total Harmonic Distortion, Differential	f = 200kHz, V_O = 16V_{P-P}, R_L = 50Ω	-72	-83		dBc
		f = 4MHz, V_O = 2V_{P-P}, R_L = 100Ω		-70		dBc
		f = 8MHz, V_O = 2V_{P-P}, R_L = 100Ω		-60		dBc
		f = 16MHz, V_O = 2V_{P-P}, R_L = 100Ω		-50		dBc
SR	Slew Rate, Single-ended	V_{OUT} from -3V to +3V	600	800	1100	V/µs
DC PERFORMANCE						
V_{OS}	Offset Voltage		-25		+25	mV
ΔV_{OS}	V_{OS} Mismatch		-3		+3	mV
R_{OL}	Transimpedance	V_{OUT} from -4.5V to +4.5V	0.7	1.4	2.5	MΩ
INPUT CHARACTERISTICS						
I_B+	Non-Inverting Input Bias Current		-5		5	µA
I_B-	Inverting Input Bias Current		-20	5	+20	µA
ΔI_B-	I_B- Mismatch		-18	0	+18	µA
e_N	Input Noise Voltage			6		nV/√Hz
i_N	-Input Noise Current			13		pA/√Hz
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing (single ended)	V_S = ±6V, R_L = 100Ω to GND	±4.8	±5		V
		V_S = ±6V, R_L = 25Ω to GND		±4.7		V
I_{OUT}	Output Current	R_L = 0Ω		450		mA
SUPPLY						
V_S	Supply Voltage	Single supply	4.5		13	V
I_S (EL1517IS only)	Supply Current, Maximum Setting	All outputs at mid supply	11	14.3	18	mA
SUPPLY (EL1517IL ONLY)						
I_S+ (full power)	Positive Supply Current per Amplifier	All outputs at 0V, $C_0 = C_1$ = 0V	11	14.3	18	mA
I_S+ (medium power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V	7	8.9	11	mA
I_S+ (low power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V	3.7	4.5	5.5	mA
I_S+ (power down)	Positive Supply Current per Amplifier	All outputs at 0V, $C_0 = C_1$ = 5V		0.1	0.5	mA
I_{INH}, C_0 or C_1	C_0, C_1 Input Current, High	C_0, C_1 = 5V	90	125	160	µA
I_{INL}, C_0 or C_1	C_0, C_1 Input Current, Low	C_0, C_1 = 0V	-5		+5	µA

Typical Performance Curves

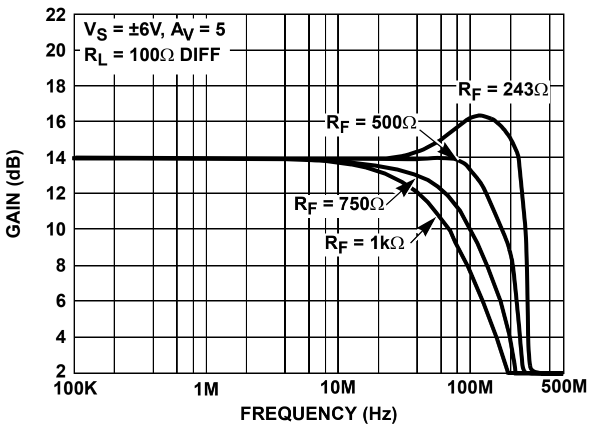


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (FULL POWER MODE)

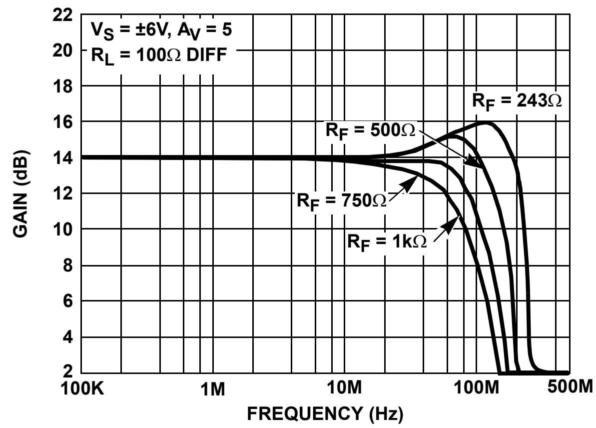


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (MEDIUM POWER MODE)

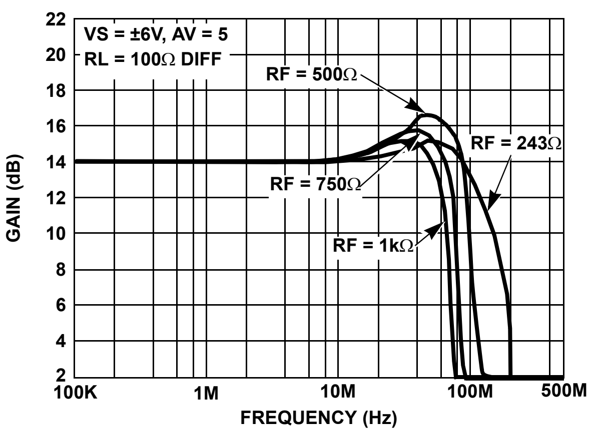


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (LOW POWER MODE)

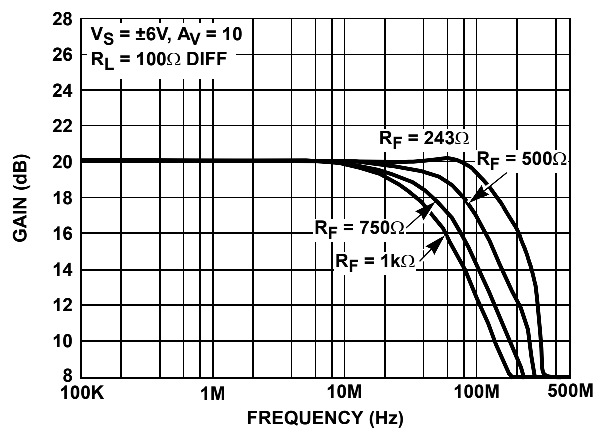


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (FULL POWER MODE)

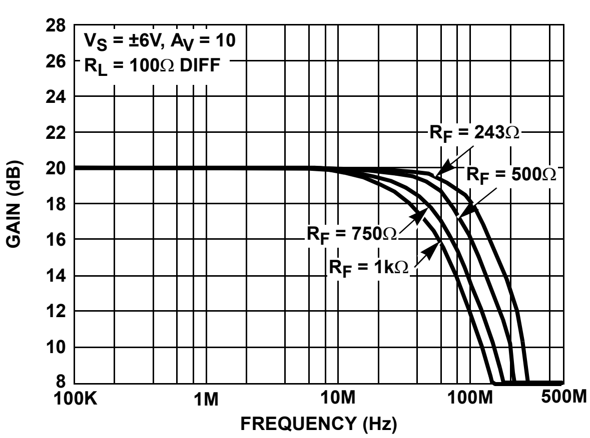


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (MEDIUM POWER MODE)

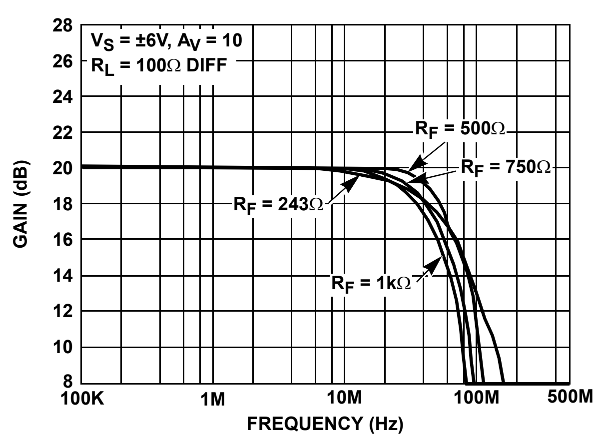


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (LOW POWER MODE)

Typical Performance Curves (Continued)

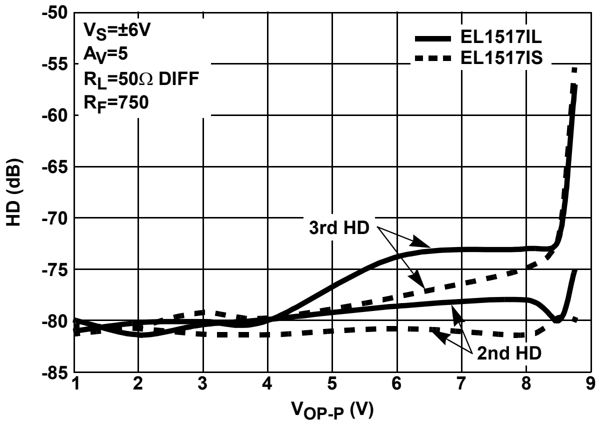


FIGURE 7. DISTORTION BETWEEN EL1517IL vs EL1517IS AT 2MHz

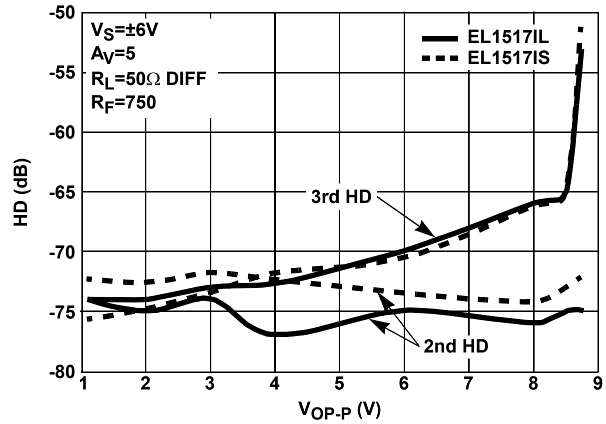


FIGURE 8. DISTORTION BETWEEN EL1517IL vs EL1517IS AT 3MHz

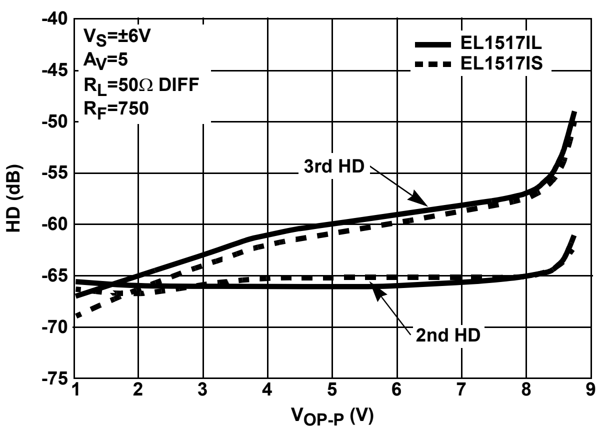


FIGURE 9. DISTORTION BETWEEN EL1517IL vs EL1517IS AT 5MHz

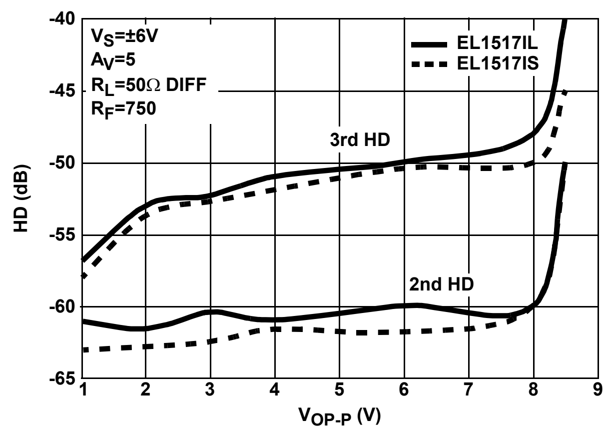


FIGURE 10. DISTORTION BETWEEN EL1517IL vs EL1517IS AT 10MHz

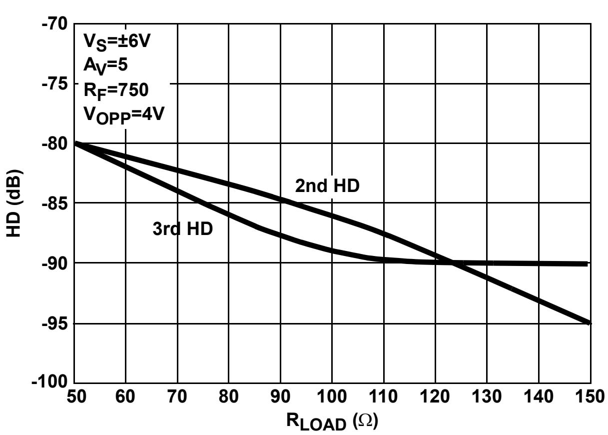


FIGURE 11. 2nd AND 3rd HARMONIC DISTORTION vs R_{LOAD} @ 2MHz (EL1517IL)

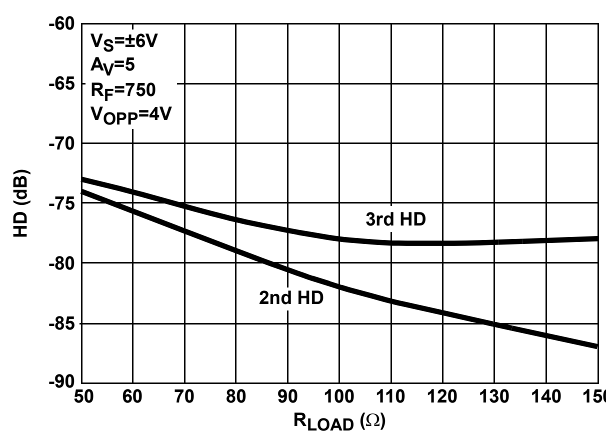


FIGURE 12. 2nd AND 3rd HARMONIC DISTORTION vs R_{LOAD} @ 3MHz (EL1517IL)

Typical Performance Curves (Continued)

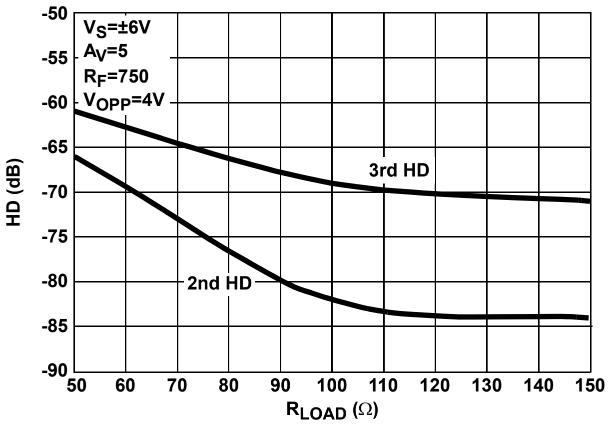


FIGURE 13. 2nd AND 3rd HARMONIC DISTORTION vs R_{LOAD} @ 5MHz (EL1517IL)

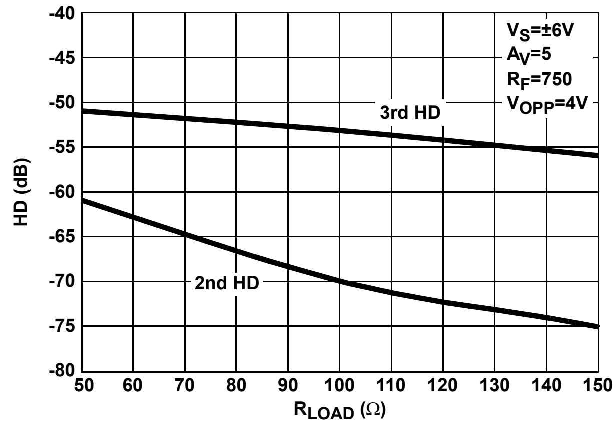


FIGURE 14. 2nd AND 3rd HARMONIC DISTORTION vs R_{LOAD} @ 10MHz (EL1517IL)

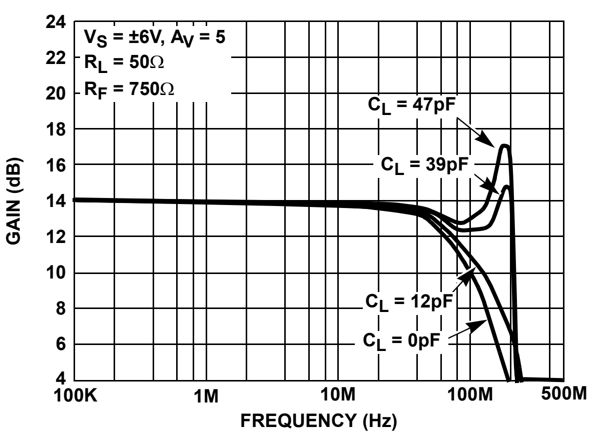


FIGURE 15. FREQUENCY RESPONSE WITH VARIOUS C_L (FULL POWER MODE)

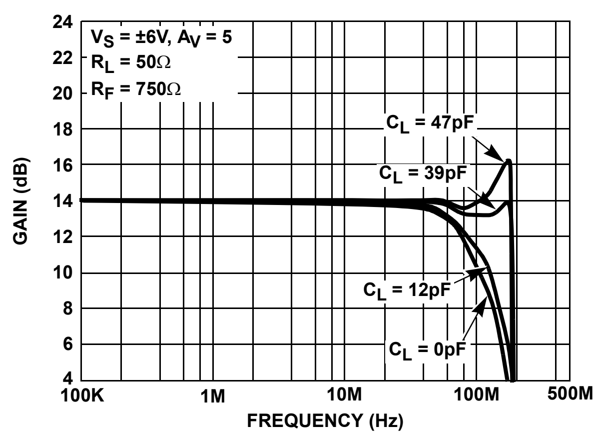


FIGURE 16. FREQUENCY RESPONSE vs VARIOUS C_L (MEDIUM POWER MODE)

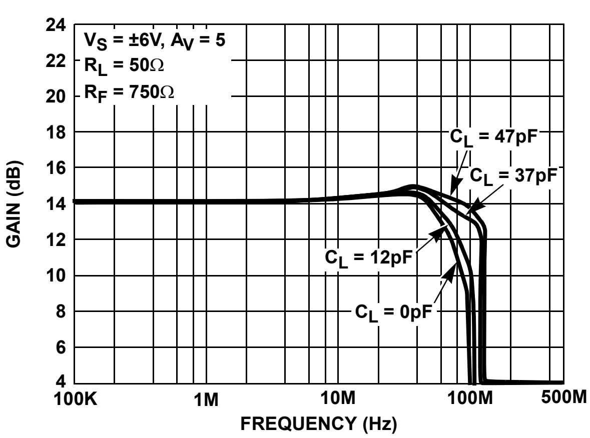


FIGURE 17. FREQUENCY RESPONSE WITH VARIOUS C_L (LOW POWER MODE)

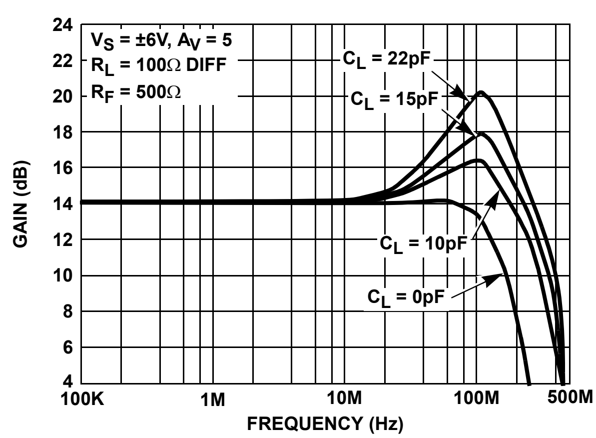


FIGURE 18. FREQUENCY RESPONSE vs C_L AT INVERTING INPUT

Typical Performance Curves (Continued)

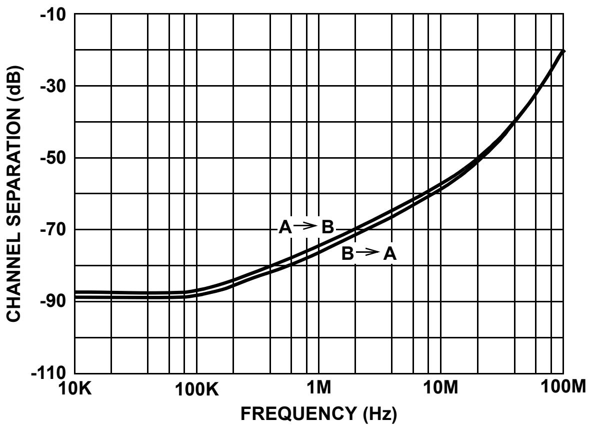


FIGURE 19. CHANNEL SEPARATION vs FREQUENCY

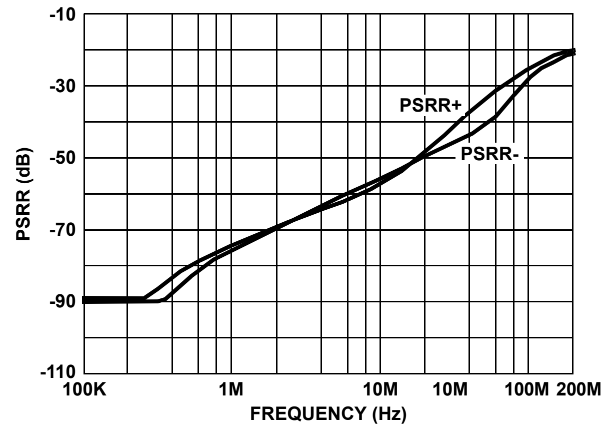


FIGURE 20. PSRR vs FREQUENCY

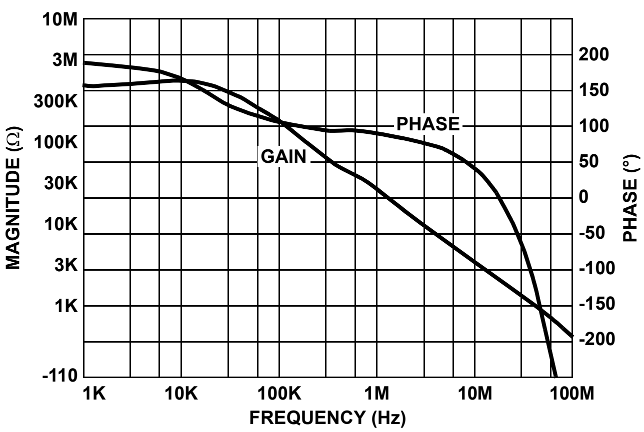


FIGURE 21. TRANSIMPEDANCE (R_{OL}) vs FREQUENCY

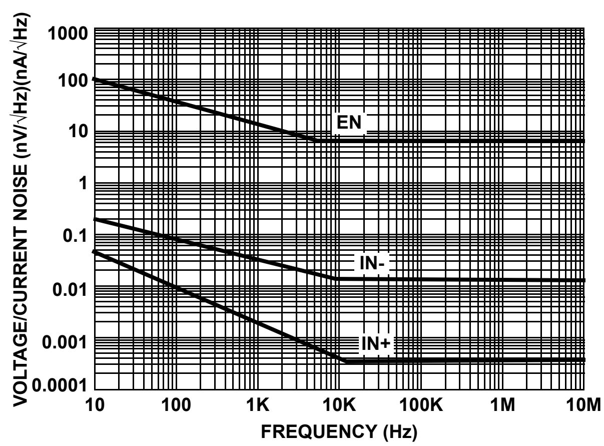


FIGURE 22. VOLTAGE AND CURRENT NOISE vs FREQUENCY

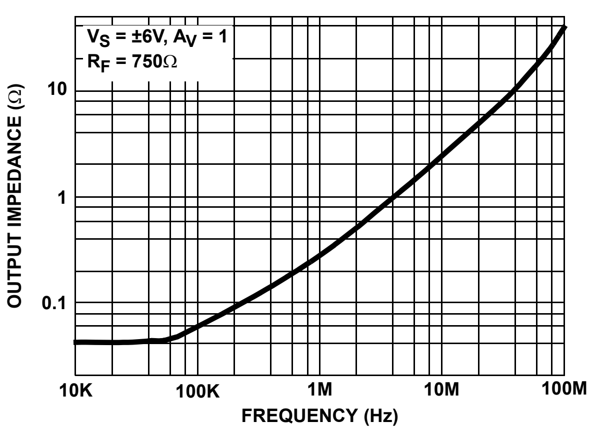


FIGURE 23. OUTPUT IMPEDANCE vs FREQUENCY

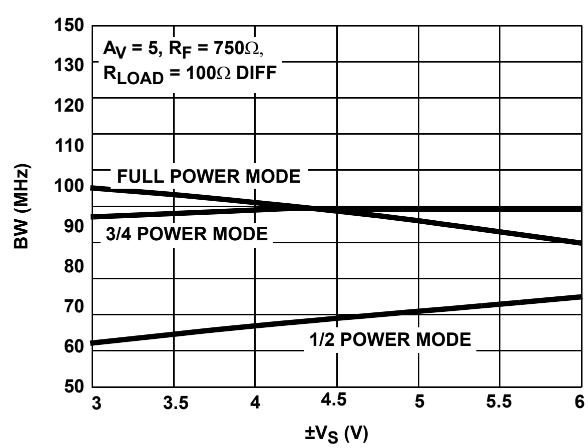


FIGURE 24. DIFFERENTIAL BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

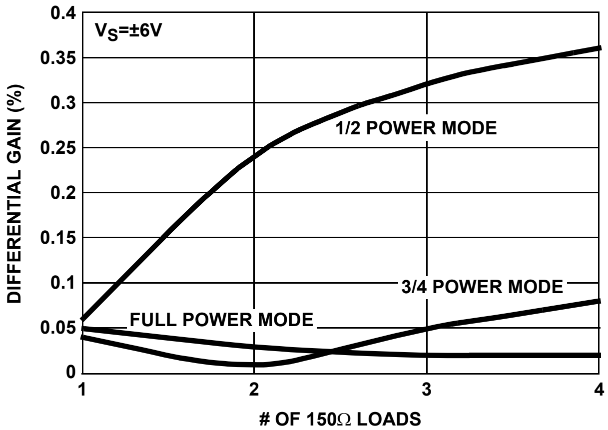


FIGURE 25. DIFFERENTIAL GAIN

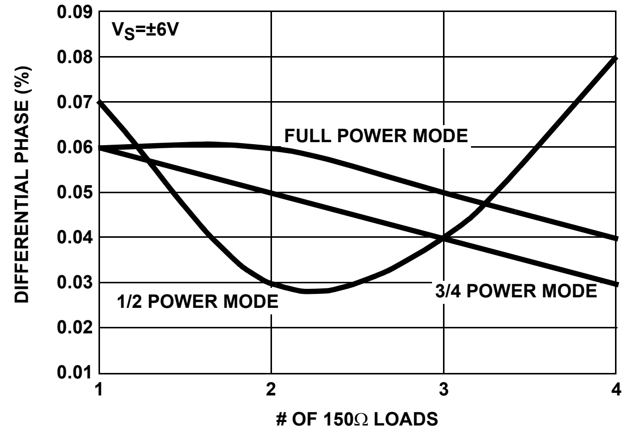


FIGURE 26. DIFFERENTIAL PHASE

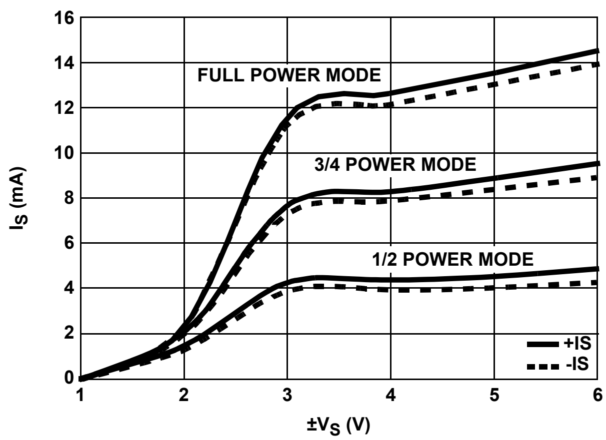


FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE

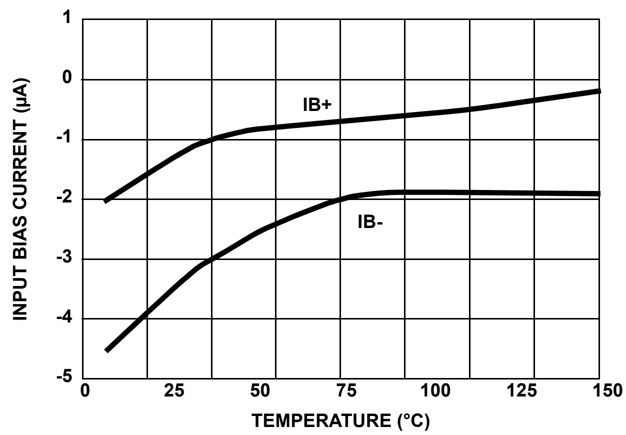


FIGURE 28. INPUT BIAS CURRENT vs TEMPERATURE

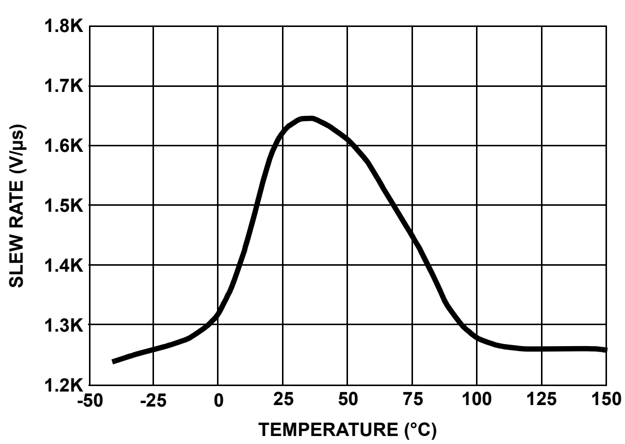


FIGURE 29. SLEW RATE vs TEMPERATURE

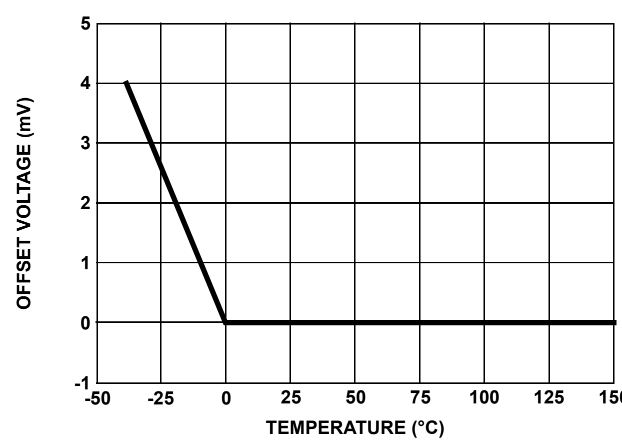


FIGURE 30. OFFSET VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

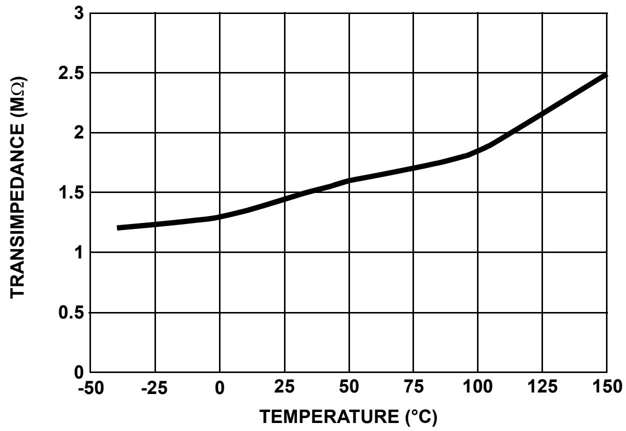


FIGURE 31. TRANSIMPEDANCE vs TEMPERATURE

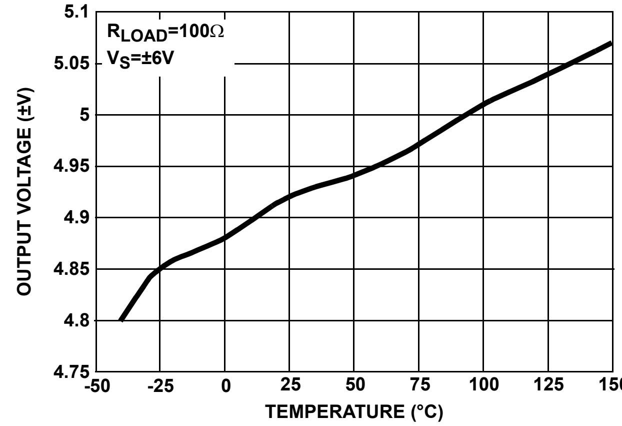


FIGURE 32. OUTPUT VOLTAGE vs TEMPERATURE

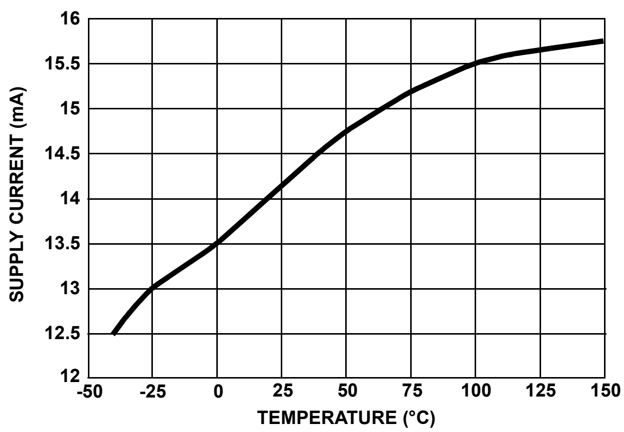


FIGURE 33. SUPPLY CURRENT vs TEMPERATURE

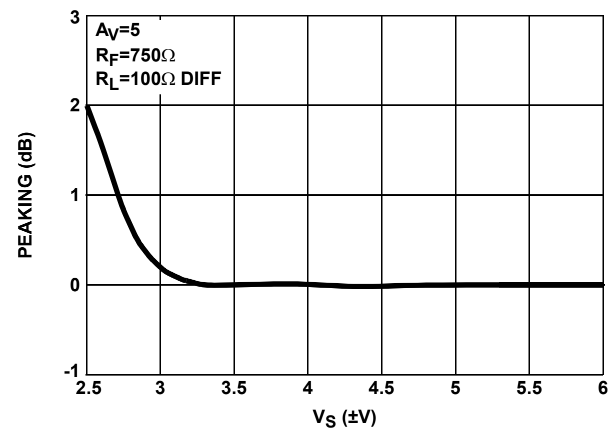


FIGURE 34. DIFFERENTIAL PEAKING vs SUPPLY VOLTAGE

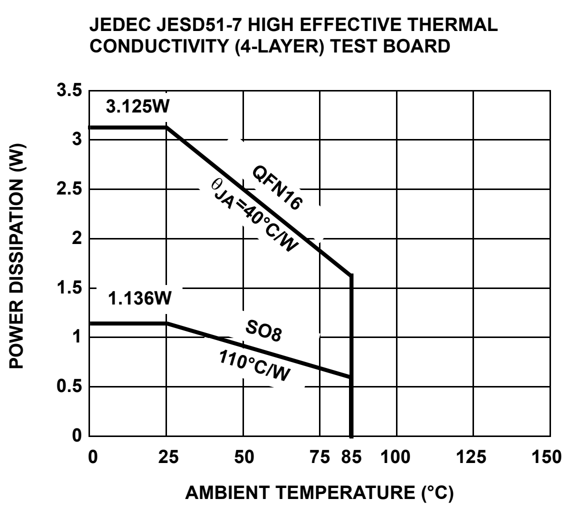


FIGURE 35. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

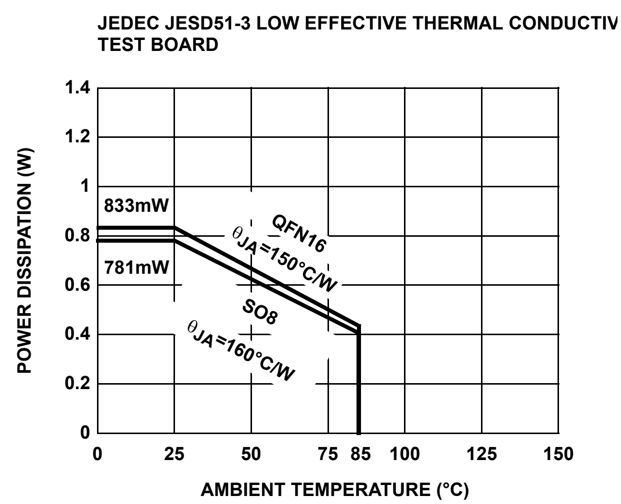


FIGURE 36. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL1517 is a dual operational amplifier designed for line driving in DMT ADSL and VDSL solutions. It is a dual current mode feedback amplifier with low distortion while drawing moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pinouts. Due to the current feedback architecture, the EL1517 closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3dB bandwidth is somewhat dependent on the power supply voltage.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. A 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input. This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL1517 when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL1517 has been designed and specified with $R_F = 750\Omega$ for $A_V = +5$. This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 200MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. See the curves in the Typical Performance Curves section which show 3dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3dB bandwidth drop off at high temperature, the EL1517 was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3dB bandwidth does not drop off drastically with temperature.

Supply Voltage Range

The EL1517 has been designed to operate with supply voltages from ±2.5V to ±6V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2.5V supplies, the 3dB bandwidth at $A_V = +5$ is a respectable 200MHz.

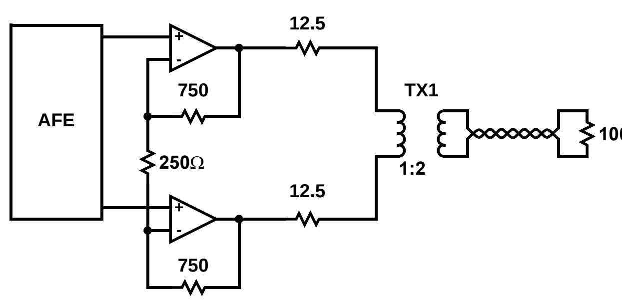
Single Supply Operation

If a single supply is desired, values from +5V to +12V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL1517.

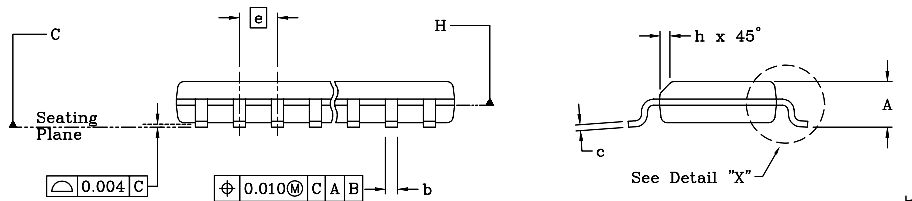
ADSL CPE Applications

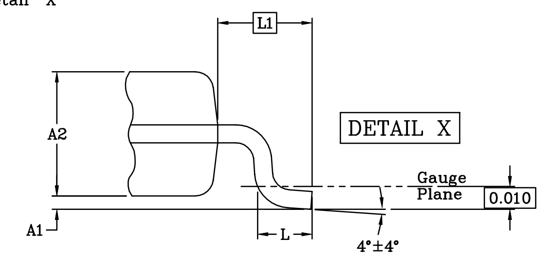
The EL1517 is designed as a line driver for ADSL CPE modems. It is capable of outputting 450mA of output current with a typical supply voltage headroom of 1.3V. It can achieve -85dBc of distortion at low 7.1mA of supply current per amplifier.

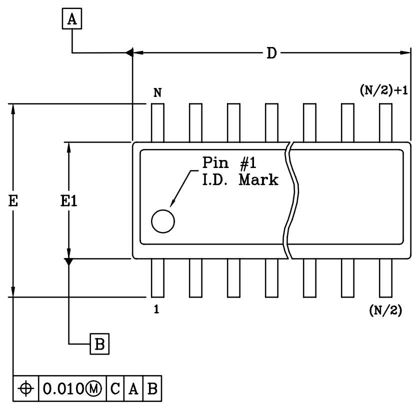
The average line power requirement for the ADSL CPE application is 13dBm (20mW) into a 100Ω line. The average line voltage is $1.41V_{RMS}$. The ADSL DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 7.5V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:2 is selected. The circuit configuration is as shown below.



SO Package Outline Drawing







DIMENSION TABLE

Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027
Rev: L
Date: 2/15/01
Units: Inches
JEDEC Reg: MS-012/013

PACKAGE OUTLINE DRAWING
SMALL OUTLINE (SO) PACKAGE FAMILY

élantec Semiconductor, Inc.
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Notes:

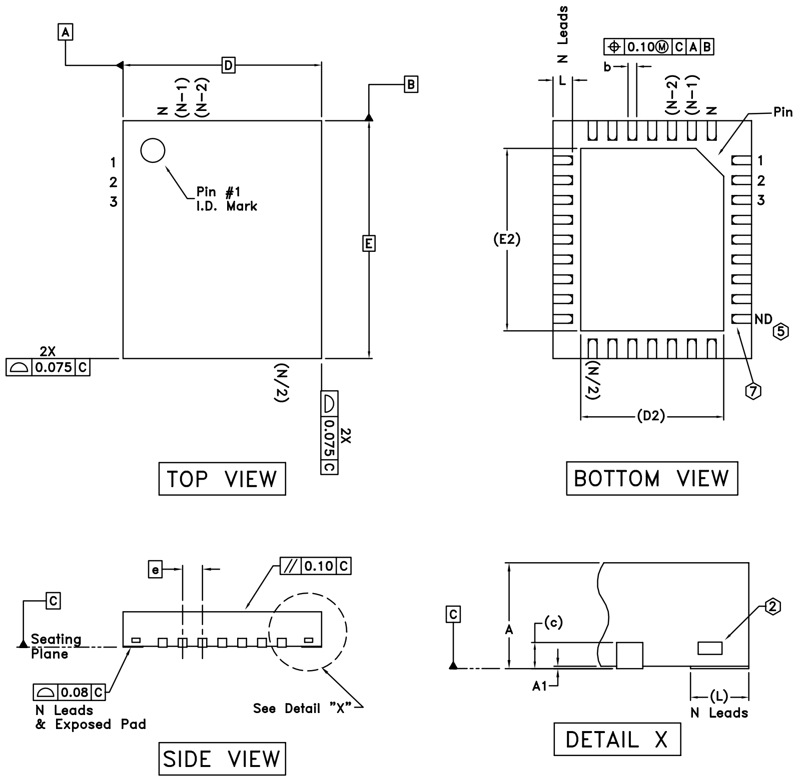
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32	QFN32	Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	7.00	5.00	8.00	5.00	Basic
D2 (8)	5.10	3.80	5.80	3.60/2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 (8)	5.10	5.80	5.80	4.60/3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N (4)	44	38	32	32	Reference
ND (5)	11	7	8	7	Reference
NE (6)	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS					
Symbol	QFN28	QFN24	QFN20	QFN16	Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	4.00	4.00	4.00	4.00	Basic
D2 (8)	2.65	2.80	2.70	2.40	Reference
E	5.00	5.00	4.00	4.00	Basic
E2 (8)	3.65	3.80	2.70	2.40	Reference
L	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.50	0.65	Basic
N (4)	28	24	20	16	Reference
ND (5)	6	5	5	4	Reference
NE (6)	8	7	5	4	Reference

Notes:

1 Dimensioning and tolerancing per ASME Y14.5M–1994.
(2) Tiebar view shown is a non-functional feature.
(3) Bottom–side pin #1 I.D. is a diepad chamfer as shown.
(4) N is the total number of terminals on the device.
(5) ND is the number of terminals on the "D" side of the package (or X–direction).
(6) NE is the number of terminals on the "E" side of the package (or Y–direction). NE = (N/2)–ND.
(7) Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
(8) If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

Drawing #: MDP0046	PACKAGE OUTLINE DRAWING QFN (QUAD FLAT NO–LEAD) PACKAGE FAMILY (Formerly Known as LPP)
Rev: 9	
Date: 5/17/04	
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO–220	

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>