No.3052A

LC9931B

1/3-Inch EIA B&W Imaging Element

Overview

The LC9931B is a 1/3-inch high-resolution frame transfer charge-coupled device (CCD) with an effective image size of 378×486 pixels. The absence of afterimage, burning and graphic distortion, combined with a high sensitivity, built-in amplifier, enhance the image quality of the LC9931B, making it ideal for use as an imaging element in compact black and white video cameras.
The LC9931B is built on a 6.6×7.7mm chip with a 12.7×7.5μm unit cell geometry and is available in 20-pin shrink DICs

Features

- Effective image size : 378×486 pixels
- Total image size : 400×504 pixels
- Optically black pixels — Horizontal : 2 before and 20 after; Vertical : 14 before and 4 after
- High sensitivity with low noise
- Blooming suppression
- No afterimage, burning or graphic distortion
- Small size
- High vibration resistance, high reliability and long life
- 20-pin shrink DIC package

Element Structure

- Image sensor : 1/3-inch high-resolution frame transfer charge-coupled device (CCD)
- Unit cell size : 12.7×7.5μm
- Chip size : 6.6×7.7mm
- CCD structure : Cross-gate
- Horizontal shift register : Includes four preceding dummy bits
- Built-in amplifier : High sensitivity, output amplifier

Case Outline 3130-D20SVL
(unit : mm)

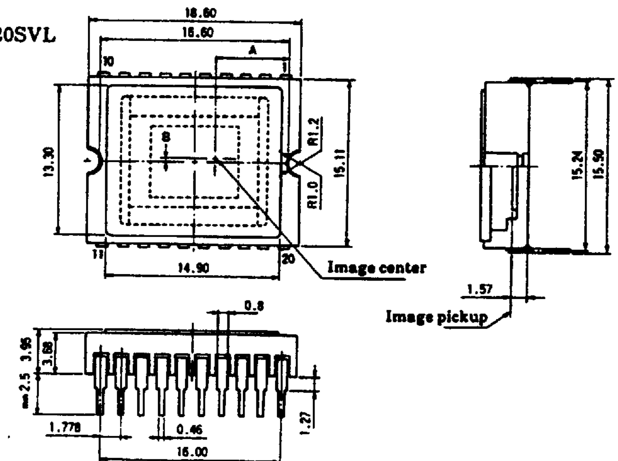

Image center

A	6.89
B	0.05

Specifications and information herein are subject to change without notice.

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Absolute Maximum Ratings at Ta = 25°C

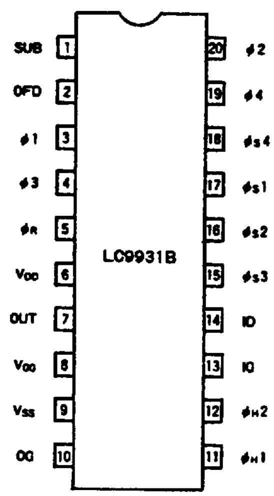
				unit
Maximum Supply Voltage	V_{OFD}, V_{DD}	(V_{SUB} = 0V)	−0.3 to +20	V
	V_{ID}, V_{OG}, V_{GG}	(V_{SUB} = 0V)	−0.3 to +14	V
Horizontal Clock Pin	ϕ_R	(V_{SUB} = 0V)	−0.3 to +18	V
Clock Pins other than above	-	(V_{SUB} = 0V)	−18 to +18	V
Pins other than above	-		−0.3 to +10	V
Storage Temperature	Tstg		−30 to +80	°C
Operating Temperature	Topg		−10 to +55	°C

Electrical Characteristics

DC Characteristics

			min	typ	max	unit
Substrate Voltage	Vsub	Vsub = GND		0		V
Output Circuit Supply Voltage	V_{DD}		17.5	18	18.5	V
	V_{SS}		R_{SS} = 2kΩ resistor			
	V_{GG}		4	5	6	V
Anti-Blooming Bias	V_{OFD}		14.5	15	15.5	V
OG Bias	V_{OG}	Adjustment required	5		12	V
DC Operating Current	I_{DD}		2	3	4	mA
Test Pin Voltage	V_{ID}		8	10	12	V
	V_{IG}	Connected to V_{GG}	4	5	6	V

Pin Assignment



(Top View)

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	SUB	Substrate	11	ϕ_{H1}	Horizontal clock
2	OFD	Overflow drain	12	ϕ_{H2}	Horizontal clock
3	ϕ_1	Image pickup clock	13	IG	Test pin
4	ϕ_3	Image pickup clock	14	ID	Test pin
5	ϕ_R	Reset gate	15	ϕ_{S3}	Image storage clock
6	V_{DD}	Power supply	16	ϕ_{S2}	Image storage clock
7	OUT	CCD output	17	ϕ_{S1}	Image storage clock
8	V_{GG}	Load gate	18	ϕ_{S4}	Image storage clock
9	V_{SS}	Output transistor source	19	ϕ_4	Image pickup clock
10	OG	CCD output gate	20	ϕ_2	Image pickup clock

Equivalent Circuit Block Diagram

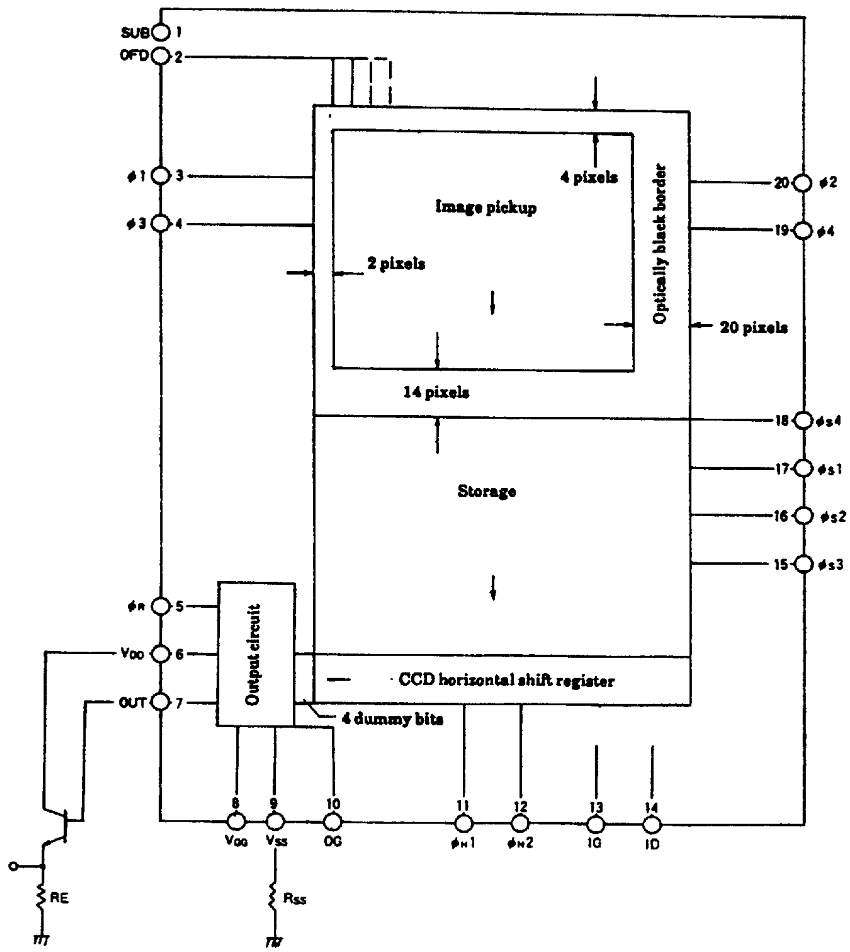


Image Pickup Clock Voltage : ϕ_1, ϕ_3

			min	typ	max	unit
Middle Level	V_{MO}	See note.	5.0	Vp	13.5	V
High Level	V_{HO}		11.5	12.0	12.5	V
Low Level	V_{LO}		−0.5	0	0.5	V

Note : Adjust Vp to obtain the highest possible output without blooming or vertical rolling.

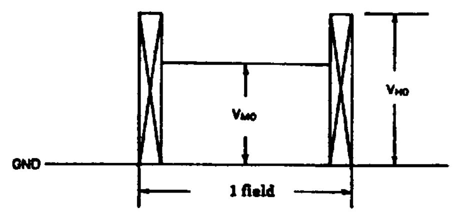


Figure 1 Image Pickup Clock

Image Pickup Clock Voltage : ϕ_2, ϕ_4

		min	typ	max	unit
High Level	V_{HE}	11.5	12.0	12.5	V
Low Level	V_{LE}	−0.5	0	0.5	V

Image Storage Clock Voltage : ϕ_{S1}, ϕ_{S2}, ϕ_{S3}, ϕ_{S4}

		min	typ	max	unit
High Level	V_{HS}	11.5	12.0	12.5	V
Low Level	V_{LS}	0	0	0.5	V

Horizontal Trace Clock Voltage : ϕ_{H1}, ϕ_{H2}

		min	typ	max	unit
High Level	V_{HH}	8.5	9	9.5	V
Low Level	V_{LH}	0	0	0.5	V

Reset Gate Voltage : ϕ_R

		min	typ	max	unit
High Level	V_{HR}	8.5	9	9.5	V
Low Level	V_{LR}	0	0	0.5	V

Gate Input Capacitance

Image	2000pF/pin
Storage	1500pF/pin
Horizontal	100pF/pin
Reset	5pF

Drive Pulse Waveform

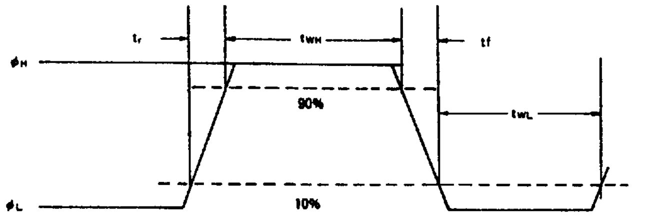


Figure 2 Pulse Waveform

Symbol	t_{WH} typ	t_{WL} typ	t_r typ	t_f typ	unit	Remarks
ϕ_1	110	110	30	30	ns	Frame shift frequency is 3.58 MHz at frame forward
ϕ_2	110	110	30	30		
ϕ_3	110	110	30	30		
ϕ_4	110	110	30	30		
ϕ_{S1}	110	110	30	30	ns	Frame shift frequency is 3.58 MHz at frame forward
ϕ_{S2}	110	110	30	30		
ϕ_{S3}	110	110	30	30		
ϕ_{S4}	110	110	30	30		
ϕ_{S1}	1.1	62.5	30	30	ns	Vertical forward at 1H line, unit for ▩ : μsec
ϕ_{S2}	1.1	62.5	30	30		
ϕ_{S3}	62.5	1.1	30	30		
ϕ_{S4}	62.5	1.1	30	30		
ϕ_R	55	55	15	15	ns	Reset pulse
ϕ_{H1}	55	55	15	15		At Horizontal forward
ϕ_{H2}	55	55	15	15		

Image Characteristics at Ta = 25°C

		Test Condition		min	typ	max	unit
Sensitivity	S	1		50			mV
Video Signal Fluctuation	VF	2				15	%
Saturation Signal	Vsat	3		300			mV
Saturation Signal Fluctuation	VFs	4				20	%
Smear	SM	5	See note.		0.04		%
Dark Signal	Vdrk	6			5	8	mV
γ Characteristic	γ				1		

Note : Frame shift frequency is 3.58MHz.

Verification of Performance

Measurement Setup

- Install the CCD on the Sanyo evaluation board.
- Measure the video level at the evaluation board's video OUT pin terminated with a 75Ω resistor.
- Attach a 1mm thick C-500 infrared filter to the front of a FUJINON HF16A lens. Place the lens 50cm from a Dai Nippon Printing Model CCV31F test pattern generator. Set the generator to a luminance of 1320NT and a color temperature of 3100K.

Measurement Procedure

1. Measure the sensitivity.
   Measure the video output at the center of the CCD with no test pattern on the screen of the test pattern generator and a lens aperture of F11.
2. Calculate the video output at the nine, evenly spaced points shown in Figure 3. Calculate VF using formula (1).

$$VF = \frac{V\,max - V\,min}{(V1 + V2 + V9)/9} \times 100 \cdots (1)$$

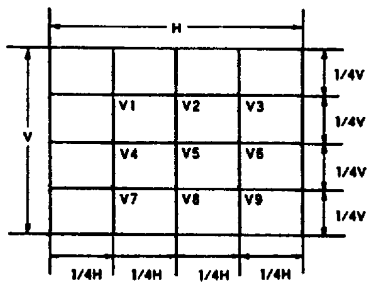


Figure 3 Measuring Points (Full Screen)

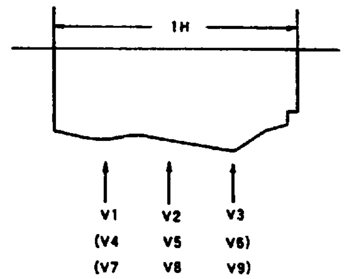
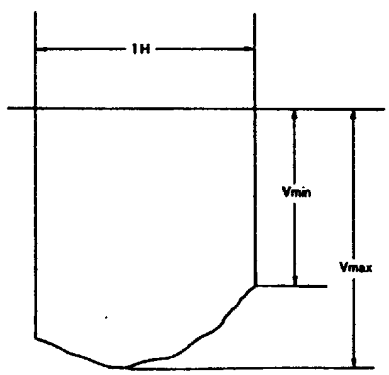


Figure 4 Measuring Points (Single Trace)

3. Measure the saturation signal level.
   Open the lens aperture fully and measure the video output at the center of the CCD.
   Note: If the output level is different for adjacent odd and even lines, use the lower of the two readings.
4. Calculate the saturated video fluctuation, VFs.
   Display the output for a single horizontal trace at the center of the CCD on a synchroscope, determine the maximum and minimum for the trace, and calculate VFs with formula (2).



$$VFs = \frac{V\,max - V\,min}{(V\,max + V\,min)/2} \cdots (2)$$

Figure 5 Saturated Video Fluctuation

5. **Calculate the amount of smear, SM.**
   Adjust the lens aperture to bring Vsig, the output level for the middle 10% of a vertical bar at the center of the test pattern, as close as possible to 250mV. See Figure 6. Calculate Vsm, the average output for the rest of the bar and calculate SM with formula.

$$SM = \frac{Vsm}{Vsig - Vsm} \times 100\ (\%)$$

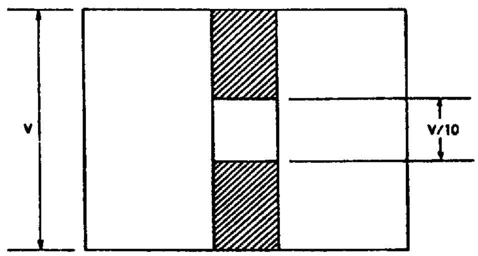


Figure 6 Smear

6. **Measure the dark signal level, Vdrk.**
   Cut off all light to the pickup and measure the difference in signal levels between the image and non-image portions of the trace. See Figure 7. Ignore the optical black portions of the signal.

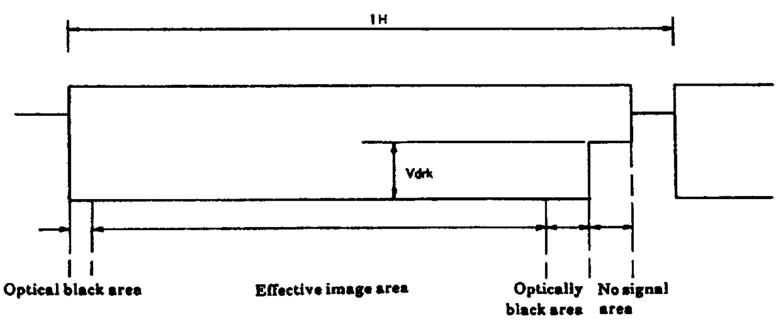


Figure 7 Single Horizontal Trace

B&W Video Camera Application

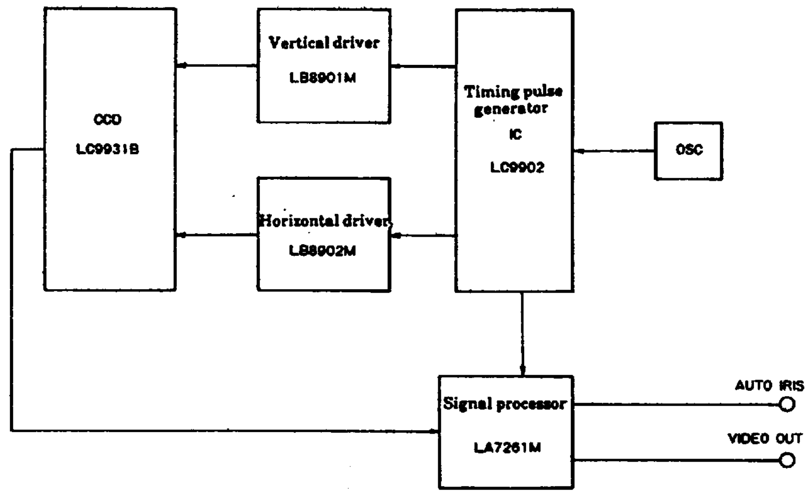


Figure 8 B&W Video Camera

Block Description

OSC :

The 14.318MHz clock signal determines the synchronization and other timing signals.

Timing pulse generator :

The LC9902 IC generates video horizontal and vertical drive, synchronization signals, and timing pulses for driving the CCD.

Vertical and horizontal drivers :

The LB8901M and LB8902M ICs amplify the pulses from the timing pulse generator to CCD drive levels.

Signal processor :

The LA7261M IC supports clamping, automatic gain control (AGC), γ correction, white peak clipping and the addition of pedestal pulses.

Care and Handling

1) Avoid static electricity as static discharges can severely damage device circuitry, rendering it inoperative. Always ground tools before touching the device. Personal should also be grounded through a 1MΩ resistor.
2) Use a 30W soldering iron instead of a mounting furnace as excessive heat can damage the protective glass seal and the glass filter over the CCD.
3) Never touch the glass plate over the CCD. If the plate is dirty, wipe it with a lens cleaning tissue and some ethyl alcohol.
4) Always store the chip in its protective case to prevent dust and foreign matter from accumulating on the surface of the glass plate.

Detect Standards

Temperature	Defect	Zone/Maximum
45°C	White defect See note 1.	I/2 II/5 III/5
25°C	Black defect See note 2.	I/2 II/3 III/3

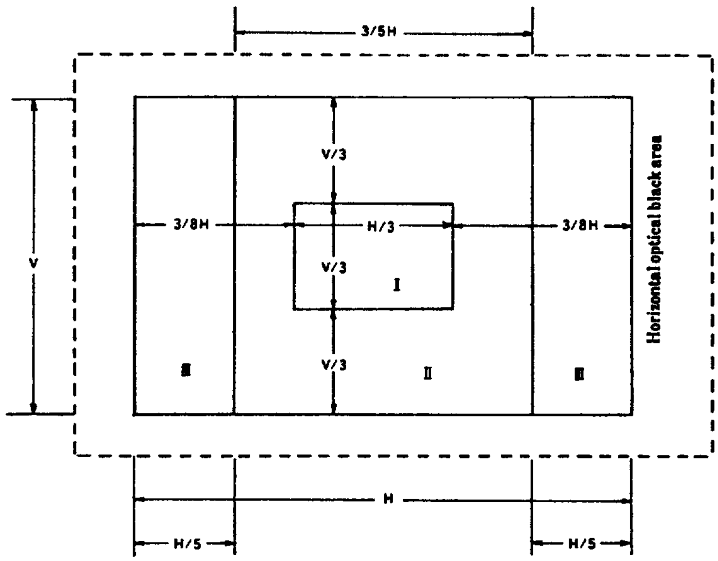


Figure 9 CCD Zones for Defect Counting

Notes :

1. A white defect is any pixel with an output level, when there is no light falling on the CCD, at least 20mV above that of an optically black pixel. The ROMs must be replaced if the number of defects for the zone exceeds the limit given in the table above.
2. A black defect is any pixel with an output level at least 35mV but less than 60mV below the saturated output level of a pixel when there is a pure white test pattern falling on the CCD. The number of defects in each zone must not exceed the limit given in the table above. There must be no pixel with an output level 60mV or more below the saturated output level.
3. There must be no horizontally adjacent white or black defects.
4. There must be no more than four vertically adjacent white or black defects.
5. When there is no light falling on the CCD, there must be no line of adjacent pixels with an output level at least 10mV above that of an optical black pixel.
6. When a pure white test pattern is generating saturated CCD output, there must be no line of adjacent pixels with an output level of more than 10mV below the saturated output level.