

256Kx32 Static RAM CMOS, High Speed Module

ADVANCE INFORMATION

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Features

The EDI8M32256C is a high speed 8 megabit Static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256Kx4 Static RAMs in LCC packages on a multi-layered ceramic substrate.

Four chip selects ($\overline{E1}$ - $\overline{E4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8M32256C is offered in a 60 pin DIP package which enables 8 megabits of memory to be placed in less than 1.8 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

Military product, incorporating semiconductor components which are compliant to MIL-STD-883, paragraph 1.2.1, is available.

256Kx32 bit CMOS Static
Random Access Memory

- Access Times 35, 45, and 55ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package

- 60 Pin DIP, No. 86
- Common Data Inputs and Outputs

Single +5V ($\pm 10\%$) Supply Operation

Pin Names

A0-A17	Address Inputs
E1-E4	Chip Enable
$\overline{W0}$ - $\overline{W1}$	Write Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground

Pin Configuration and Block Diagram

VCC	1	□	60	VSS
A0	2	□	59	DQ31
DQ0	3	□	58	DQ30
DQ1	4	□	57	DQ29
DQ2	5	□	56	DQ28
DQ3	6	□	55	A17
$\overline{E0}$	7	□	54	A16
A1	8	□	53	$\overline{E3}$
DQ4	9	□	52	DQ27
DQ5	10	□	51	DQ26
DQ6	11	□	50	DQ25
DQ7	12	□	49	DQ24
A2	13	□	48	A15
A3	14	□	47	A14
$\overline{W0}$	15	□	46	$\overline{W1}$
A4	16	□	45	A13
A5	17	□	44	A12
DQ8	18	□	43	DQ23
DQ9	19	□	42	DQ22
DQ10	20	□	41	DQ21
DQ11	21	□	40	DQ20
A6	22	□	39	A11
A7	23	□	38	A10
$\overline{E1}$	24	□	37	$\overline{E2}$
DQ12	25	□	36	DQ19
DQ13	26	□	35	DQ18
DQ14	27	□	34	DQ17
DQ15	28	□	33	DQ16
A8	29	□	32	A9
VSS	30	□	31	VCC

