IS61LV6416

64K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

OCTOBER 2000

FEATURES

- High-speed access time: 8, 10, 12, 15, and 20 ns
- CMOS low power operation
  - — 250 mW (typical) operating
  - — 250 µW (typical) standby
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available

DESCRIPTION

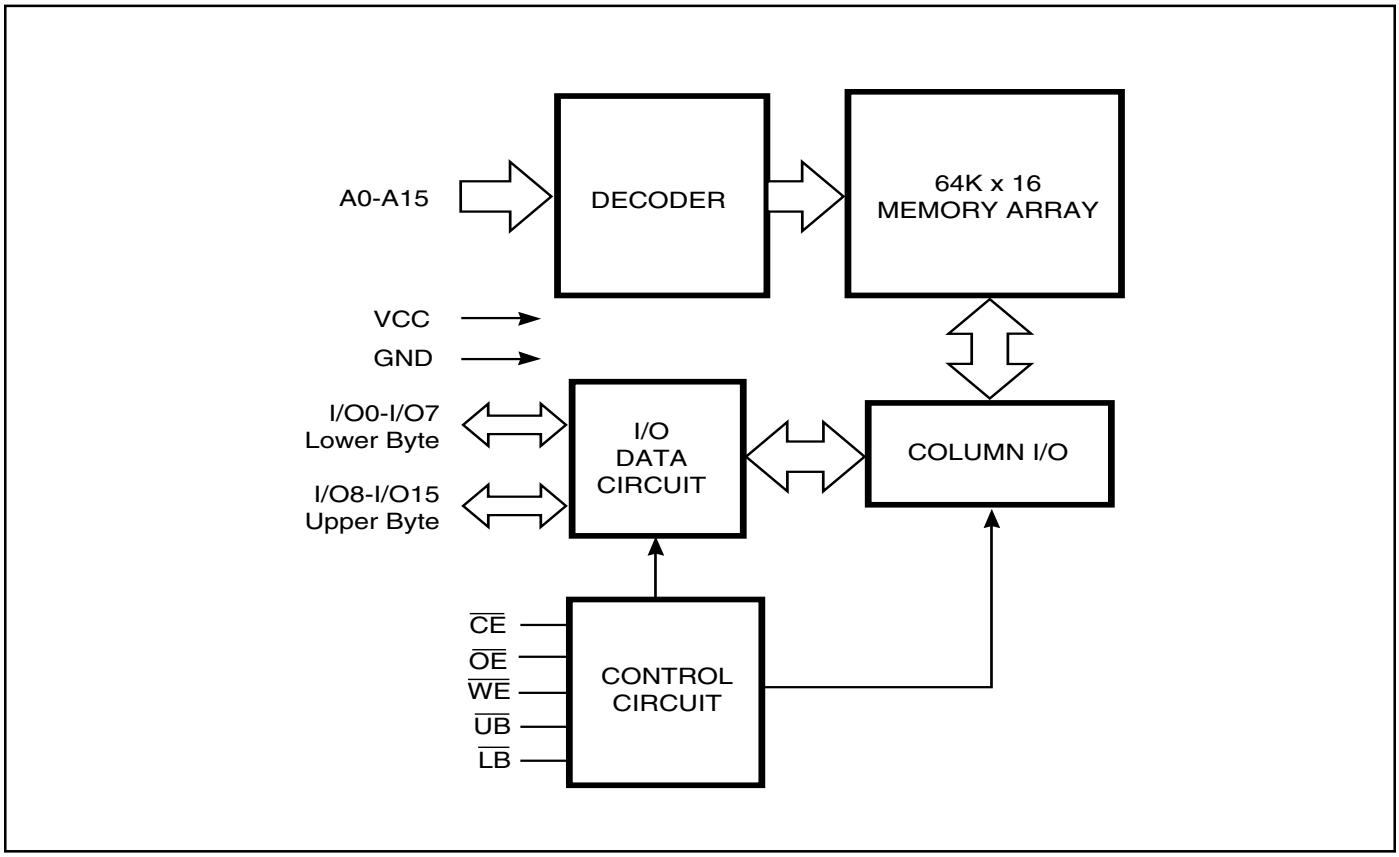
The *ISSI* IS61LV6416 is a high-speed, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

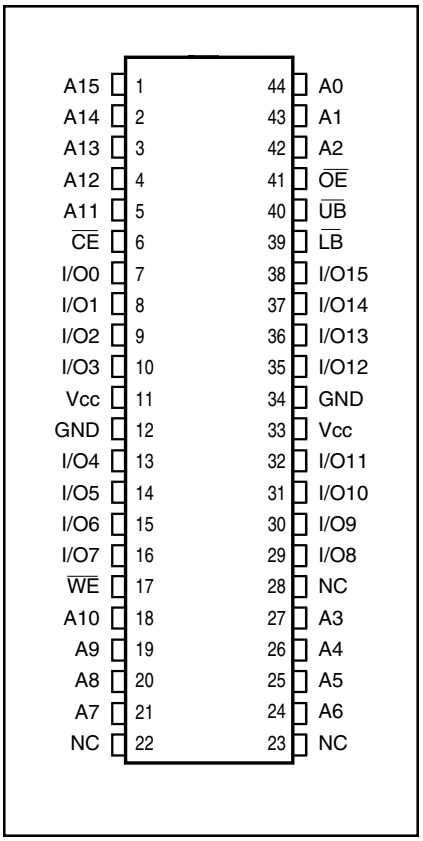
The IS61LV6416 is packaged in the JEDEC standard 44-pin 400-mil SOJ, 44-pin TSOP, and 48-pin mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM

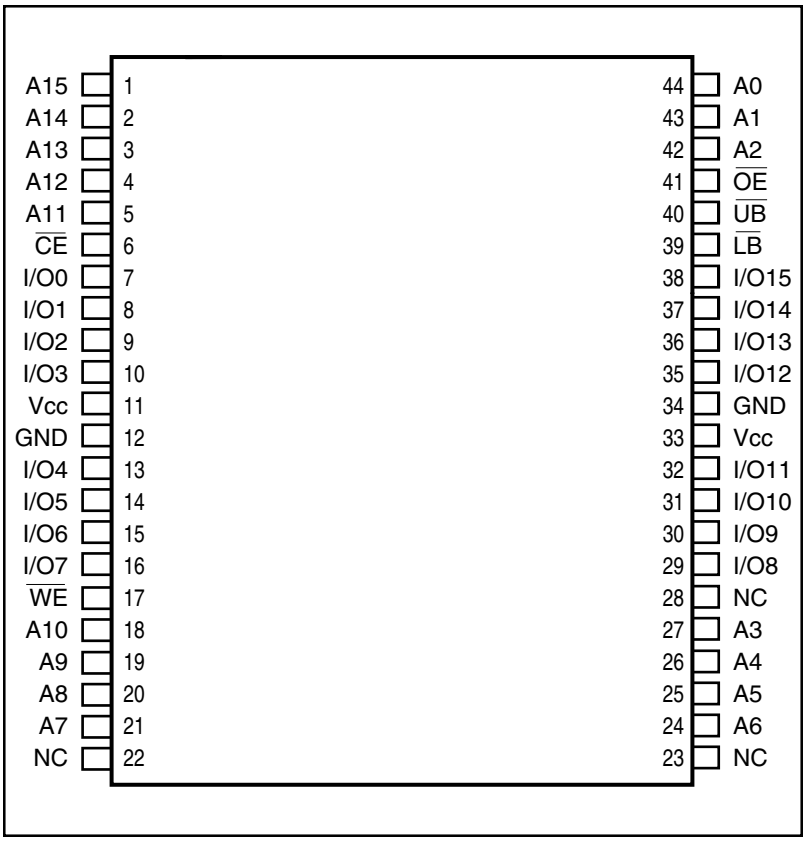


PIN CONFIGURATIONS

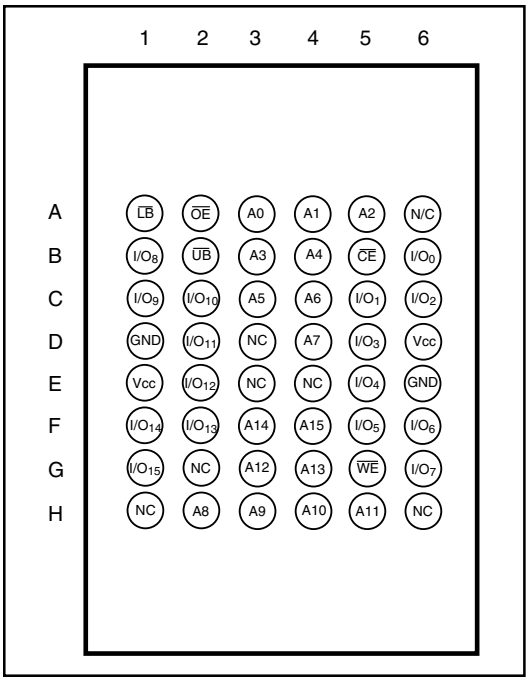
44-Pin SOJ



44-Pin TSOP



48-Pin mini BGA (6mm x 8mm)



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc(8,10ns)	V_{CC} (12,15,20ns)
Commercial	0°C to +70°C	3.3V+10%,-5%	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V+10%,-5%	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–2	2	µA

Notes:
1. V_{IL} (min.) = –2.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	210	—	190	—	150	—	130	—	120	mA
			Ind.	—	215	—	210	—	170	—	150	—	140	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	25	—	25	—	15	—	15	—	15	mA
			Ind.	—	30	—	30	—	25	—	25	—	25	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	10	—	10	—	10	—	10	—	10	mA
			Ind.	—	15	—	15	—	15	—	15	—	15	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	—	15	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	—	6	—	7	—	8	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	5	—	6	0	6	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2	$\overline{CE}$ to High-Z Output	0	4	0	5	0	6	0	6	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	6	—	6	—	6	—	7	—	8	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	4	0	5	0	6	0	6	0	8	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

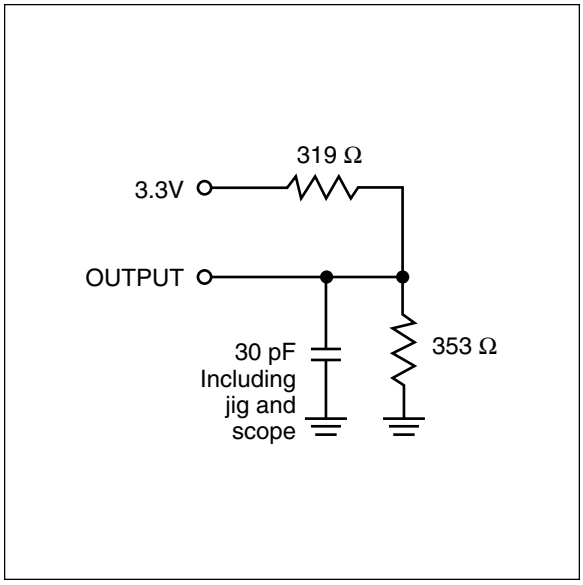


Figure 1a.

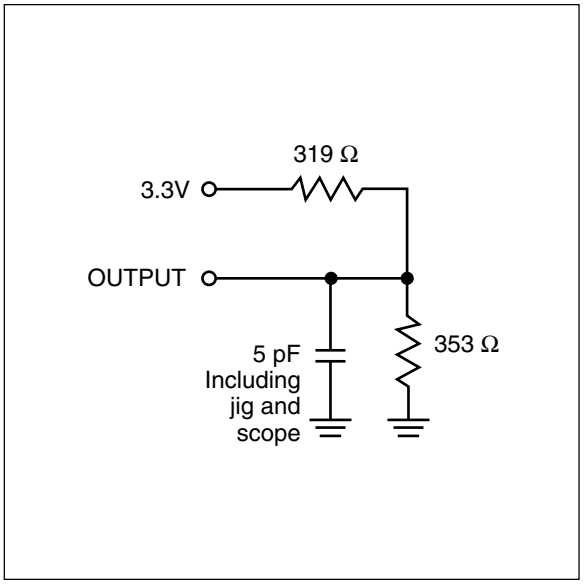
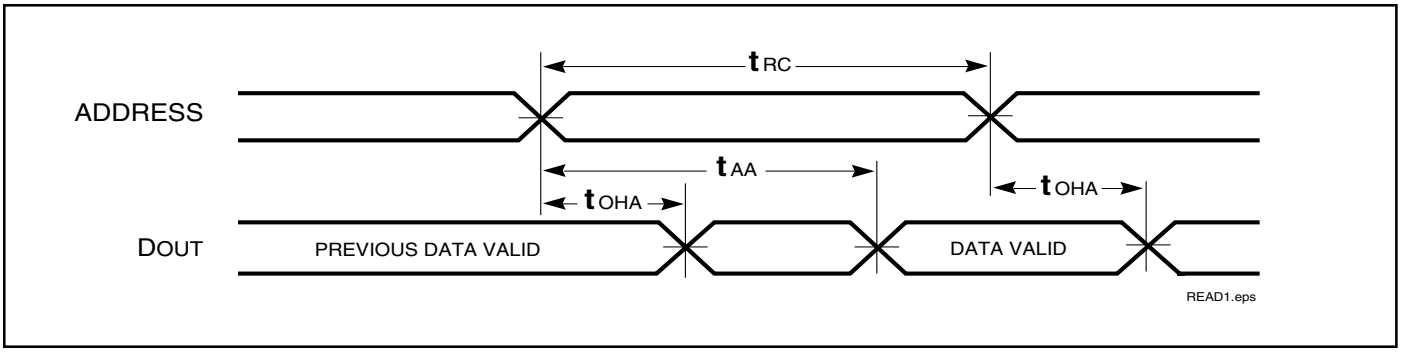


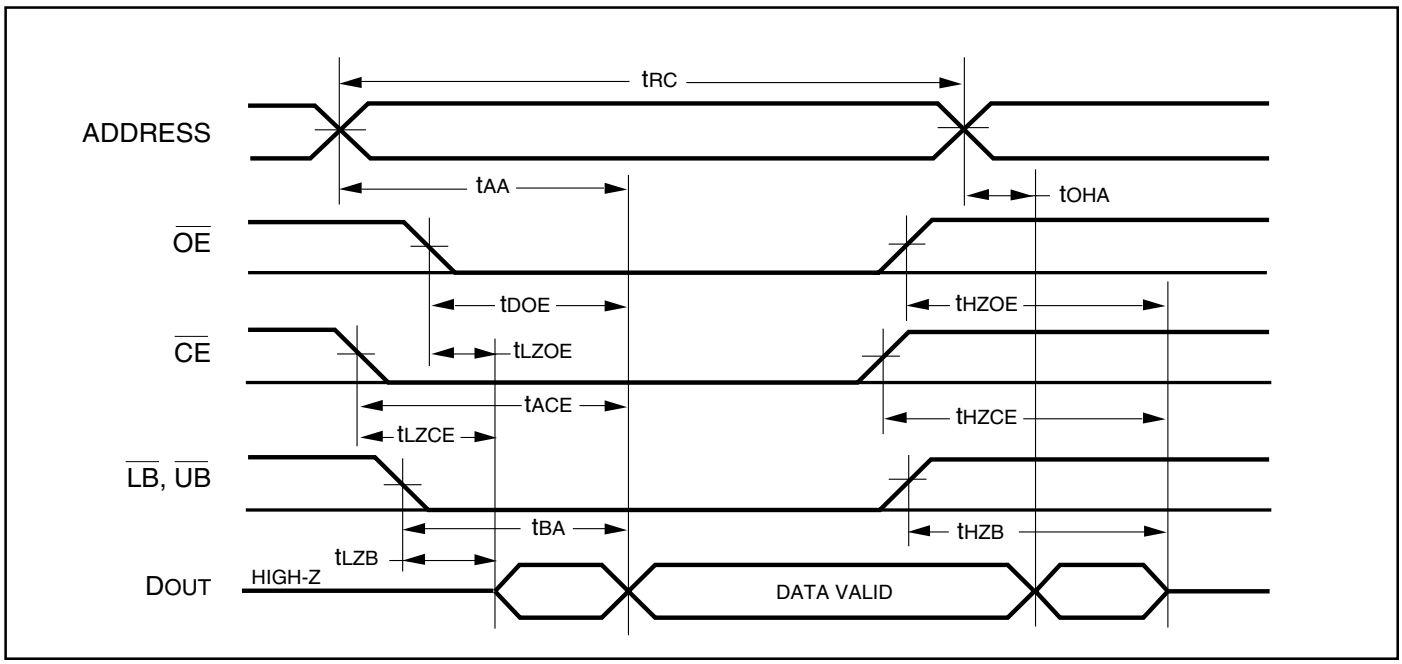
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

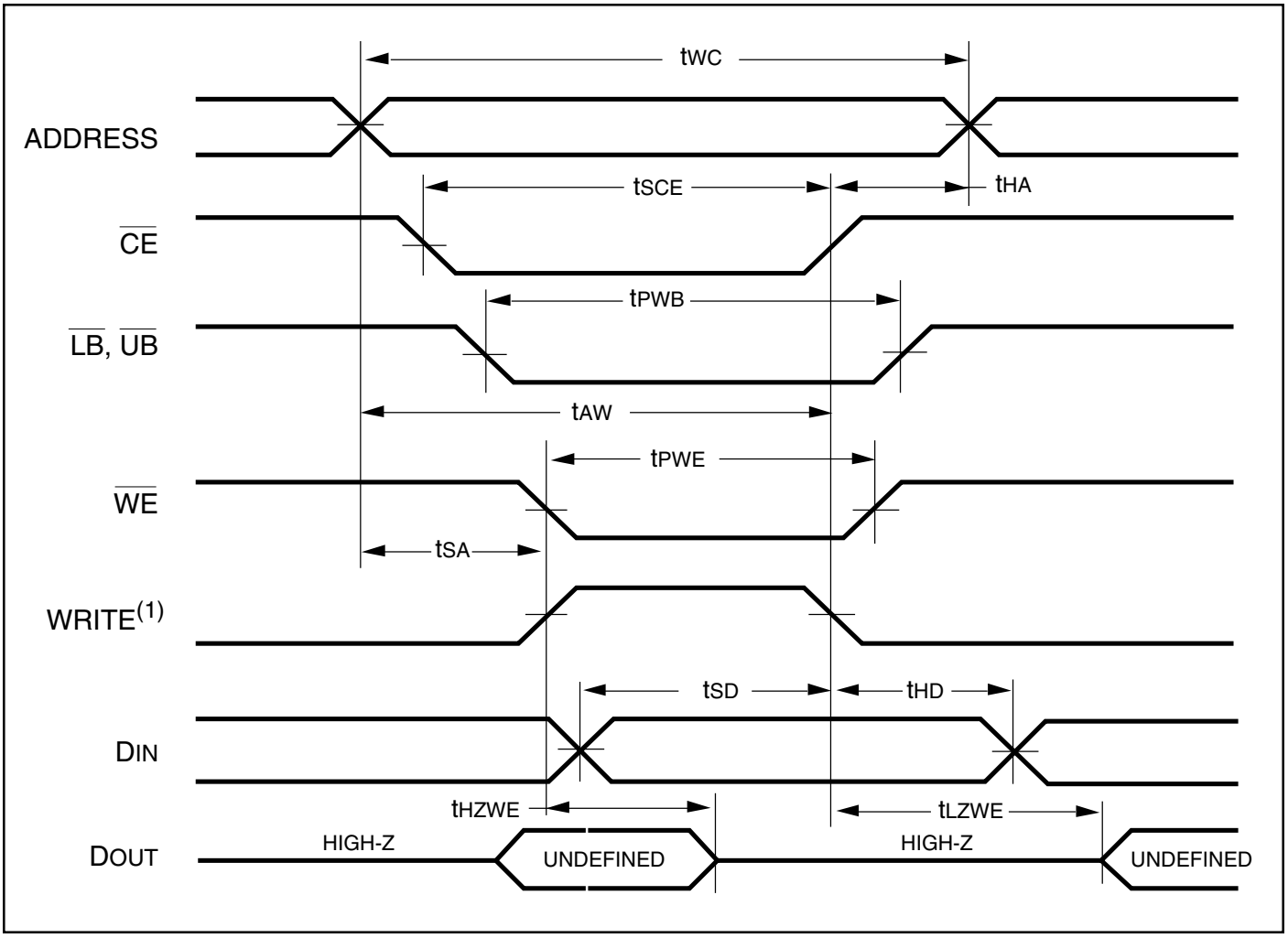
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		-20 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6	—	8	—	9	—	10	—	12	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	9	—	10	—	12	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	7	—	8	—	9	—	10	—	12	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	6	—	8	—	9	—	10	—	12	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	6	—	7	—	9	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	4	—	5	—	6	—	7	—	9	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
8	IS61LV6416-8B	mini BGA (6mm x 8mm)
8	IS61LV6416-8T	Plastic TSOP
8	IS61LV6416-8K	400-mil Plastic SOJ
10	IS61LV6416-10B	mini BGA (6mm x 8mm)
10	IS61LV6416-10T	Plastic TSOP
10	IS61LV6416-10K	400-mil Plastic SOJ
12	IS61LV6416-12B	mini BGA (6mm x 8mm)
12	IS61LV6416-12T	Plastic TSOP
12	IS61LV6416-12K	400-mil Plastic SOJ
15	IS61LV6416-15B	mini BGA (6mm x 8mm)
15	IS61LV6416-15T	Plastic TSOP
15	IS61LV6416-15K	400-mil Plastic SOJ
20	IS61LV6416-20B	mini BGA (6mm x 8mm)
20	IS61LV6416-20T	Plastic TSOP
20	IS61LV6416-20K	400-mil Plastic SOJ

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS61LV6416-8BI	mini BGA (6mm x 8mm)
8	IS61LV6416-8TI	Plastic TSOP
8	IS61LV6416-8KI	400-mil Plastic SOJ
10	IS61LV6416-10BI	mini BGA (6mm x 8mm)
10	IS61LV6416-10TI	Plastic TSOP
10	IS61LV6416-10KI	400-mil Plastic SOJ
12	IS61LV6416-12BI	mini BGA (6mm x 8mm)
12	IS61LV6416-12TI	Plastic TSOP
12	IS61LV6416-12KI	400-mil Plastic SOJ
15	IS61LV6416-15BI	mini BGA (6mm x 8mm)
15	IS61LV6416-15TI	Plastic TSOP
15	IS61LV6416-15KI	400-mil Plastic SOJ
20	IS61LV6416-20BI	mini BGA (6mm x 8mm)
20	IS61LV6416-20TI	Plastic TSOP
20	IS61LV6416-20KI	400-mil Plastic SOJ

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