Ordering number : EN8798

SANYO Semiconductors
DATA SHEET

LB11980H — Monolithic Digital IC For VCR Capstan Three-Phase Brushless Motor Driver

Overview

LB11980H is a 3-phase brushless motor driver optimal for driving the VCR capstan motors.

Features

- 3-Phase full-wave current-linear drive system.
- Torque ripple correction circuit built-in.(correction factor variable)
- Current limiter circuit built in.
- Output stage upper/lower over-saturation prevention circuit built in. (No external capacitor required)
- FG amplifier built in.
- Thermal shutdown circuit built in.

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
	VS max		25	V
Maximum output current	I_O max		1.3	A
Allowable power dissipation	Pd max	Mounted on a specified board *	1.81	W
		Independent IC	0.77	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 114mm×71.1mm×1.6mm, glass epoxy board

Allowable Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VS		5 to 24	V
	V_{CC}		4.5 to 5.5	V
Hall input amplitude	VHALL	Between hall inputs	±30 to ±80	mVo-p
GSENSE input range	VGSENSE	With respect to the control system ground	-0.20 to +0.20	V

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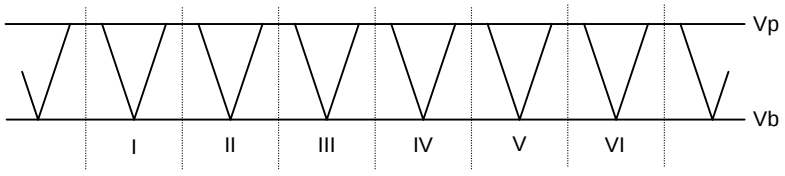
Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, VS = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} supply current	I_{CC}	R_L = ∞, VCTL = 0, VLIM = 0V (Quiescent)		12	18	mA
Output						
Output saturation voltage	$V_O$sat1	I_O = 500mA, Rf = 0.5Ω, sink+source VCTL = VLIM = 5V (With saturation prevention)		2.1	2.6	V
	$V_O$sat2	I_O = 1.0A, Rf = 0.5Ω, sink+source VCTL = VLIM = 5V (With saturation prevention)		2.6	3.5	V
Output leakage current	$I_O$leak				1.0	mA
FR						
FR pin input threshold voltage	VFSR		1.0	1.25	2	V
FR pin input input bias current	Ib (FSR)	VFR = 3V	100	150	200	μA
Control						
CTL pin input Input bias current	Ib (CTL)	VCTL = 5V		1.5	3	μA
CTL pin input motor current	Imctl	VCTL = 0V			5	mA
CTL pin control start voltage	VCTL (ST)	Rf = 0.5Ω, VLIM = 5V, I_O ≥ 10mA Hall input logic fixed (U, V, W = H, H, L)	2.25	2.50	2.75	V
CTL pin control Gm	Gm (CTL)	Rf = 0.5Ω, ΔI_O = 200mA Hall input logic fixed (U, V, W = H, H, L)	0.86	1.06	1.26	A/V
Current limit						
LIM pin input current	Ilim	VLIM = 3V		1.5	3	μA
LIM pin motor current	Imlim	VLIM = 0V			5	mA
LIM current limit offset voltage	Voff (LIM)	Rf = 0.5Ω, VCTL = 5V, I_O ≥ 10mA Hall input logic fixed (U, V, W = H, H, L)	1.0	1.25	1.5	V
LIM pin control Gm	Gm (lim)	Rf = 0.5Ω, VCTL = 5V Hall input logic fixed (U, V, W = H, H, L)	0.59	0.71	0.83	A/V
Hall amplifier						
Hall amplifier input offset voltage	VOFF (HALL)		-6		+6	mV
Hall amplifier input bias current	Ib (HALL)			1.0	3.0	μA
Hall amplifier common-mode input voltage	VCM (HALL)		1.3		3.3	V
TRC						
Torque ripple correction ratio	TRC	For the high and low peaks in the Rf waveform when I_O = 200mA (Rf = 0.5Ω, ADJ-OPEN) Note.2		13		%
ADJ pin voltage	VADJ		2.37	2.50	2.63	V
FG Amplifier						
FG amplifier input offset voltage	VOFF (FG)		-8		+8	mV
FG amplifier input bias current	Ib (FG)		-100			nA
FG amplifier output saturation voltage	$V_O$sat (FG)	Sink side; With internal pull-up resistance load		0.5	0.6	V
FG amplifier voltage gain	VG (FG)	For open loop at f = 10kHz	41.5	44.5	47.5	dB
FG amplifier common-mode input voltage	VCM (FG)		0.5		4.0	V
Schmitt amplifier						
Duty ratio	DUTY	Under specified conditions (RF = 39kΩ) Note 3	49.0	50	51.0	%
Upper side output saturation voltage	Vsatu (SH)	I_O = -20μA	4.8			V
Lower side output saturation voltage	Vsatd (SH)	I_O = 100μA			0.2	V
Hysteresis width	Vhys		32	46	60	mV
FGS output pin pull-up resistance	RFGout			4.7		kΩ
Saturation						
Saturation prevention circuit lower set voltage	V_O sat (DET)	Voltage between each OUT and Rf with I_O = 10mA, Rf = 0.5Ω, VCTL = VLIM = 5V	0.175	0.25	0.325	V
TSD						
TSD operating temperature	T-TSD	(Design target) Note.1		180		°C

Note 1. No measurements are made on the parameters with Note (Design target).

Note 2. The torque ripple compensation ratio is determined as follows from the Rf voltage waveform.



Each hall logic setting

GND level

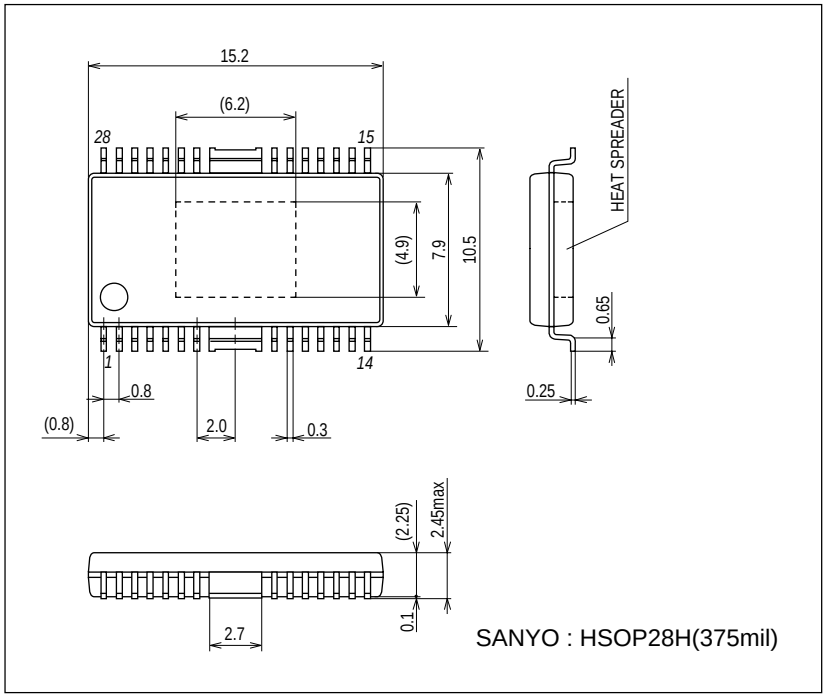
$$\text{Correnction ratio} = \frac{2^{*}(Vp - Vb)}{Vp + Vb} \quad 100^{*}(\%)$$

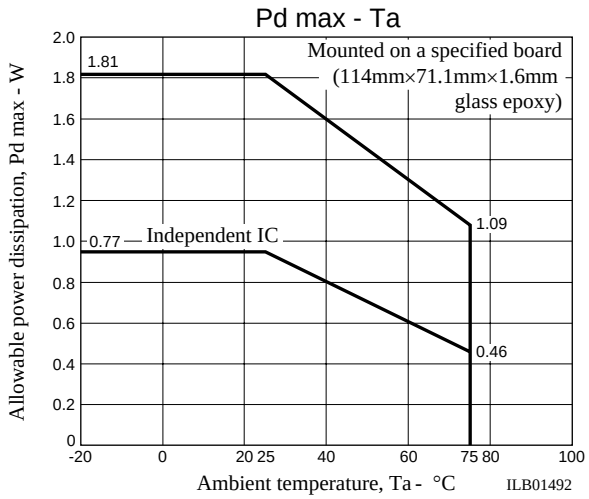
Note 3. Apply the sine wave of 1kHz, 20mVP-P under conditions with a sample circuit installed externally as shown above.

Package Dimensions

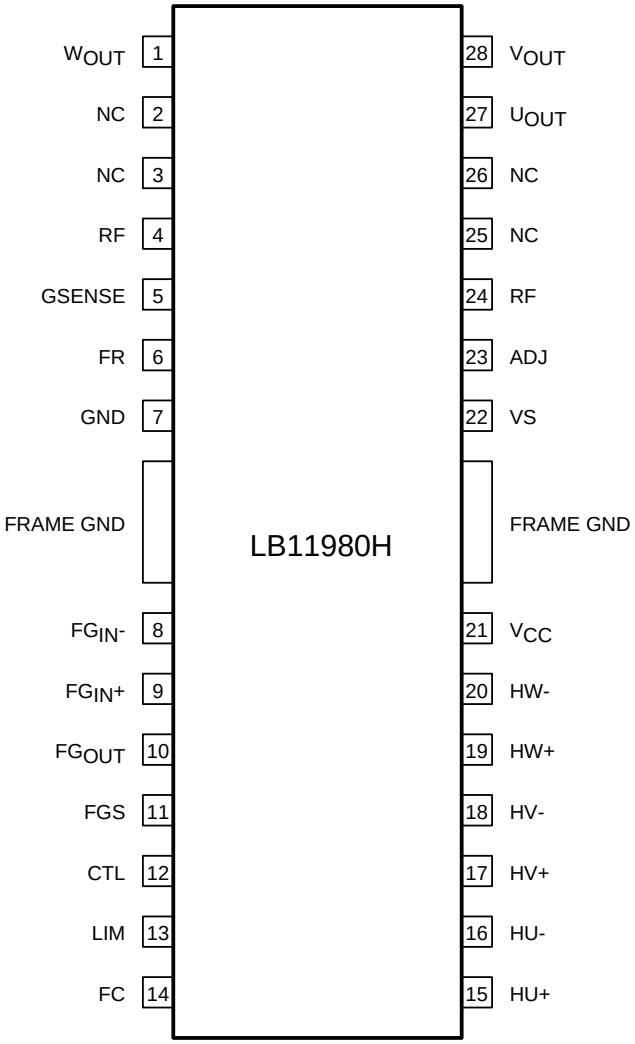
unit : mm (typ)

3233B



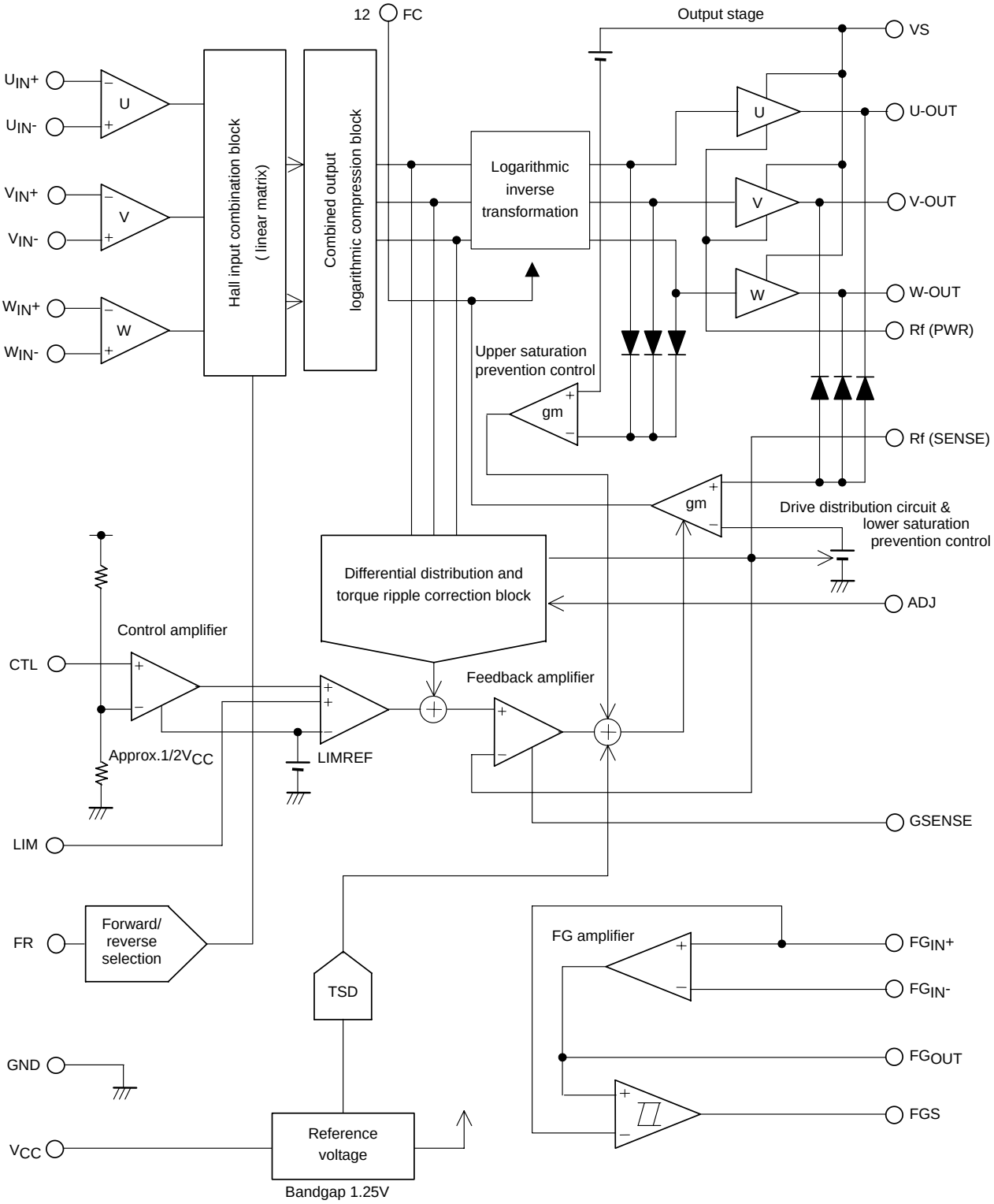


Pin Assignment



Top view

Block Diagram



Truth Table and Control Function

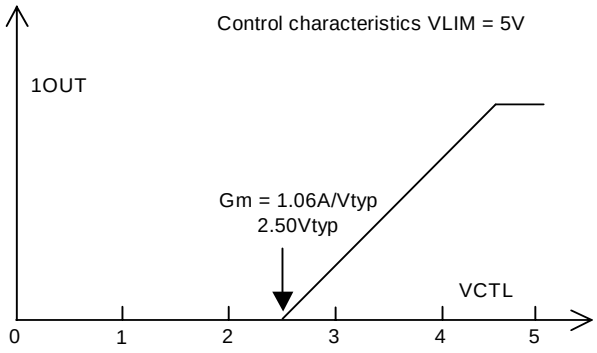
	Source → Sink	Hall input			FR
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

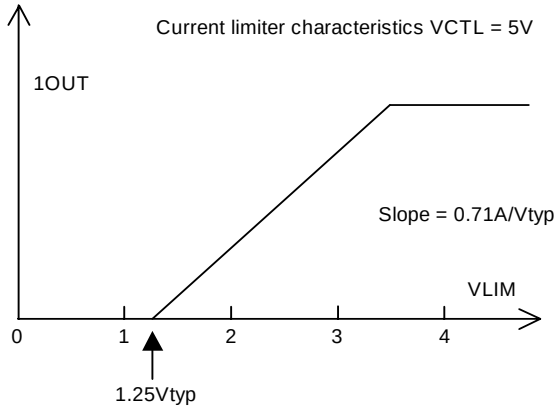
Note: “H” in the FR column represents a voltage of 2.75V or more. “L” represents a voltage of 2.25V or less. (At V_{CC} = 5V)

Note: “H” under the Hall Input columns represents a state in which “+” has a potential which is higher by 0.01V or more than that of the “-” phase inputs. Conversely “L” represents a state in which “+” has a potential which is lower by 0.01V or more than that of the “-” phase inputs.

Note: Since a 180° energized system is used as a drive system, other phases than the sink and source are not OFF.

[Control Function & Current Limiter Function]

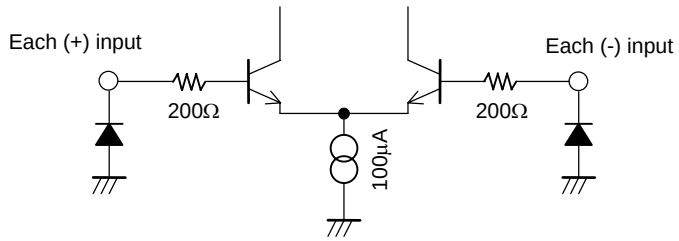
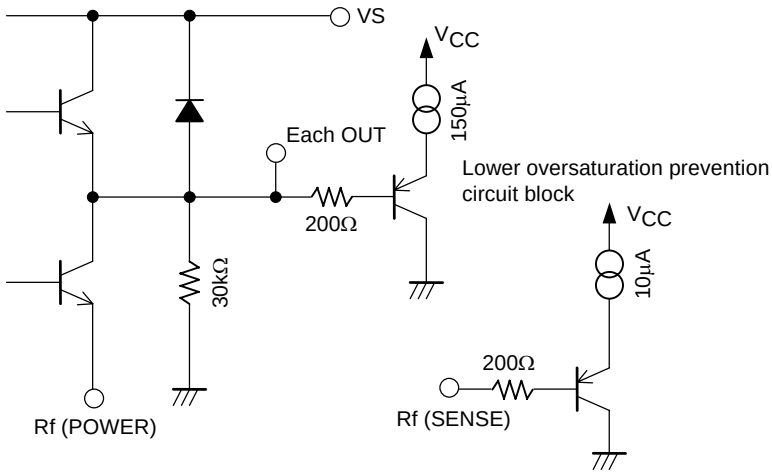
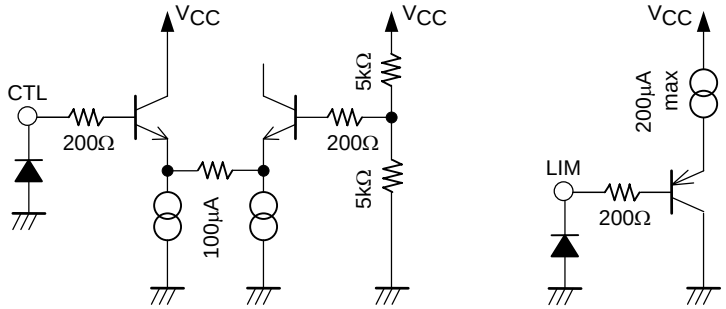
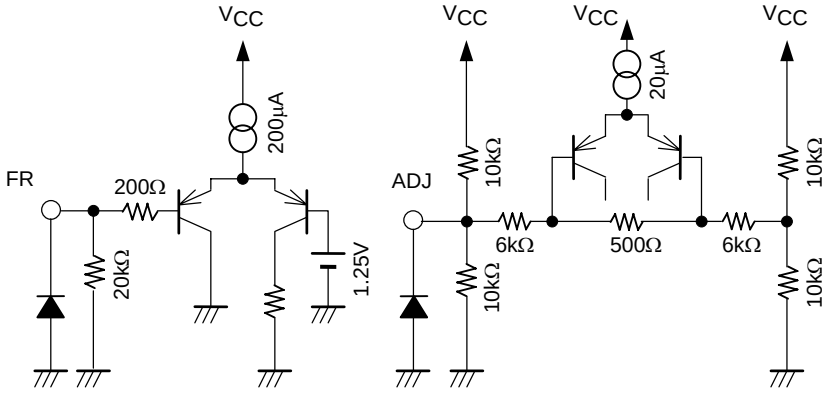




Pin Functions

Pin name	Pin no	Functions
FR	6	Forward/reverse select pin. This pin voltage determines forward/reverse. (Vth = 1.25V TYP at V_{CC} = 5V)
GND	7	GND for others than the output transistor. Minimum potential of output transistor is at Rf pin.
FG_{IN} (-)	8	Input pin for the FG amplifier to be used with inverted input. A feedback resistor is connected between this pin and FG OUT.
FG_{IN} (+)	9	Non-inverted input pin for the FG amplifier to be used as differential input. No bias is applied internally.
FG-OUT	10	FG amplifier output pin. Resistive load provided internally.
CTL	12	Speed control pin. Control is performed by means of constant current drive which is applied by current feedback from Rf. Gm = 1.06A/VTYP at Rf = 0.5Ω
LIM	13	Current limiter function control pin. This pin voltage is capable of varying the output current linearly. Slope = 0.71A/VTYP at Rf = 0.5Ω
FC	14	Speed control loop's frequency characteristics correction pin.
U_{IN}+, U_{IN}- V_{IN}+, V_{IN}- W_{IN}+, W_{IN}-	15, 16 17, 18 19, 20	U-phase Hall device input pin; logic "H" presents IN+>IN- V-phase Hall device input pin; logic "H" presents IN+>IN- W-phase Hall device input pin; logic "H" presents IN+>IN-
V_{CC}	21	Power supply pin for supplying power to all circuits expect output section in IC; this voltage must be stabilized so as to eliminate ripple and noise.
VS	22	Power supply pin for supplying power to output section in IC.
ADJ	23	Pin to be used to adjust the torque ripple correction factor externally. When adjusting the correction factor, apply voltage externally to the ADJ pin through a low impedance. Increasing the applied voltage decreases the correction factor; lowering the applied voltage increases the correction factor. The rate of change, when left open, ranges approximately from 0 to 2 times. (Approximately V_{CC}/2 is set internally and the input impedance is approximately 5kΩ.)
Rf (PWR) Rf (SNS)	24 4	Output current detection pins. Current feedback is provided to the control blocks by connecting Rf between the pins and GND. The operation of the lower over-saturation prevention circuit and torque ripple correction circuit depends on the pin voltage. In particular, since the oversaturation prevention level is set by the pin voltage, decreasing the Rf value extermely may cause the lower over-saturation prevention to work less efficiently in the large current region. The PWR pin and SENSE pin must be connected.
FGS	11	FG Schmidt amp output pin, that is pulled up with 4.7kΩ.
U_{OUT} V_{OUT} W_{OUT}	27 28 1	U-phase output pin. V-phase output pin. W-phase output pin. (Built-in spark killer diode)
GSENSE	5	GND sensing pin. By connecting this pin to GND in the vicinity of the Rf resistor side of the Rf included motor GND wiring, the influence that the GND common impedance exerts on Rf can be excluded. (Must not be left open.)

Each Input/Output Equivalent Circuit

Pin No.	Pin name	Input/Output equivalent circuit
15 16 17 18 19 20	U_{IN} (+) U_{IN} (-) V_{IN} (+) V_{IN} (-) W_{IN} (+) W_{IN} (-)	
27 28 1 22 24 4	U_{OUT} V_{OUT} W_{OUT} VS Rf (POWER) Rf (SENSE)	
12 13	CTL LIM	
6 23	FR ADJ	

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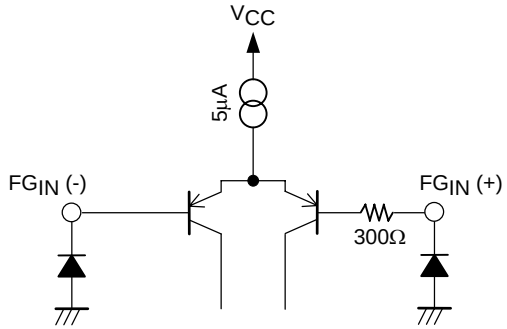
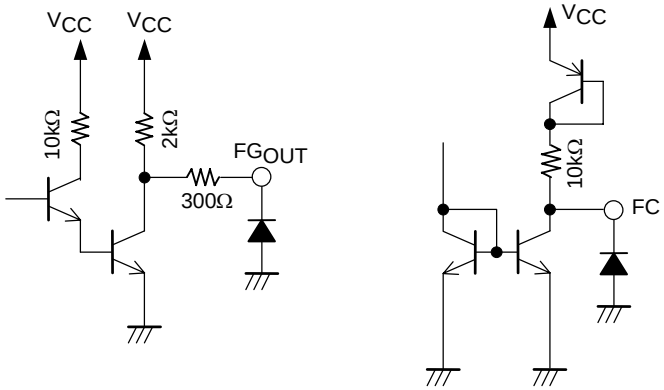
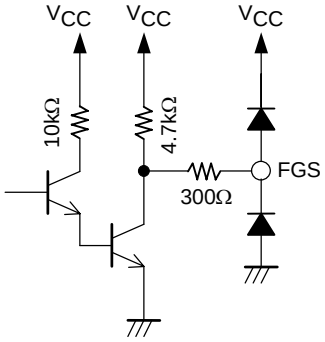
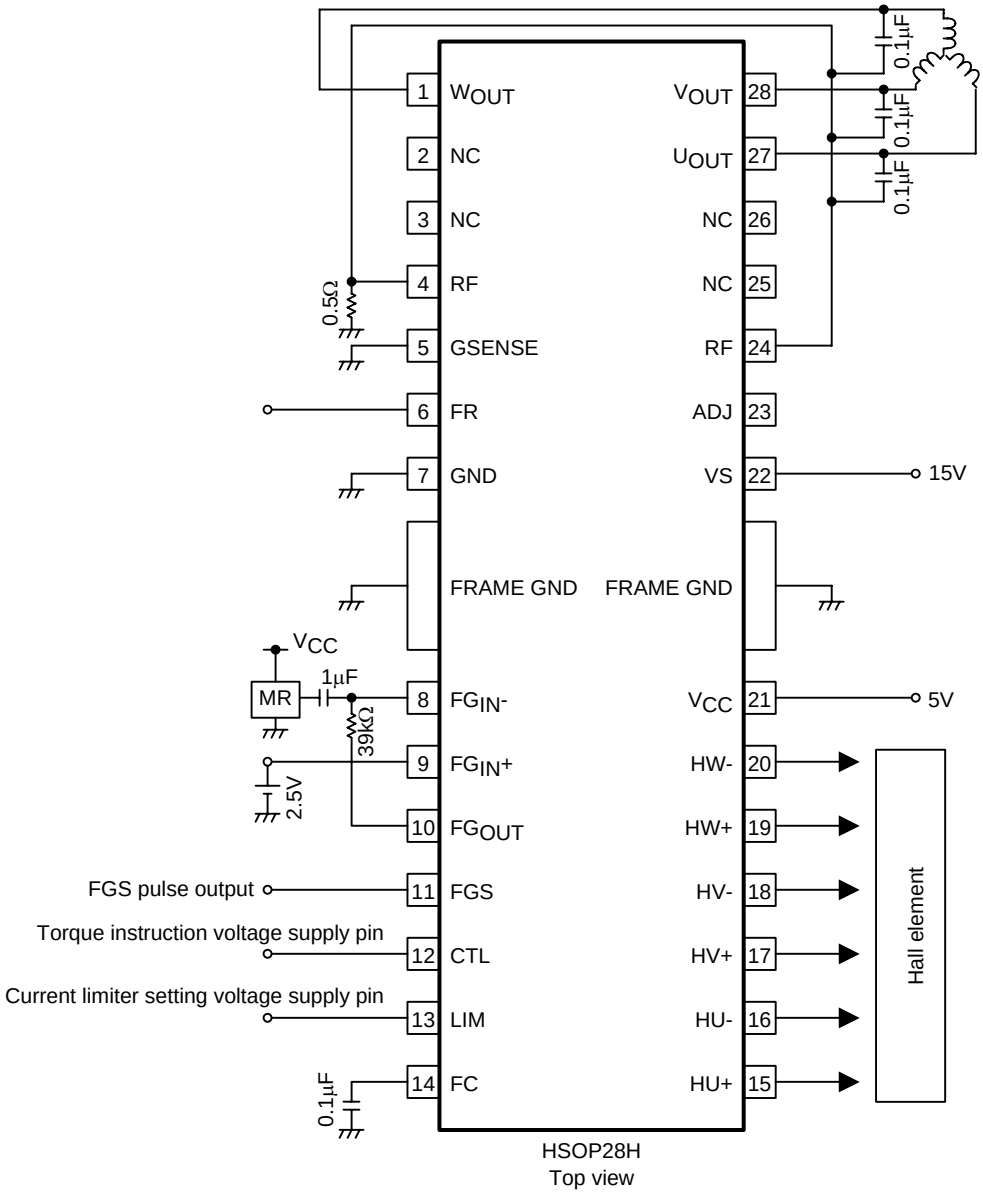
Pin No.	Pin name	Input/output equivalent circuit
8 9	FG_{IN} (-) FG_{IN} (+)	
10 14	FG_{OUT} FC	
11	FGS	

Sample Application Circuit



Note) The constant shown in this example is only for reference and does not guarantee the characteristics.
Connect a capacitor between power supply and GND and between Hall inputs as required.