Advanced 2/1-Phase PWM Controller for CPU Core Power

General Description

The RT8869A is an advanced 2/1-phase synchronous buck controller with 2 integrated MOSFET drivers. It integrates an 8-bit DAC that supports Intel VR11.x CPUs power application.

The IC adopts state-of-the-art dynamic phase control capability by PS1 pin and achieves high efficiency over a wide load range. It uses lossless $R_{DS(ON)}$ current sensing to achieve phase current balance. Other features include adjustable operating frequency, adjustable soft-start, short circuit protection, adjustable over current protection, over voltage protection, under voltage protection, power good indication, VR_HOT indication and $\overline{\text{VR\_SHDN}}$ indication.

The RT8869A is available in a small footprint with WQFN-40L 5x5 package.

Ordering Information

RT8869A □□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free))

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8869AZQW : Product Number

YMDNN : Date Code

Features

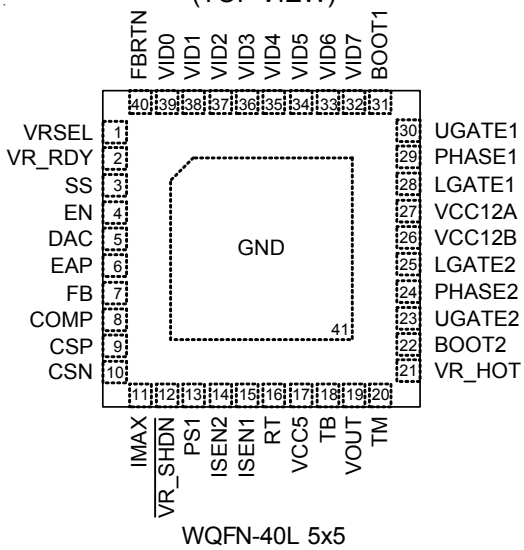
- **12V Power Supply Voltage**
- **2/1-Phase Power Conversion**
- **Integrated 2 MOSFET Drivers with Internal Bootstrap Diode**
- **Dynamic Phase Control Capability**
- **8-bit DAC Supports Intel VR11.x CPUs**
- **Lossless $R_{DS(ON)}$ Current Sensing for Current Balance**
- **Adjustable Frequency : 50kHz to 1MHz**
- **Adjustable Over Current Protection**
- **Adjustable Soft-Start**
- **VR_RDY, VR_HOT and $\overline{\text{VR\_SHDN}}$ Indications**
- **Small 40-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Desktop CPU Core Power
- Middle/High End Graphic Cards
- Low Voltage, High Current DC/ DC Converters

Pin Configurations

(TOP VIEW)



WQFN-40L 5x5

Typical Application Circuit

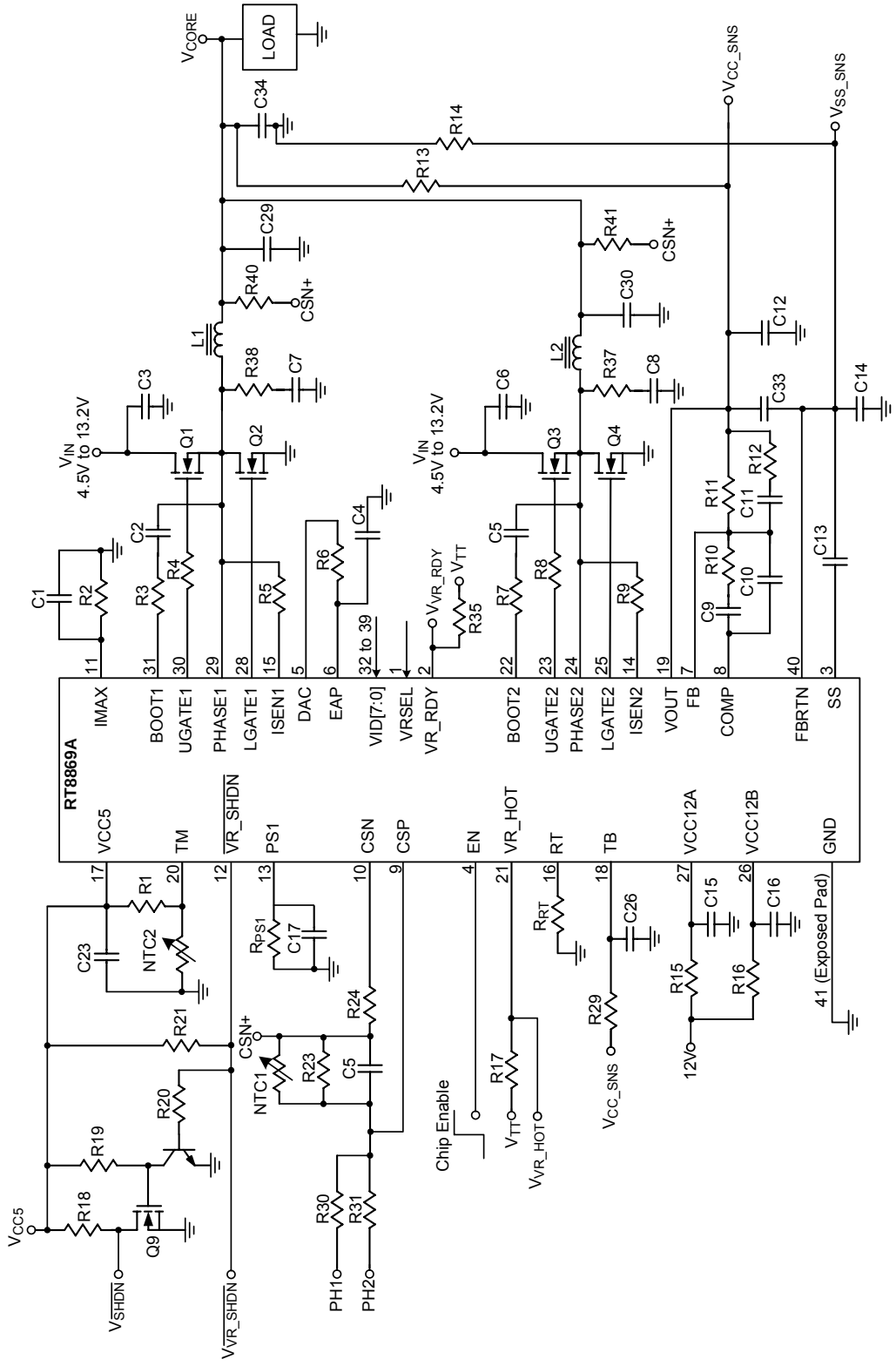


Table 1. VR11.1 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125

To be continued

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

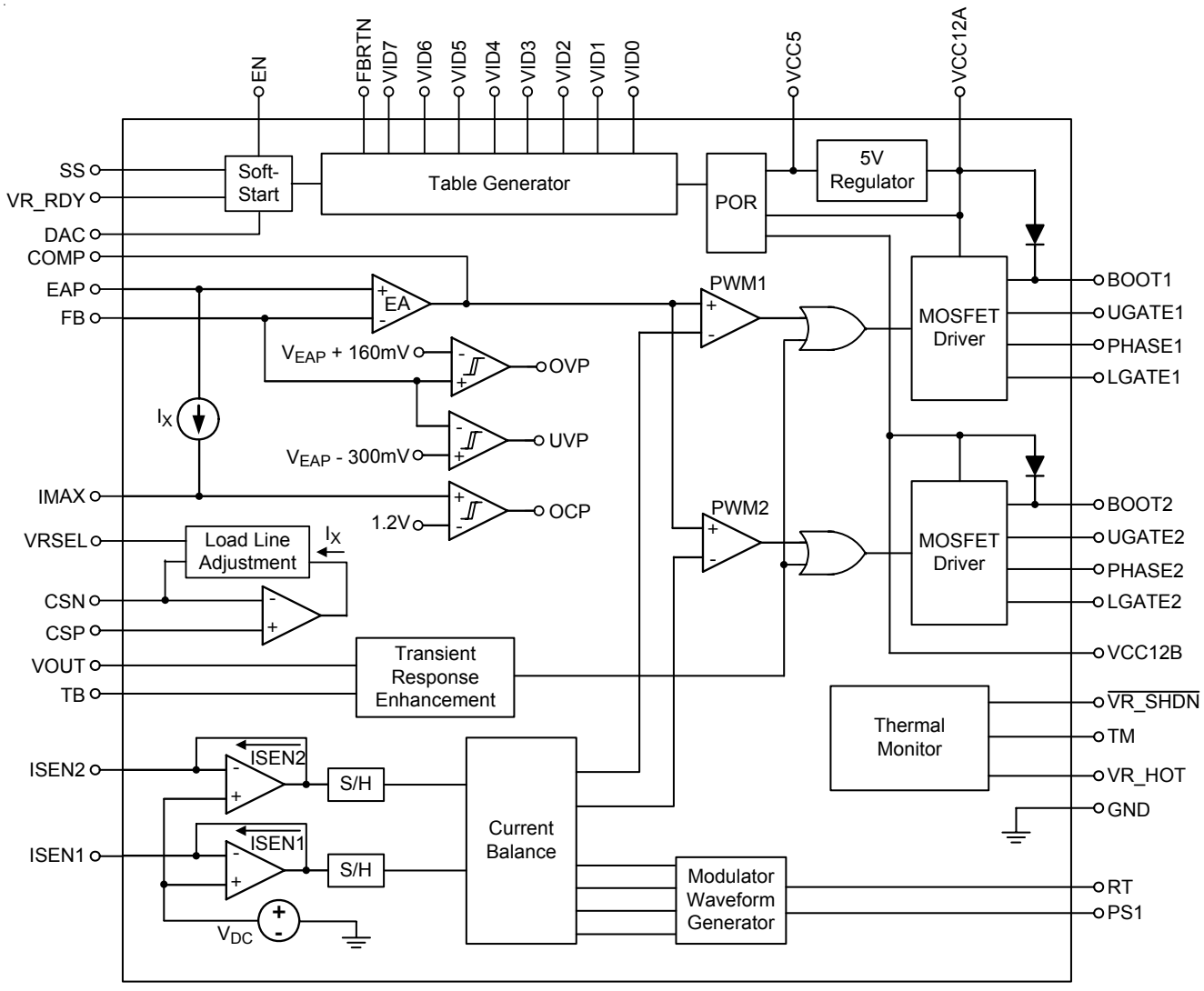
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VRSEL	Load Line Adjustment Enable Pin. Connect this pin to VTT and GND to disable and enable load line adjustment function respectively.
2	VR_RDY	VR Ready Indication.
3	SS	Soft-Start Ramp Slope Set Pin. Connect this pin to FBRTN by a capacitor to adjust soft-start slew rate.
4	EN	Chip Enable Pin. Pull this pin higher than 0.8V to enable the PWM controller.
5	DAC	DAC Output Pin. Connect a resistor from this pin to EAP pin for setting the load line slope.
6	EAP	Non-inverting Input of Error-Amplifier Pin. Connect a resistor from this pin to DAC pin to set the load line slope.
7	FB	Inverting Input of Error Amplifier Pin.
8	COMP	Compensation Pin. Output of error amplifier and input of PWM comparator.
9, 10	CSP, CSN	Input of Current Sensing Amplifier. The sensed current is for droop control and over current protection.
11	IMAX	Output Current Indication. Connect a resistor from this pin to GND to set the over current protection threshold.
12	$\overline{\text{VR\_SHDN}}$	$\overline{\text{VR\_SHDN}}$ Indication.
13	PS1	Dynamic Phase Control Threshold Input 1. Connect this pin to GND by a resistor to set dynamic phase control threshold.
14, 15	ISEN2, ISEN1	Phase Current Sense Pins for Phase 2 and Phase 1. Per phase current signal is sensed via the voltage across low side MOSFETs $R_{DS(ON)}$ for current balance.
16	RT	Switching Frequency Set Pin. Connect this pin to GND via a resistor to adjust switching frequency.
17	VCC5	Internal 5V Regulator Output.
18	TB	Transient Boost Pin. This pin along with the VOUT pin sets the transient boost function.
19	VOUT	Positive Voltage Sensing Pin. This pin is the positive node of the differential voltage sensing and along with TB pin sets the transient boost function.
20	TM	Thermal Monitoring Input Pin. Connect a resistive voltage divider with NTC to detect temperature.
21	VR_HOT	Thermal Monitoring Output Pin. Connect a resistor to VTT for VR_HOT signal assertion.
22, 31	BOOT2, BOOT1	Bootstrap Power Pins for Phase 2 and Phase 1. This pin powers the high side MOSFETs drivers. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode.
23, 30	UGATE2, UGATE1	Upper Gate Drivers for Phase 2 and Phase 1. This pin drives the gate of the high side MOSFETs.
24, 29	PHASE2, PHASE1	Switch Nodes of High Side Driver 2 and Driver 1. Connect this pin to high side MOSFETs sources together with the low side MOSFETs drains and inductor.
25, 28	LGATE2, LGATE1	Lower Gate Drivers for Phase 2 and Phase 1. This pin drives the gate of low side MOSFETs.

To be continued

Pin No.	Pin Name	Pin Function
26	VCC12B	Supply Input Pin. This pin supplies current for phase 2 gate driver.
27	VCC12A	Supply Input Pin. This pin supplies current for phase 1 gate driver and control circuits.
32 to 39	VID7 to VID0	Voltage Identification Input for DAC.
40	FBRTN	Return Ground Pin. This pin is negative node of the differential remote voltage sending.
41 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage (VCC12A, VCC12B) ---------- –0.3V to 15V
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  - DC ---------- –2V to 15V
  - < 20ns ---------- –5V to 30V
- UGATEx to GND ---------- (V_{PHASEx} – 0.3V) to (V_{BOOTx} + 0.3V)
  - < 20ns ---------- (V_{PHASEx} – 5V) to (V_{BOOTx} + 5V)
- LGATEx to GND ---------- (GND – 0.3V) to (V_{CC12x} + 0.3V)
  - < 20ns ---------- (GND – 5V) to (V_{CC12x} + 5V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–40L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN–40L 5x5, θ_{JA} ---------- 36°C/W
  - WQFN–40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage (VCC12A, VCC12B) ---------- 10.8V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC12x} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Current	I_{CC12}		--	6	--	mA
VCC5 Supply Voltage	V_{CC5}	I_{LOAD} = 10mA	4.9	5	5.1	V
VCC5 Output Sourcing	I_{VCC5}		10	--	--	mA
Soft-Start Current	I_{SS1}	VR_RDY = Low	68	80	92	μA
VID Change Current	I_{SS2}	VR_RDY = High	135	160	185	μA
Transient Boost Sinking Current	I_{TB}		9	10	11	μA
Thermal Management						
VR_HOT Threshold Level			41	43	48	%V_{CC5}
VR_HOT Hysteresis			--	7	--	%V_{CC5}
$\overline{VR\_SHDN}$ Threshold Level			30	32	34	%V_{CC5}

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power On Reset							
VCC12 Rising Threshold		$V_{CC12RTH}$	VCC12 Rising	9.2	9.6	10	V
VCC12 Hysteresis		$V_{CC12HYS}$	VCC12 Falling	--	0.9	--	V
VCC5 Rising Threshold		V_{CC5RTH}	VCC5 Rising	4.4	4.6	4.8	V
VCC5 Hysteresis		V_{CC5HYS}	VCC5 Falling	--	0.4	--	V
Enable Control							
EN Input Threshold Voltage	Logic-High	V_{IH}		0.8	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Oscillator							
Switching Frequency		f_{OSC}	R_{RT} = 24kΩ, for 2 Phase Operation	270	300	330	kHz
Adjustable Frequency Range				50	--	1000	kHz
Ramp Amplitude			(Note 5)	3.5	4	4.5	V
Maximum Duty			(Note 5)	61	66	71	%
RT Pin Voltage		V_{RT}		1.55	1.6	1.65	V
Reference Voltage and DAC							
DAC Accuracy			1V to 1.6V	–0.5	--	0.5	%
			0.8V to 1V	–8	--	8	mV
			0.5V to 0.8V	–10	--	10	mV
DAC Input Threshold Voltage (VID0 to VID7, VRSEL)	Logic-High	V_{IH}		0.8	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Error Amplifier							
DC Gain		A_{DC}	No Load	--	80	--	dB
Gain Bandwidth		GBW	C_{LOAD} = 10pF	--	10	--	MHz
Slew Rate		SR	C_{LOAD} = 10pF	10	--	--	V/μs
Output Voltage Range		V_{COMP}		0.5		3.6	V
Maximum Current		I_{EA_SLEW}		300	--	--	μA
Current Sense							
Maximum Current		I_{GMMAX}		100	--	--	μA
Input Offset Voltage		V_{OSCS}		–1	0	1	mV
IMAX Current Mirror Accuracy			I_{MAX} / I_{AVG}, 2 Phase Operation	368	400	432	%
Droop Current Mirror Accuracy			I_{DRP} / I_{AVG}, 2 Phase Operation	368	400	432	%
Gate Driver							
UGATE Drive Source		$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 8V 250mA Source Current	--	2	4	Ω
UGATE Drive Sink		$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 8V 250mA Sink Current	--	1	2	Ω
LGATE Drive Source		$R_{LGATEsr}$	V_{LGATE} = 8V	--	2	4	Ω
LGATE Drive Sink		$R_{LGATEsk}$	250mA Sink Current	--	0.8	1.6	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection						
Total Current Protection Threshold	V_{IMAX}		1.1	1.2	1.3	V
Over Voltage Threshold	V_{OVP}	$V_{FB} - V_{EAP}$	350	390	430	mV
Under Voltage Threshold	V_{UVP}	$V_{FB} - V_{EAP}$	–380	–300	–250	mV
Over Temperature Protection Threshold		(Note 5)	145	150	175	°C
Over Temperature Protection Hysteresis			--	20	--	°C
Output Pin Capability						
VR_HOT Sinking Capability	V_{VR_HOT}	I_{VR_HOT} = 4mA	--	0.05	0.2	V
VR_RDY Sinking Capability	V_{VR_RDY}	I_{VR_RDY} = 4mA	--	0.05	0.2	V
$\overline{\text{VR\_SHDN}}$ Sinking Capability	$V_{\overline{VR\_SHDN}}$	$I_{\overline{VR\_SHDN}}$ = 4mA	--	0.05	0.2	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high-effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

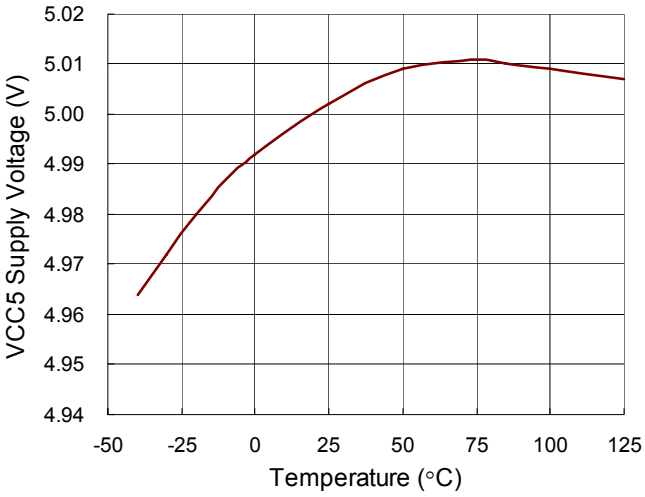
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

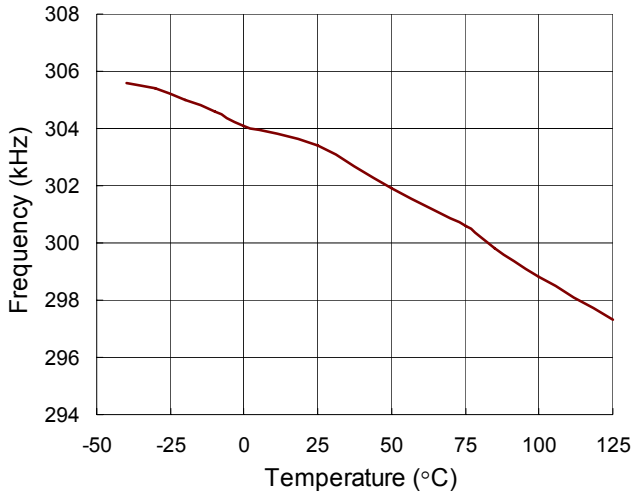
Note 5. Guaranteed by Design.

Typical Operating Characteristics

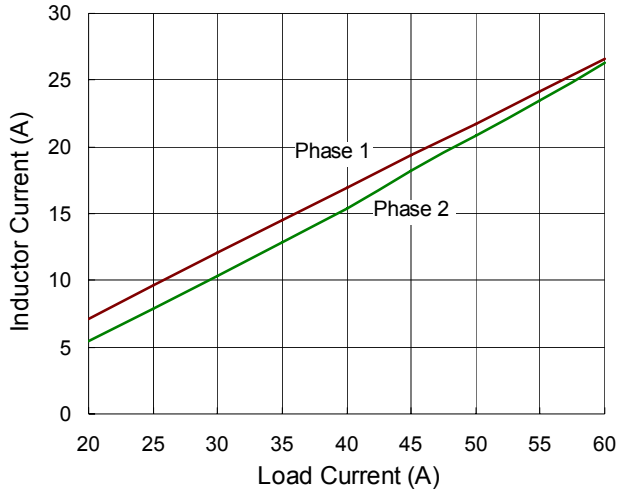
VCC5 Supply Voltage vs. Temperature



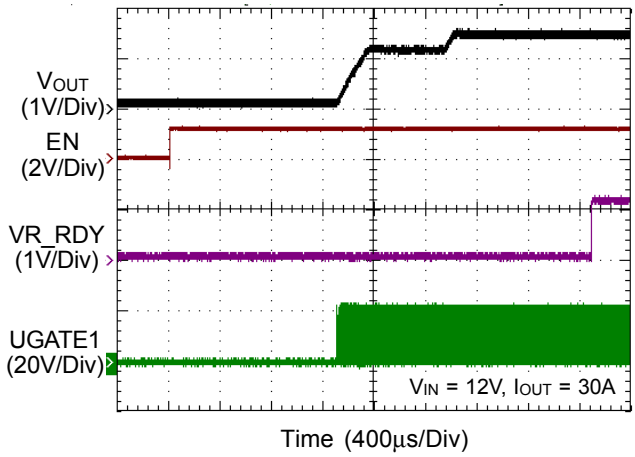
Frequency vs. Temperature



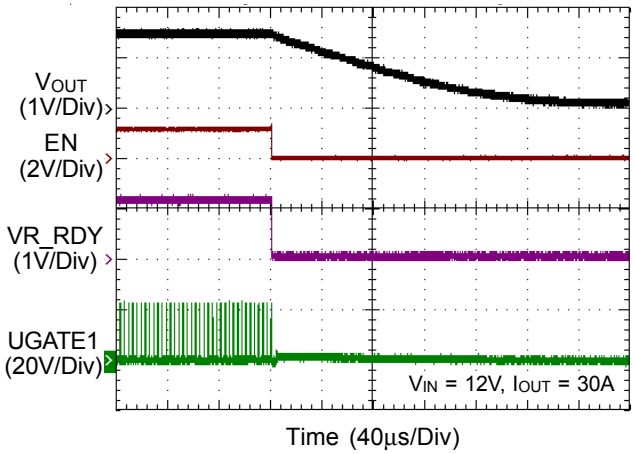
Inductor Current vs. Load Current



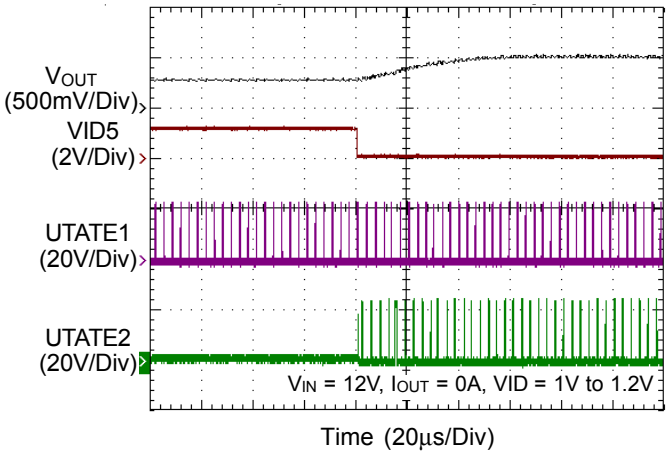
Power On from EN



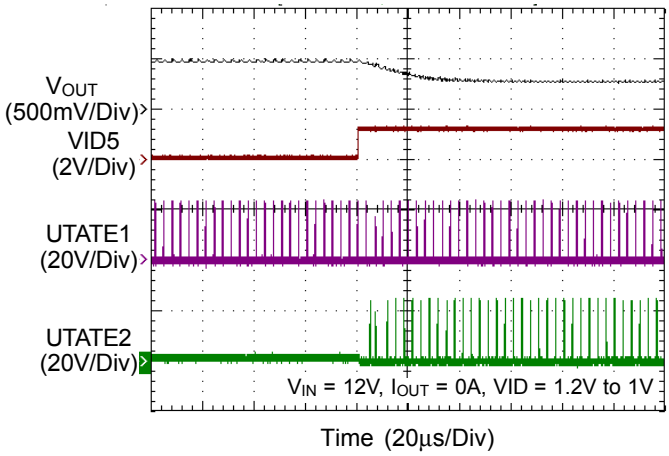
Power Off from EN



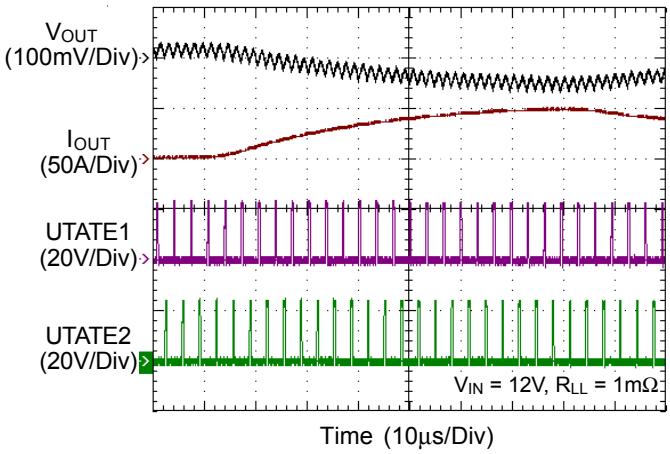
Dynamic Output Voltage Control



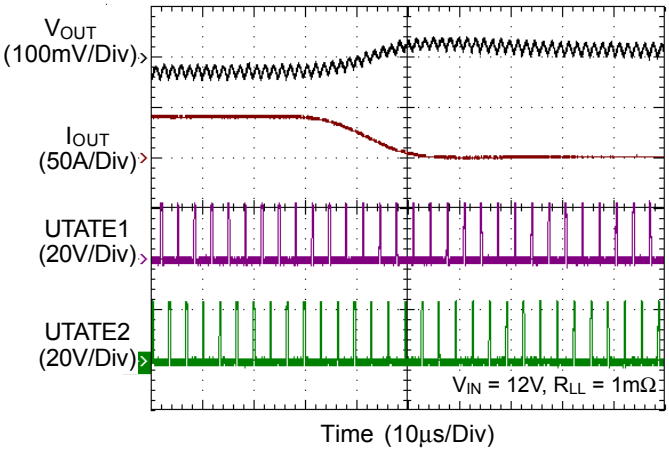
Dynamic Output Voltage Control



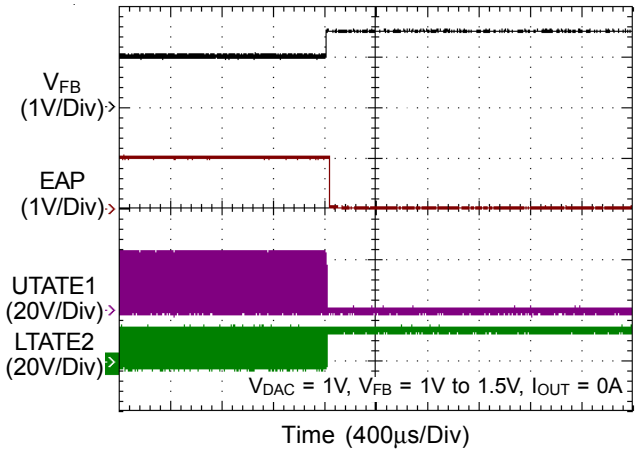
Load Step Up



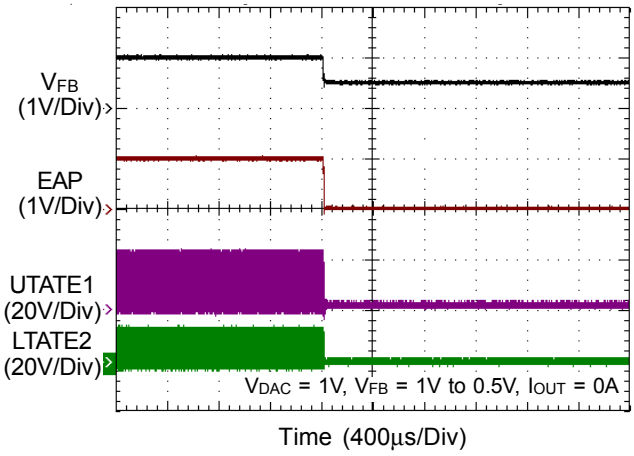
Load Step Down



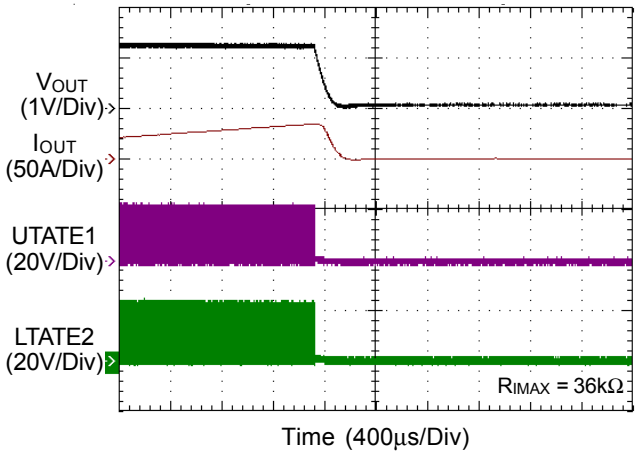
OVP



UVP



OCP



Application Information

The RT8869A is an advanced 2/1 phase synchronous buck controller with 2 integrated MOSFET drivers. It integrates an 8-bit DAC that supports Intel VR11.x VID tables.

Supply Voltage and POR

There are three supply voltage pins built in the RT8869A: VCC12A/VCC12B and VCC5. VCC12A/VCC12B are power input pins that receive an external 12V voltage for the embedded driver logic operation. VCC5 is a power output pin which is the output of an internal 5V LDO regulator. The 5V LDO regulator regulates VCC12A to generate a 5V voltage source for internal gate logic and external circuit biasing, e.g., OCP biasing. Since the VCC5 voltage is regulated, the variation of VCC5 (2%) will be much smaller than Platform ATX + 5V (5% to 7%). The maximum supply current of VCC5 is 10mA, which is designed only for controller circuit biasing. The recommended configuration of the RT8869A supply voltages is as follows: Platform ATX + 12V to the VCC12A/VCC12B pins, and decoupling capacitors on the VCC12A/VCC12B and VCC5 pins (minimum 0.1μF). The initialization of the RT8869A requires all the voltage on VCC12A/VCC12B and VCC5 to be ready. Since VCC5 is regulated internally from VCC12A, the VCC5 voltage will be ready (>4.6V) after VCC12A reaches about 7V, so there is no power sequence problem between VCC12A/VCC12B and VCC5. After VCC5 > 4.6V and VCC12A/VCC12B > 9.6V, the internal power-on-reset (POR) signal goes high. This POR signal indicates the power supply voltages are all ready. When POR = high and EN = high, the RT8869A initiates soft-start sequence. When POR = low, the RT8869A will try to turn off both high side and low side MOSFETs to prevent catastrophic failure.

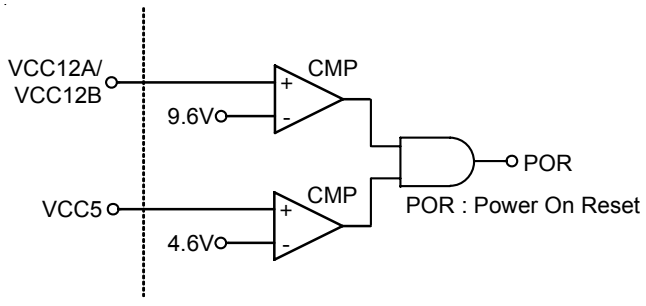


Figure 1. Circuit for Power Ready Detection

Switching Frequency

The switching frequency of the RT8869A is set by an external resistor connected from the RT pin to GND. The frequency follows the graph in Figure 2.

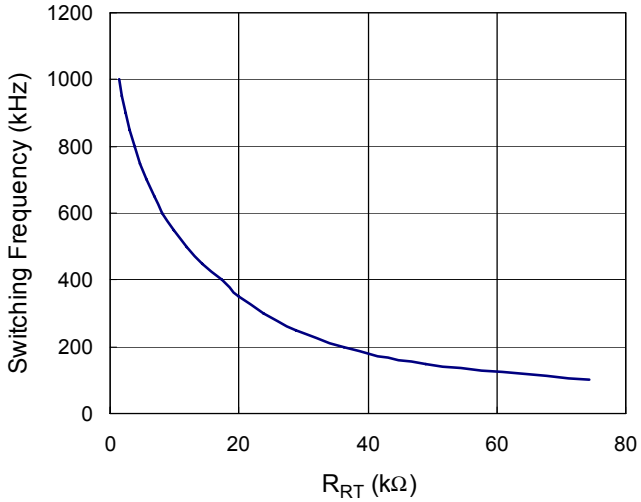


Figure 2. Switching Frequency vs. R_{RT} Resistance

Soft-Start

The V_{OUT} soft-start slew rate is set by a capacitor from the SS pin to FBRTN. Before power on reset (POR = low), the SS pin is held at GND. After power on reset (POR = high, EN = high) and an extra delay of 1600μs (T1), the controller initiates ramping up. V_{OUT} will always trace V_{EAP} during normal operation of the RT8869A, where V_{EAP} is the positive input of the error amplifier, which can be described as $V_{EAP} = V_{DAC} – V_{DROOP}$. (The definition of V_{DROOP} will be described later in the Load Line section). The first ramping up duration of V_{OUT} (T2) ramps V_{OUT} to V_{BOOT}.

After V_{OUT} ramps to V_{BOOT}, the RT8869A stays in this state for 800μs (T3), waiting for a valid VID code sent by the CPU. After receiving the valid VID code, V_{OUT} continues ramping up or down to the voltage specified by VID code. After V_{OUT} ramps to $V_{EAP} = V_{DAC} – V_{DROOP}$, the RT8869A stays in this state for 1600μs (T5) and then asserts VR_RDY = high. The ramping slew rate of T2 and T4 is controlled by the external capacitor connected to SS pin. The voltage of the SS pin will always be VEAP+0.7V, where the mentioned 0.7V is the typical turn-on threshold of an internal power switch. Before VR_RDY = high, the slew rate of V_{EAP} is limited to 80μA/C_{SS}. When VR_RDY

= high, the slew rate of V_{EAP} is limited to 160μA/C_{SS}, which is 2 times faster than the soft-start slew rate for dynamic VID feature. The soft start waveform is shown in Figure 2.

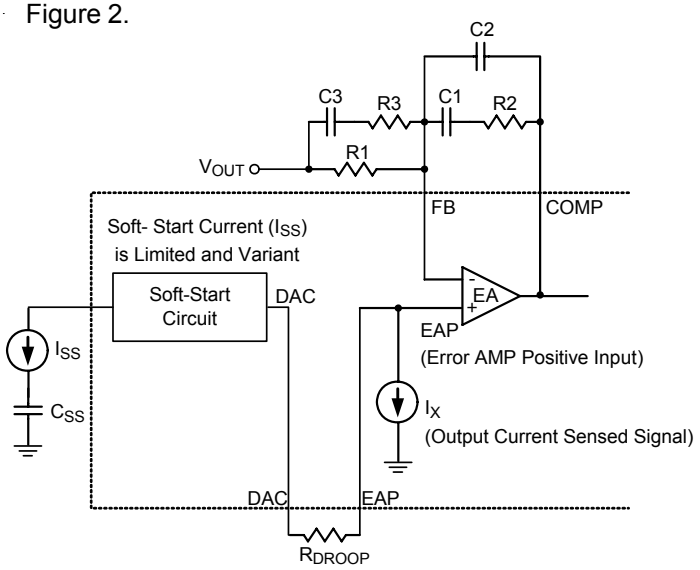


Figure 3. Circuit for Soft-Start and Voltage Control Loop

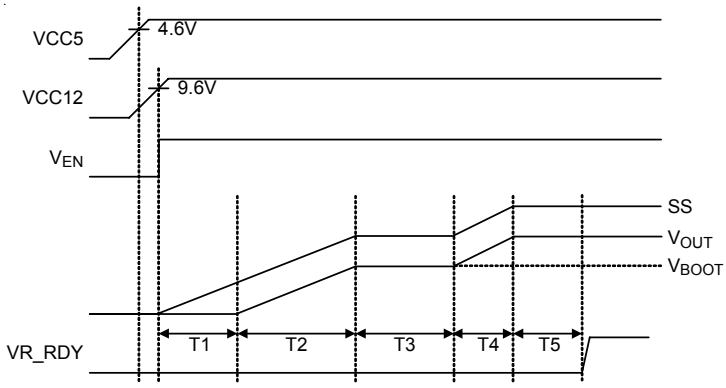


Figure 4. Soft-Start Waveforms

T1 is the delay time from power on reset state to the beginning of V_{OUT} rising. T2 is the soft-start time from V_{OUT} = 0 to V_{OUT} = V_{BOOT}. T3 is the dwelling time for V_{OUT} = V_{BOOT}. T4 is the soft-start time form V_{OUT} = V_{BOOT} to V_{OUT} = V_{DAC}.

T5 is the VR_RDY delay time.

T1 = 1600μs + 0.7V x C_{SS} /80μA.

T2 = V_{BOOT} x C_{SS}/80μA.

T3 ≈ 800μs.

T4 ≈ |V_{DAC} – V_{BOOT}| x C_{SS}/80μA.

T5 ≈ 1600μs.

Dynamic VID

The RT8869A can accept VID input changing while the controller is running. This allows the output voltage (V_{OUT}) to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID On-The-Fly (OTF). A VID OTF can occur under either light or heavy load conditions. The CPU changes the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative. Theoretically, V_{OUT} should follow V_{DAC} which is a staircase waveform, but in real application, the bandwidth of the converter is finite while the staircase waveform needs infinite bandwidth to follow. Thus, undesired V_{OUT} overshoot (when V_{DAC} changes up) or undershoot (when V_{DAC} changes down) is often observed in this type of design.

However, for the RT8869A, as mentioned before in the soft-start section, V_{DAC} slew rate is limited by I_{SS2}/C_{SS} when VR_RDY = high. This slew rate limiter works as a low-pass filter of V_{DAC} and makes the bandwidth of V_{DAC} waveform finite. By smoothening the V_{DAC} staircase waveform, V_{OUT} will no longer overshoot or undershoot. On the other hand, C_{SS} will increase the settling time of V_{OUT} during VID OTF. In most cases, a 5nF to 30nF ceramic capacitor will be suitable for C_{SS}.

Output Voltage Differential Sensing

The RT8869A uses a high gain low offset error amplifier for differential sensing. The CPU voltage is sensed between the FB and FBRTN pins. A resistor (R_{FB}) connects FB pin with the positive remote sense pin of the CPU (V_{CC_SNS}), while the FBRTN pin connects directly to the negative remote sense pin of the CPU (V_{SS_SNS}). The error amplifier compares V_{EAP} (= V_{DAC} – V_{DROOP}) with the V_{FB} to regulate the output voltage.

Transient Boost

In steady state, the voltage of V_{OUT} is controlled to be very close to V_{EAP}, however a load step transient from light load to heavy load could cause V_{OUT} to be lower than V_{EAP} by several tens of mV. In conventional buck converter design (without non-linear control) for CPU VR application, due to limited control bandwidth, it is hard for the VR to prevent V_{OUT} undershoot during quick load transient from light load to heavy load. Hence, the RT8869A builds in a

state-of-the-art transient boost function which detects load transient by monitoring V_{OUT}. If V_{OUT} suddenly DROOPs below "V_{TB}" the transient boost signal rises up and the RT8869A turns on all high side MOSFETs and turns off all low side MOSFETs. The voltage difference "$V_{OUT} - V_{TB}$" is set by following equation :

$V_{OUT} - V_{TB} = 10\mu A \times R_{TB}$.

Sensitivity of the transient boost can be adjusted by varying the values of C_{FB} and R_{FB}. Smaller R_{FB} and/or larger C_{FB} will make transient boost easier to be triggered. Figure 5 shows the circuit and typical waveforms.

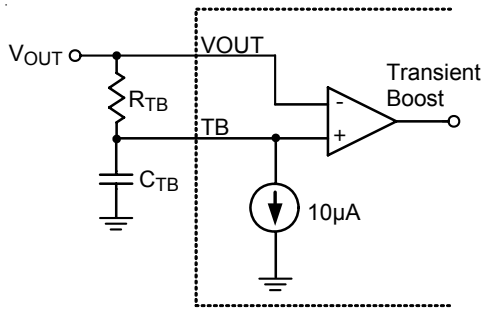


Figure 5. (a) Transient Boost Circuit

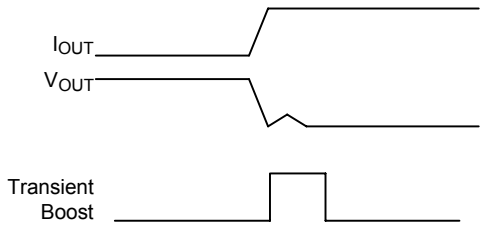


Figure 5. (b) Typical Waveforms

Output Current Sensing

The RT8869A provides a low input offset current-sense amplifier (CSA) to monitor the output current. The output current of CSA (I_X) is used for load line control, dynamic phase control and over current protection. In this average inductor current sensing topology, R_S and C_S must be set according to the equation below :

$$Requ = R_X // R_{NTC}$$

$$\frac{L}{DCR} = \frac{R_S \times C_S}{N + \frac{R_S}{Requ}}$$

Where the constant N is a set maximum operation phase number, not affected by the dynamic phase control machine. Then, the output current of CSA will follow the equation below :

$$I_X = \frac{I_{OUT} \times DCR}{N \times R_{CSN}}$$

Figure 6 is the current sense circuit.

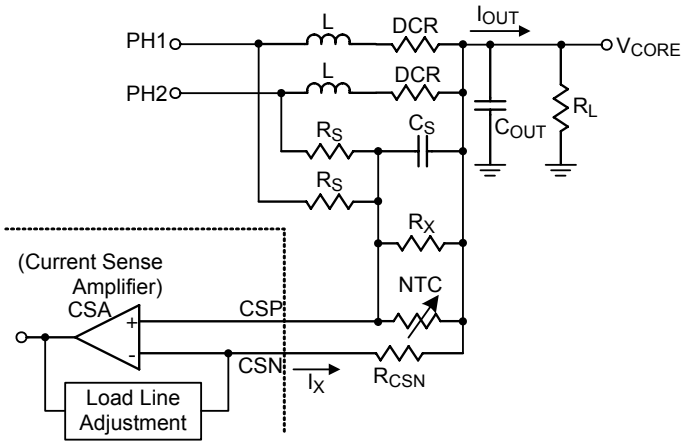


Figure 6. Circuit for Current Sensing

Load Line

The RT8869A utilizes inductor DCR current sense technique for load line control function. The sensed output current is proportionally mirrored from the I_X signal to the R_{DROOP} resistor to establish the voltage of V_{DROOP}. V_{DROOP} subtracted from V_{DAC} generates V_{EAP}. The voltage control loop is shown in Figure 3. Because I_X is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect in parallel with the capacitor C_S. If the NTC resistor is properly selected to compensate the temperature coefficient of I_X, the V_{DROOP} voltage will be proportional to I_{OUT} without temperature effect. In the RT8869A, the positive input of error amplifier is V_{EAP} and V_{OUT} will follow "$V_{DAC} - V_{DROOP}$". Thus, the output voltage which decreases linearly with I_{OUT} is obtained. The load line is defined as :

$$LL(Load\ Line) = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{\Delta V_{DROOP}}{\Delta I_{OUT}} = \frac{DCR \times R_{DROOP} \times 4}{N \times R_{CSN}}$$

Basically, the resistance of R_{DROOP} sets the resistance of the load line. The temperature coefficient of R_{DROOP} compensates the temperature effect of the load line.

Connecting VRSET pin to GND can enable load line adjustment function. Meanwhile, the current I_X is decreased by 10mV/R_{CSN}, and the minimum output current sensing range is also reduced by 10mV/R_{CSN}.

Current Balance

The RT8869A sensed per phase current signal I_{SENx} via the voltages on the low side MOSFETs switch on resistance ($R_{DS(ON)}$) for current balance as shown in Figure 7, in which I_{SENx} is defined as :

$$I_{SENx} = \frac{I_{PHASEx} \times R_{DSON} + V_{DC}}{R_{SENx}}$$

Where V_{DC} is the offset voltage for the current balance circuit.

In Figure 7, the phase current sense signals I_{SENx} are used to raise or lower the internal sawtooth waveforms (RAMP [1] and RAMP [2]) which are compared with error amplifier output (COMP) to generate a PWM signal. The raised sawtooth waveform will decrease the PWM duty of the corresponding phase current and the lowered sawtooth waveform will increase the PWM duty of the corresponding phase current. Eventually, current flowing through each phase will be balanced.

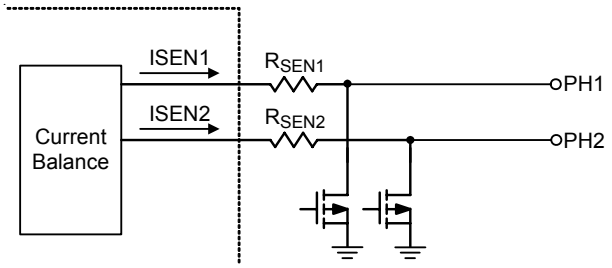


Figure 7. Circuit for Current Balance

Dynamic Phase Control Capability

The RT8869A has the ability to automatically control its phase number according to the total load current. Connect a resistor to ground at PS1 pin to set the 1-2 phase transition threshold, V_{PS1}.

The voltage at IMAX pin (V_{IMAX}) represents total current information, and the RT8869A will compare V_{IMAX} with V_{PS1} to determine the number of operating phases. Figure 8 shows the typical connections of PS1 pin for setting the dynamic phase control thresholds.

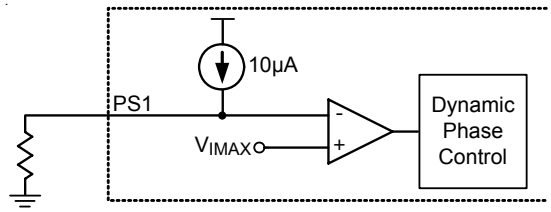


Figure 8. Circuit for Dynamic Phase Control and VR Shutdown

Table 2. Dynamic Phase Control

V_{IMAX}	Phase Number
V_{PS1} > 1.6V V_{IMAX} = Don't Care	Forced 1
0.8V < V_{PS1} < 1.6V V_{IMAX} = Don't Care	Forced 2
> V_{PS1}	2
< V_{PS1}	1

After setting the voltage at the PS1 pin, the RT8869A will continuously compare V_{IMAX} and V_{PS1} after POR. Once the V_{IMAX} enters each voltage state mentioned in Table 2, the RT8869A will automatically change its operation phase number. See Table 2 for the dynamic phase control mechanism. For Example, if V_{PS1} = 0.3V, the RT8869A will operate in 2 phase operation when V_{IMAX} = 0.9V, and 1 phase operation when V_{IMAX} = 0.1V. There are two states mentioned in Table 2 that the RT8869A will be forced not to change its operating phase number, and the V_{IMAX} voltage is meaningless for dynamic phase control circuit under these conditions.

Over Current Protection (OCP)

When V_{IMAX} is higher than 1.2V, the over current protection is triggered with 100µs delay to prevent false trigger, and the short circuit OCP level is designed at 1.6V with 10µs delay. The controller will turn off all high side / low side MOSFETs to protect CPU. Note that, the OCP level does not change according to different operating phase numbers.

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds "V_{EAP} + 390mV", OVP is triggered and latched. The RT8869A will turn on low side MOSFET and turn off high side MOSFET to protect CPU.

Under Voltage Protection (UVP)

The under-voltage protection monitors the output voltage via the FB pin. Once VFB is lower than "V_{EAP} – 300mV", UVP is triggered and latched. The RT8869A will turn off all high side / low side MOSFETs to protect CPU.

Loop Compensation

The RT8869A is a voltage mode controller and requires external compensation. To compensate a typical voltage mode buck converter, there are two ordinary compensation schemes, commonly known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator lies with the platform designers, and the main concern deals with the position of the capacitor ESR zero and mid-frequency to high frequency gain boost. Typically, the ESR zero of output capacitor will tend to stabilize the effect of output LC double poles. Hence, the position of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. Figure 9 shows a typical control loop using type-III compensator. Below is the compensator design procedure.

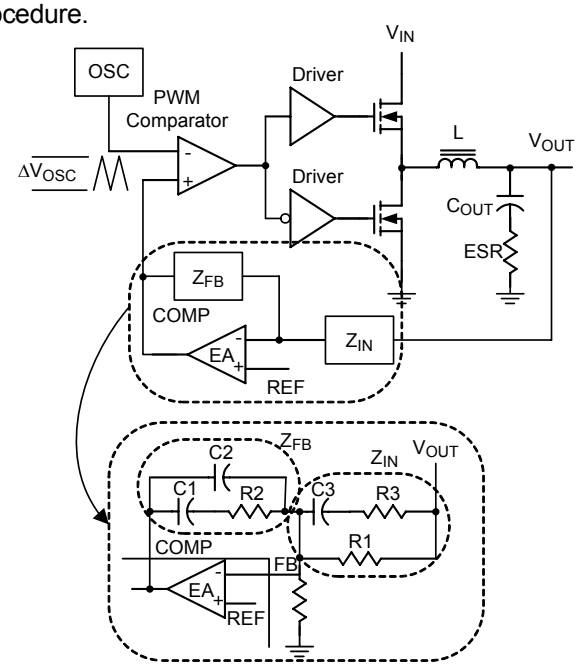


Figure 9. Compensation Circuit

1) Modulator Characteristic

The modulator consists of the PWM comparator and power stage. The PWM comparator compares the error amplifier output (COMP) with oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) gate-driving signal. The PWM wave is smoothed out by the output filter, L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier. The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output). This transfer function is dominated by a DC gain, a double pole, and an ESR zero as shown in Figure 10. The DC gain of the modulator is the input voltage (VIN) divided by the peak-to-peak oscillator voltage V_{OSC}. The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter is expressed as:

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires the output capacitor to have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as the following equation :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

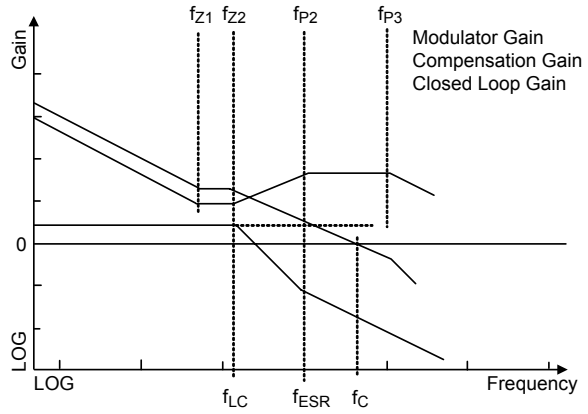


Figure 10. Bode Plot of Loop Gain

2) Design of the Compensator

A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (usually greater than 45°) and the highest bandwidth (0dB crossing frequency, f_C) possible. It is also recommended to manipulate the loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. According to Figure 10, the location of poles and zeros are :

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{Z2} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times C3 \times R3}$$

$$f_{P3} = \frac{1}{2\pi \times \frac{C1 \times C2 \times R2}{C1 + C2}}$$

Generally, f_{Z1} and f_{Z2} are designed to cancel the double pole of the modulator. Usually, place f_{Z1} at a fraction of f_{LC}, and place f_{Z2} at f_{LC}. f_{P2} is usually placed at f_{ESR} to cancel the ESR zero, and f_{P3} is placed below the switching frequency to cancel high frequency noise.

For a given bandwidth, R2, f_{Z1}, f_{Z2}, f_{P2}, f_{P3}, then

$$C1 = \frac{1}{2\pi \times R2 \times f_{Z1}}$$

$$C3 = \frac{G_{MOD@BW}}{2\pi \times f_C \times R2}$$

$$R1 = \frac{1}{2\pi \times f_{Z2} \times C3}$$

$$R3 = \frac{1}{2\pi \times f_{P2} \times C3}$$

$$C2 = \frac{1}{2\pi \times f_{P3} \times C1 \times R2 - 1}$$

Thermal Monitoring (VR_HOT&$\overline{\text{VR\_SHDN}}$)

The RT8869A provides thermal monitoring function via sensing the TM pin voltage, and which can set 2 thresholds to indicate ambient temperatures through the voltage divider R1 and R_{NTC}. The voltage of TM is typically set to be higher than 0.5 x VCC5 when ambient temperature is lower than VR_HOT & $\overline{\text{VR\_SHDN}}$ assertion target. However, when ambient temperature rises, TM voltage will fall, and the VR_HOT signal will be set to high if TM voltage DROOPs below 0.43 x VCC5. Furthermore, if the temperature continues to rise and the TM voltage is lower than 0.32 x VCC5, the controller will shutdown and pull the $\overline{\text{VR\_SHDN}}$ signal to low. Accordingly, VR_HOT will be reset when TM voltage rises above 0.5 x VCC5, but the controller will not reboot once thermal shutdown occurs.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8869A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 packages, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (36°C/W) = 2.778W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8869A package, the derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

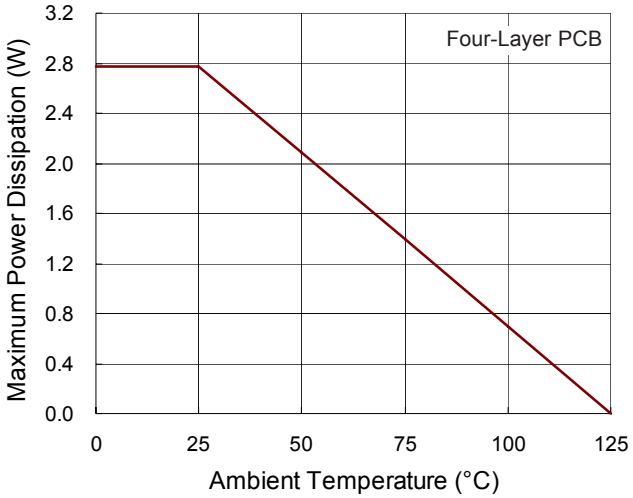
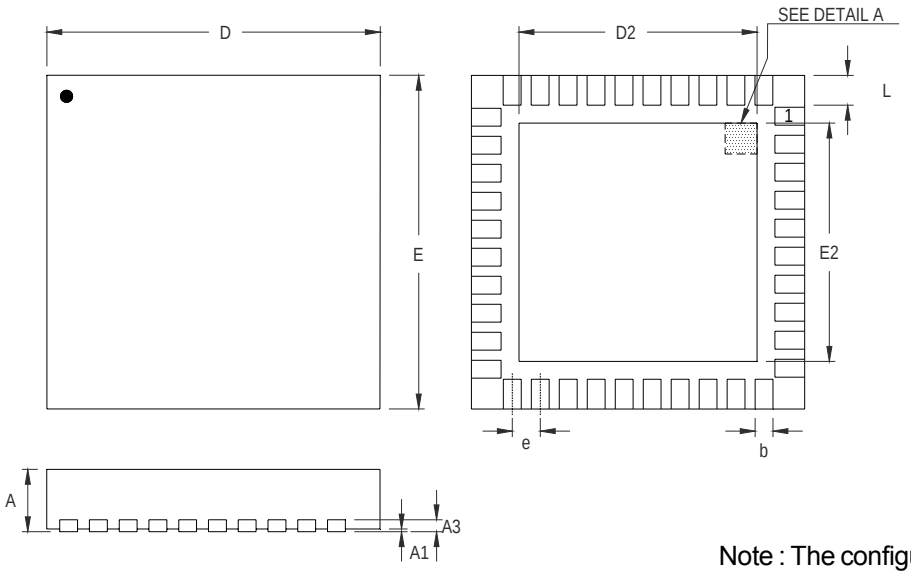
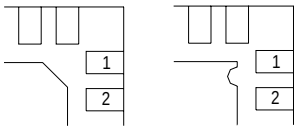


Figure 11. Derating Curve for RT8869A Package

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com