偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT9051

SYNC SINGAL PROCESSOR FOR MULTI-SYNC DISPLAY

Data Sheet

REV1.0

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新竹市科學工業園區工業東九路24號2樓
2F, No. 24, Industry E. 9th RD., Science-Based Industrial Park, Hsin-Chu, Taiwan
TEL:886-3-5780241FAX:886-3-5794278.5770419
Email:support@weltrend.com.tw

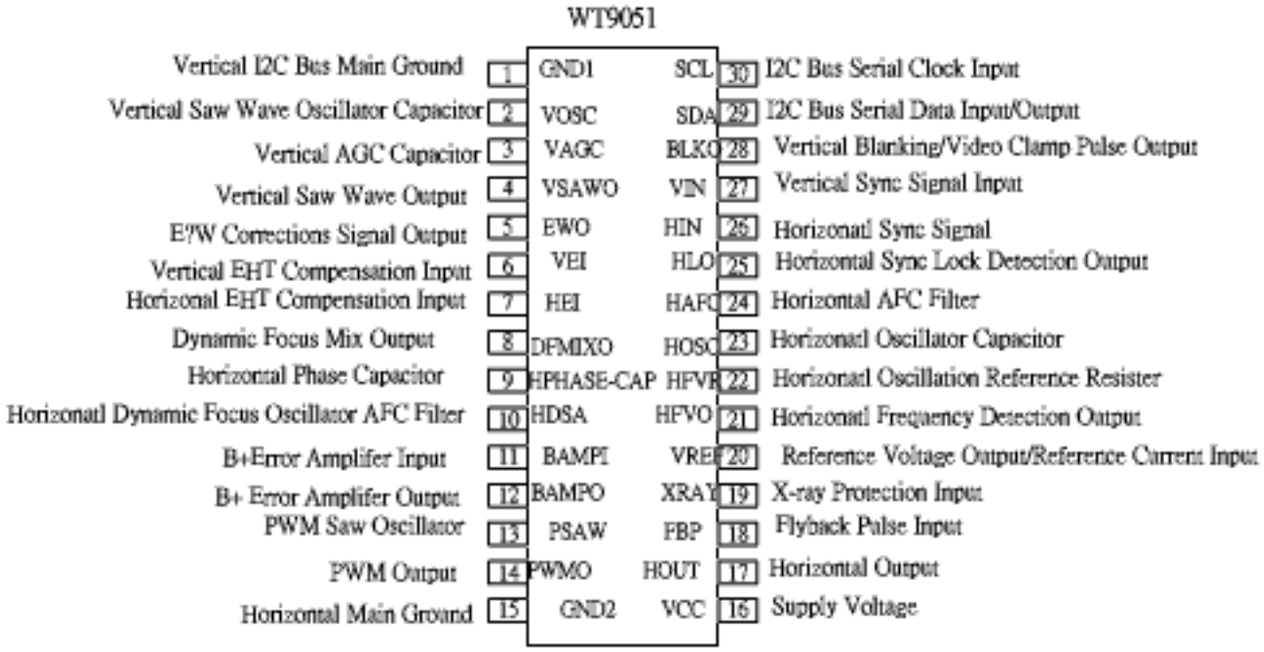
GENERAL DESCRIPTION

WT9051 is a sync signal processor for Multi-sync display.
The horizontal/vertical sync signal processing, the geometry compensation, the horizontal/vertical mixed dynamic focus, the PWM, and the D/A converter are incorporated on a chip.
These functions are controlled by the I^2C bus, it is easy to design application.

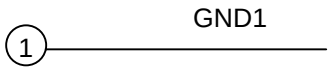
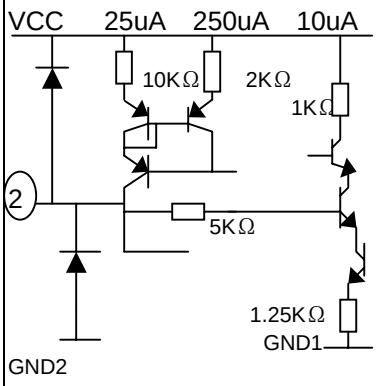
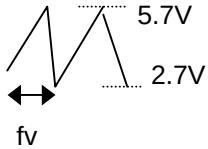
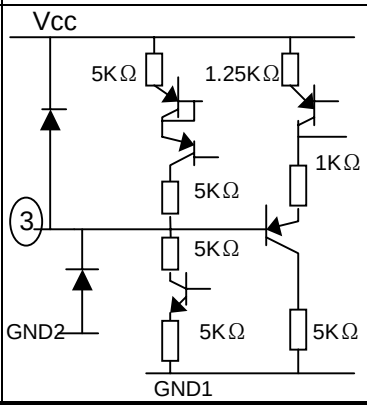
FEATURES

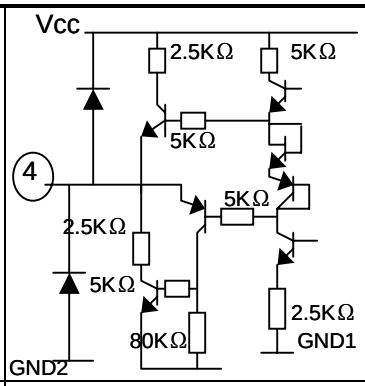
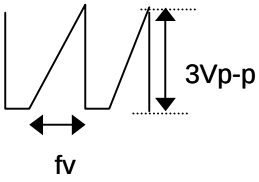
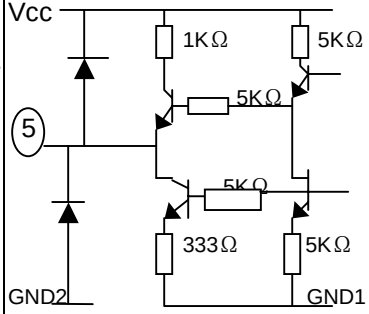
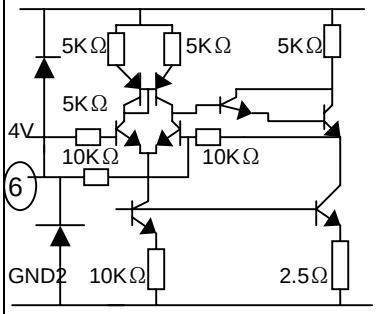
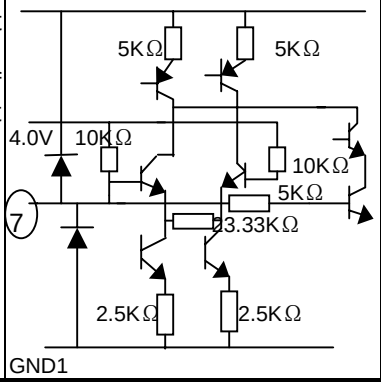
- Automatic Sync. Processing
- I^2C bus control: All functions are controlled by I^2C bus.
- Geometry compensation function: Geometry compensation circuits are integrated on a chip for Vertical Linearity S/C, trapezoid, side pin , side pin corner Top &Bottom individually, parallelogram and side pin balance
- D/A converter: D/A converter are integrated on a chip for variable amount.
- Horizontal/Vertical mixed
- Dynamic Focus
- Horizontal/Vertical Moire Canceller: Moire cancel amount can be controlled.
- Horizontal/Vertical Size control: Horizontal/vertical screen size can be controlled by 8bits.
- Horizontal/Vertical Position control: Horizontal/vertical screen position can be controlled by 8bits.
- Polarity normalization circuit: Both positive and negative polarity are acceptable.
- Vertical blanking pulse and video clamp pulse generation circuit: Sand castle output. Vertical blanking pulse width can be changed.
- Horizontal output duty adjustable
- Horizontal Lock detection circuit
- B+ Supply function
- EHT compensation for horizontal &vertical
- X-ray protection

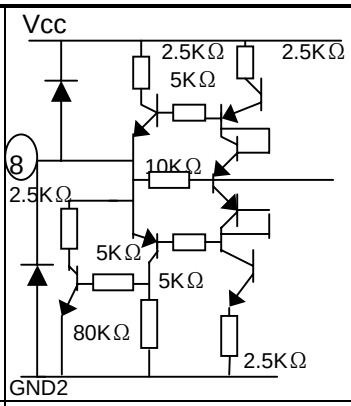
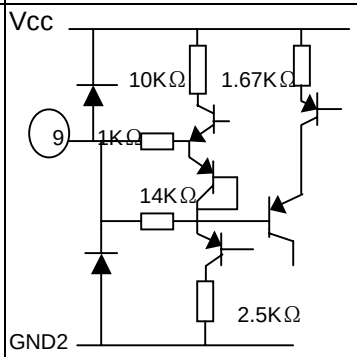
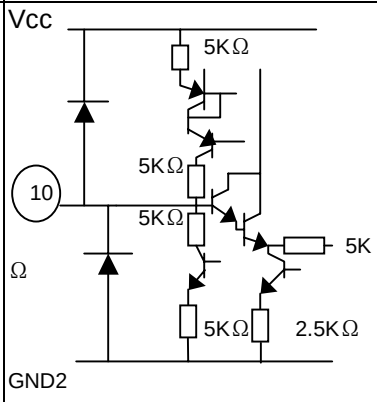
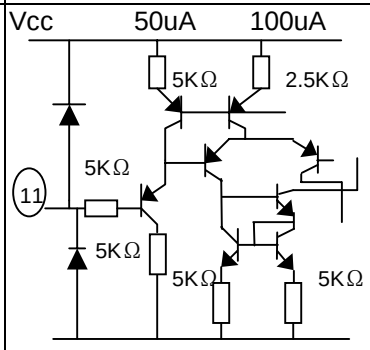
PIN CONFIGURATION

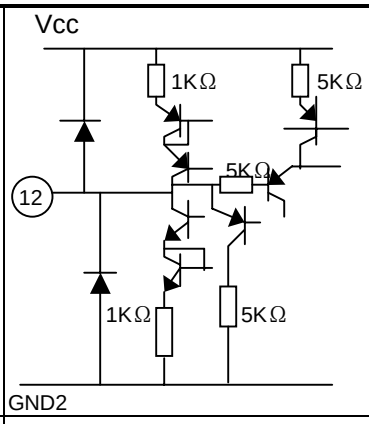
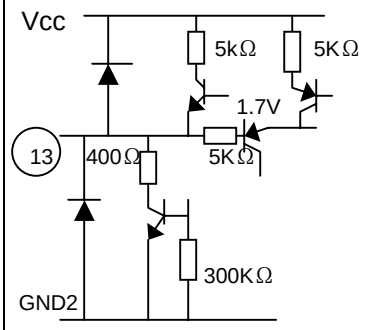
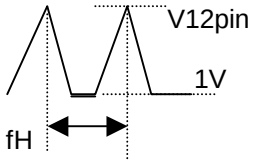
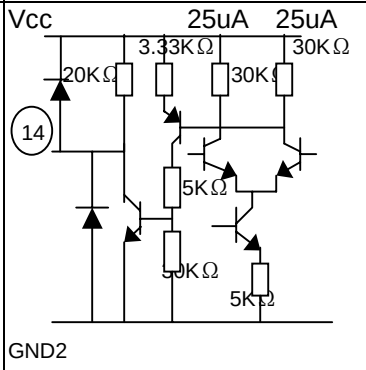
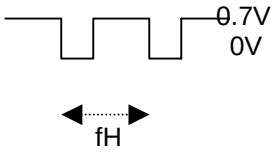
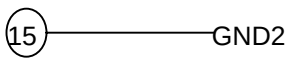
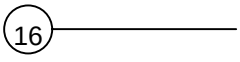


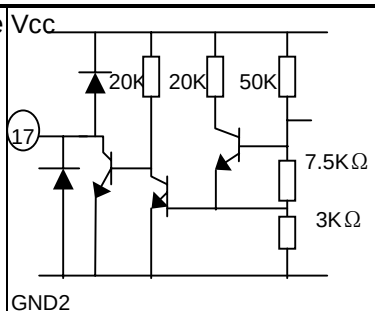
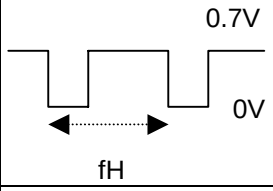
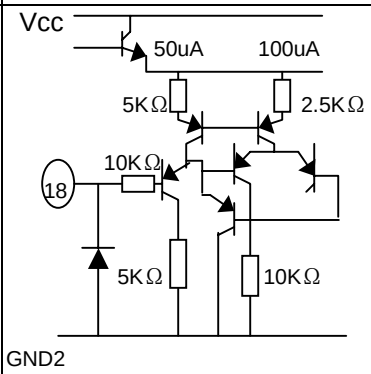
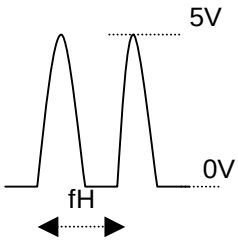
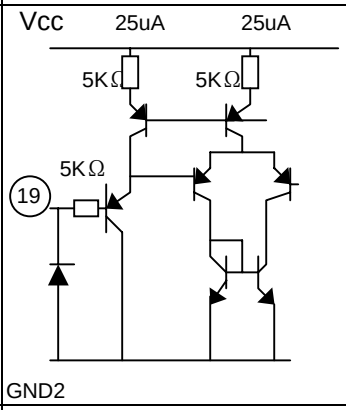
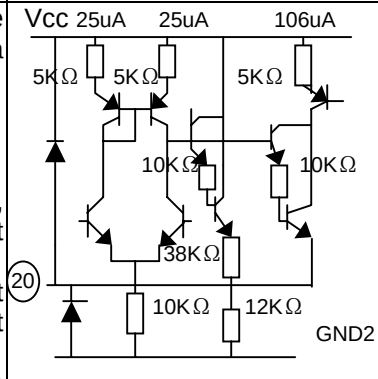
PIN DESCRIPTION

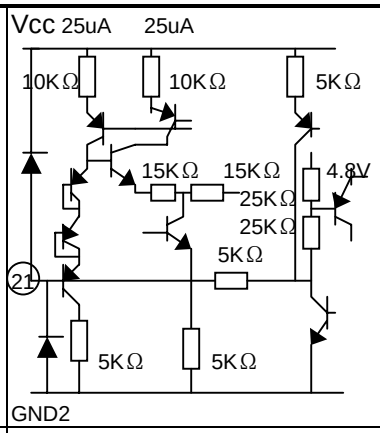
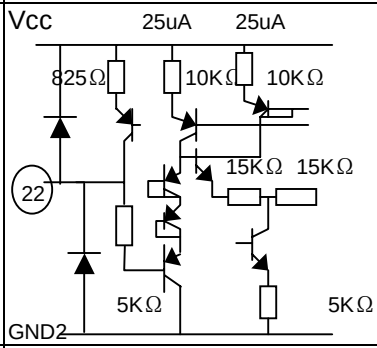
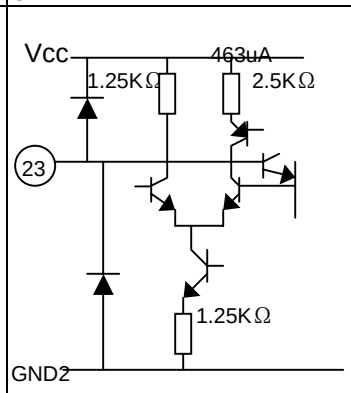
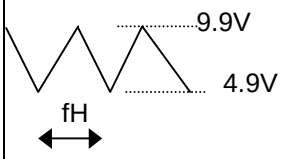
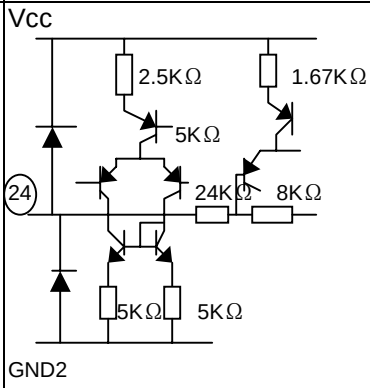
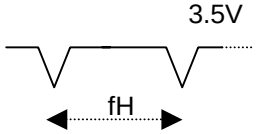
Pin No.	Pin Name	Description	Internal Equivalent Circuit	Wave Form
1	GND1	The main ground pin for the vertical circuit and the I ^{2} C bus circuit.		
2	VOSC	Connect the capacitor for oscillation of vertical saw wave. Please connect near pin, because series resistance component distorts Rising waveform of the vertical saw waveform. Use the capacitor of the small temperature drift.		
3	VAGC	Connect the capacitor for AGC of vertical saw Amplitude of vertical saw wave is held constant by the AGC circuit.		DC Voltage=3~4V

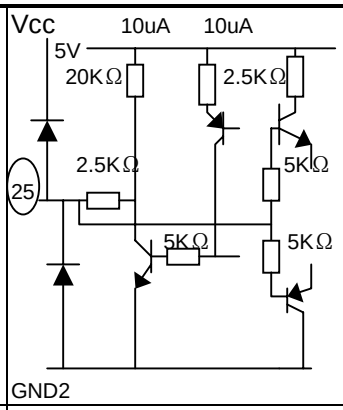
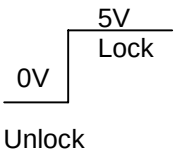
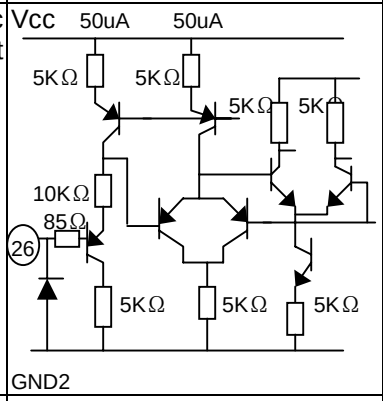
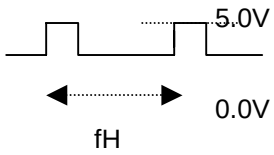
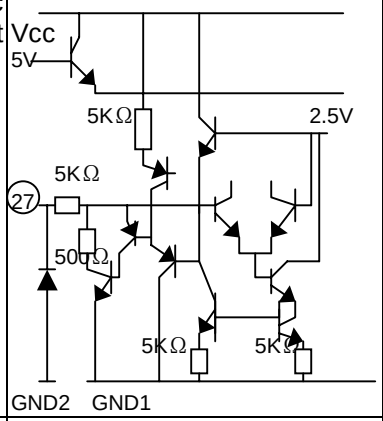
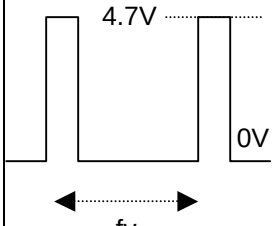
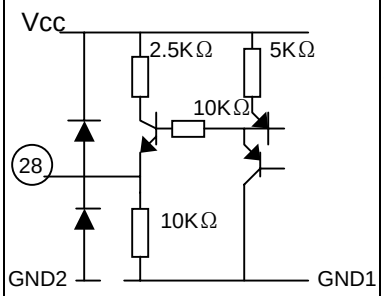
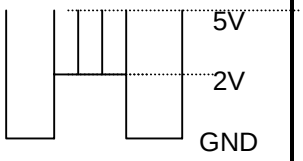
4	VSAWO	The vertical linearity S/C compensation are added to the vertical saw wave form		Refers the following picture image of correction 
5	EWO	Outputs the compensation signal of the trapezoid, the side pin, the side pin corner and the horizontal size.		Refers the following picture image of correction
6	VEI	Input the High voltage of the EHT. For, it cancel a transient response of the deflecting voltage. If this pin isn't used, connect 10uF capacitor to GND.	Vcc 25uA 370uA 	DC voltage=4V
7	HEI	Input the High voltage of the EHT. For, it cancel a transient response of the deflecting voltage. If this pin isn 't used, connect 10uFcapacitor to GND.	Vcc 	DC Voltage=4V

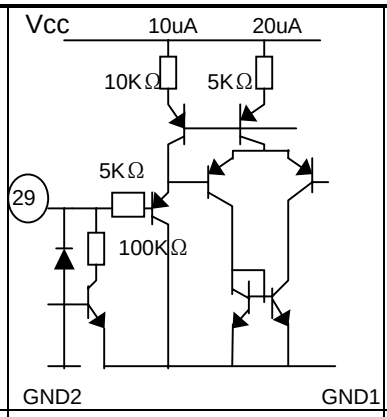
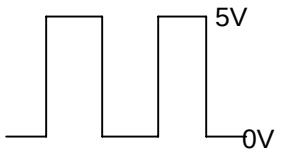
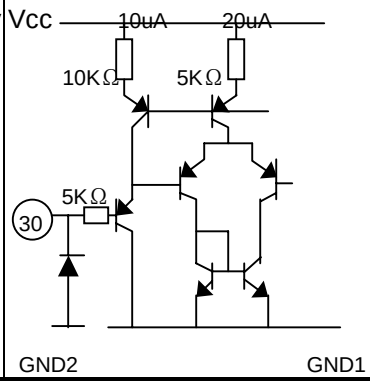
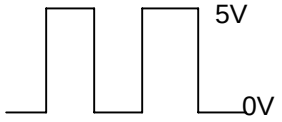
8	DFMIXO	Outputs the mixed signal of horizontal and vertical parabola wave for dynamic focus signal.		
9	HPHASE-CAP	Connect the capacitor 10 μF to GND		
10	HDSA	Connect the capacitor for oscillation of Horizontal dynamic focus signal.		DC Voltage=3~4V
11	BAMPI	The input of the error amplifier for the high voltage control.		DC Voltage

12	BAMPO	Outputs the voltage to control the PWM pulse width.		DC Voltage
13	PSAW	Connect the capacitor and the resistance for oscillation of PWM.		
14	PWMO	Outputs the PWM pulse Please connect the drive transistor, because it doesn't have an enough driving force.		
15	GND2	The main ground pin for the horizontal circuit.		
16	VCC	Input 12volts for the power supply.		DC voltage=12V

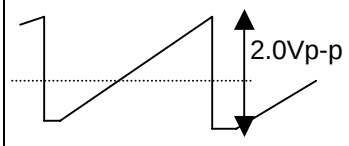
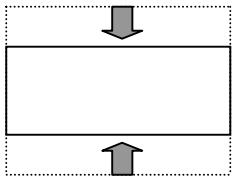
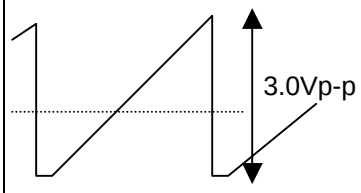
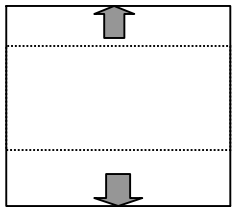
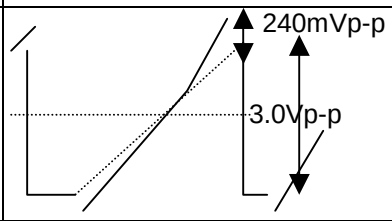
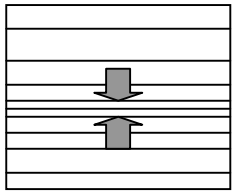
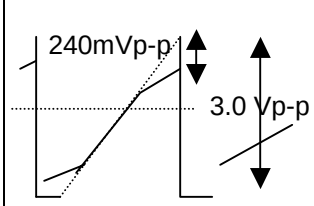
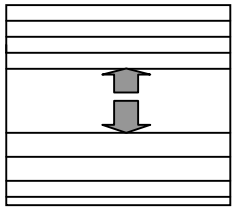
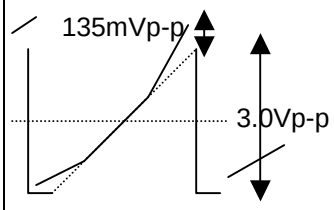
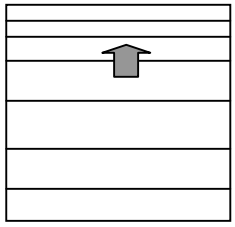
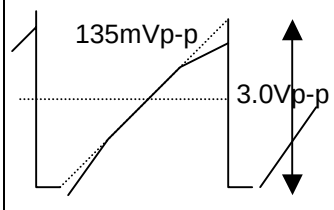
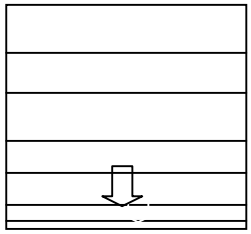
17	HOUT	Outputs the horizontal derive pulse		
18	FBP	Input the fly back pulse		
19	XRAY	The input pin for the X ray protection.		The bias voltage of the outside
20	VREF	Outputs the internal reference voltage, and creates a internal Reference current by the resistance. Please connect the resistor and Capacitor near this pin, because noise component input to this pin affects Horizontal jitter. A current control function is not provided, such that an External circuit cannot use the voltage output from this pin.		DC voltage=5V

21	HFVO	Outputs the voltage tracking to the horizontal frequency. Please connect the resistor and capacitor near this pin, because noise component input to this pin affects horizontal jitter		DC voltage tracking to the horizontal frequency
22	HFVR	Creates the current for the horizontal oscillator. Please connect this resistor near this pin, because noise component input to this pin affects horizontal jitter.		Same voltage that pin21
23	HOSC	Please connect the capacitor (390pF) for horizontal oscillation.		
24	HAFC	Creates the current for the horizontal oscillator. Please connect this resistor near this pin, because noise component input to this pin affects horizontal jitter. Please connect the capacitor (390pF) for horizontal oscillation. Connect the filter for the auto frequency control of horizontal. Following is the item that the filter affects jitter. The time constant of the filter The noise of the Vcc and GND. Connect resistor and capacitor near this pin.		

25	HLO	The lock detection output of the horizontal oscillator		DC voltage 
26	HIN	The separate horizontal sync signal input is a direct connection.		 separate sync
27	VIN	The separate Vertical sync signal input is a direct connection.		 separate sync
28	BLKO	Outputs the following 3 items by I^2C bus. The mixed signal of the vertical blanking pulse and the video clamp pulse. The vertical blanking pulse only. The video clamp pulse only.		Refers the following figure. 

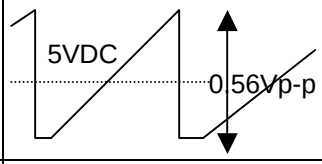
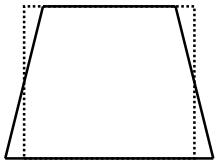
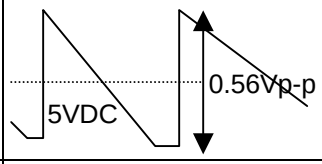
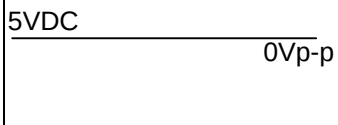
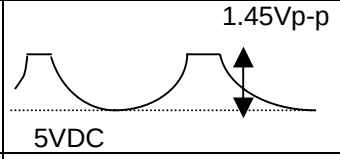
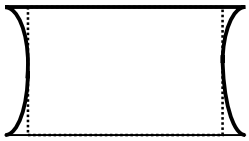
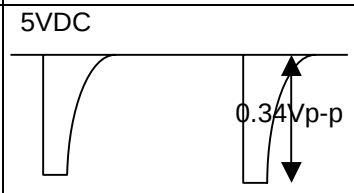
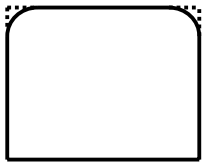
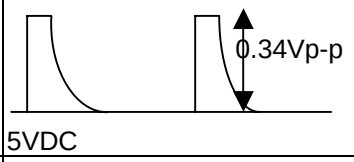
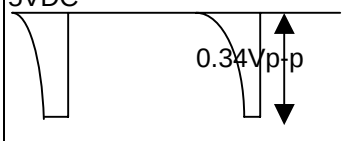
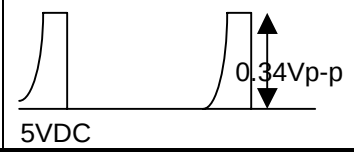
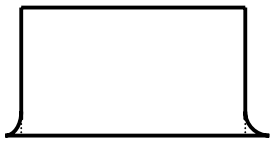
29	SDA	Input the serial data, and outputs the acknowledge of the I 2 C bus.		
30	SCL	Input the serial clock of I 2 C bus. The clock frequency corresponds to 400 KHZ		

Picture Image of Correction
Vertical Output Stage

Function	Output Pin	Control Sub Address	Control Condition	Output Wave form	Image
Vertical Size Correction	4	$0B_{HEX}$ D7~D0 (8bits)	00_{HEX}		
			FF_{HEX}		
Vertical Linearity S Correction	4	$0D_{HEX}$ D6~D0 (7bits)	01_{HEX}		
			$7F_{HEX}$		
Vertical Linearity C Correction	4	$0E_{HEX}$ D6~D0 (7bits)	01_{HEX}		
			$7F_{HEX}$		

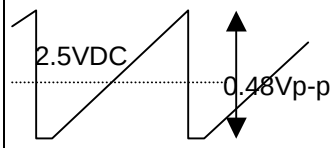
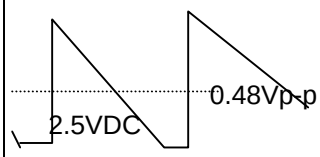
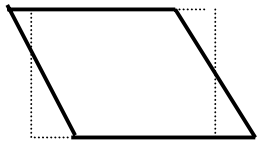
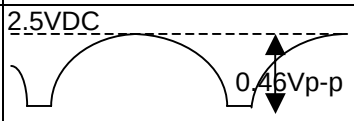
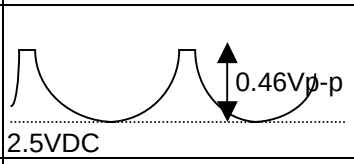
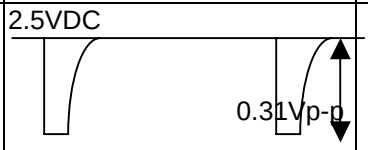
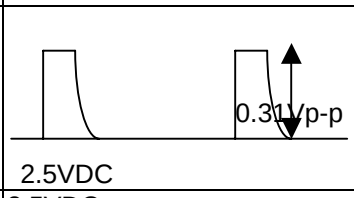
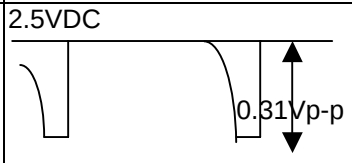
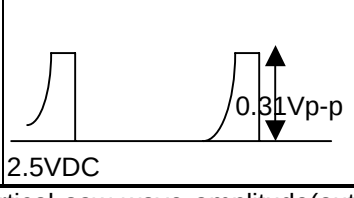
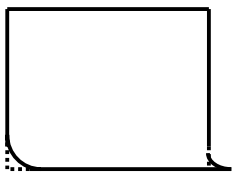
Notice: 1. The output amplitude depends on vertical saw wave amplitude("output amplitude" shows the wave form when the vertical saw wave is 3.0 Vp-p)
2. Vertical Linearity S or C corrections are OFF status when DAC value is 00H.

E/W Output Stage

Function	Output Pin	Control Sub Address	Control Condition	Inside Wave form	Image
Trapezoid Correction Control	5	$0A_{HEX}$ D6~D0 (7bits)	01_{HEX}		
			$7F_{HEX}$		
Side Pin Correction Control	5	09_{HEX} D6~D0 (7bits)	00_{HEX}		
			$7F_{HEX}$		
Side Pin Corner Top Correction Control	5	07_{HEX} D6~D0 (7bits)	00_{HEX}		
			$7F_{HEX}$		
Side Pin Corner Bottom Correction Control	5	08_{HEX} D6~D0 (7bits)	00_{HEX}		
			$7F_{HEX}$		

Notice1The output amplitude depends on vertical saw wave amplitude(output amplitude shows the waveform when the vertical is 3.0Vp-p.2. Trapezoid or side pin correction is OFF status when DAC value is 00H.3Side Pin Corner Top/Bottom is 0FF status when both DAC(SPCT and SPCB)value are 00H.

Horizontal Phase Stage

Function	Output Pin	Control Sub Address	Control Condition	Inside Wave form	Image
Parallelogram Correction Control	--	04_{HEX} D6~D0 (7bits)	01_{HEX}		
			$7F_{HEX}$		
Side Pin Balance Correction Control	--	03_{HEX} D6~D0 (7bits)	01_{HEX}		
			$7F_{HEX}$		
Side Pin Corner Balance Top Correct Control	--	05_{HEX} D6~D0 (7bits)	00_{HEX}		
			$7F_{HEX}$		
Side Pin Corner Balance Bottom Correction Control	--	06_{HEX} D6~D0 (7bits)	00_{HEX}		
			$7F_{HEX}$		

Notice: 1. The output amplitude depends on vertical saw wave amplitude(output amplitude shows the waveform when the vertical is 3.0Vp-p.

2. Trapezoid or side pin Balance correction is OFF status when DAC value is 00H.

3. Side Pin Corner Balance Top/Bottom are 0FF status when both DAC(SPCT and SPCB)value are 00H.

FUNCTIONAL DESCRIPTION

I 2 C Bus Interface

1. Serial Bus(I 2 C Bus)Interface

(1) I ^{2} C Bus Overview

The I ^{2} C bus is a dual bi-directional serial bus, developed by Philips. It is configured with two lines –a serial data line(SDA)and a serial clock line(SCL).

The WT9051 features a built-in I ^{2} C bus interface circuit,20 8-bit rewritable registers, and one 8-bit read-only register that is used for indicating the internal status of the IC and so on. These are used in write mode(slave receive)and read mode(slave transmit).

(2) Data Transmission Format

The transmission format features a sub address in write mode only. Data is configured in 8-bit units, after which an acknowledge bit must be appended. Note that data transmission is performed by transmitting the most significant bit(MSB)first.

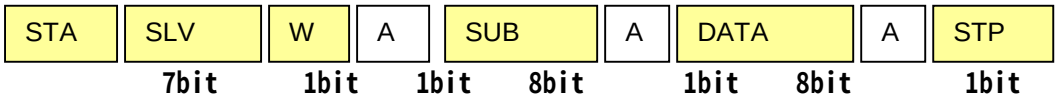
The data to be transmitted immediately after the issue of the start conditions is the slave address used to select the address of the WT9051.This address is configured using seven bits, with the remaining one bit being the data direction bit, used to set the direction of the subsequently transmitted data. Read involves transferring data from the WT9051 to the master device, while write involves transferring data from the master device to the WT9051.

Set 1 for read, or 0 for write. An example of the data transfer format is shown below.

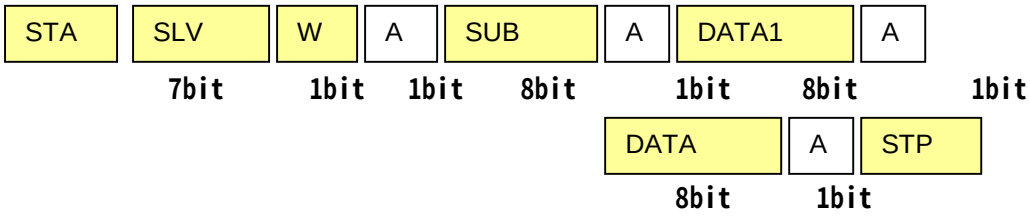
1.Write Mode(Slave Receive)

The slave address is read into the first byte, the sub address is read into the second byte, while the data can be read into the third and subsequent bytes. By using the sub address auto-increment function, data can be read out continuously.

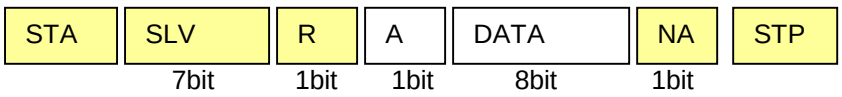
(A)1-byte transfer format



(B) Continuous byte transfer format



2.Read Mode(Slave Transmit)
The slave address is transmitted from the first byte and data is transmitted from the second and subsequent bytes. When no acknowledgement bit is received from the master device, release the SDA line. Do not return an acknowledge signal before issuing the stop conditions.



*Remarks
- STA :Start condition
- SLV :Slave address
- W/R :Data direction bit

W :Write mode (slave receive)
R :Read mode (salve transmit)
- Data :Data
- Sub :Sub address
- A/NA :Acknowledge bit

A :acknowledge
N :No acknowledge
STP :Stop condition

(3) V Period Transfer Mode

The WT9051 is provided with a switch (05H :D7)for setting whether rewriting DAC of the WT9051 is performed in free-run mode or in sync with the V-Sync signal.

- 05H :D7 =“0 ”→ Rewriting is performed in free-run mode.

Data is changed while the screen is being displayed, such that if the VSAW amplitude or position data is changed, horizontal noise lines will appear on the screen.

- 05H :D7 =“1 ”→ Rewriting is performed in sync with the V-Sync signal.

Data is changed in the BLK period, such that horizontal noise lines do not appear on the screen.
This technique can be used only to convert the following four items of vertical data.
1.Vertical size control (0BH : D7 to D0)
2.Vertical position control (0CH : D7 to D0)
3.Vertical S linearity (0DH : D6 to D0)
4.Vertical C linearity (0EH : D6 to D0)

*Note on data rewriting in V period transfer mode
When V period transfer mode is used, automatic increment cannot be used.
Only one item of data can be received for each 1V.The second and subsequent items of data are discarded until BLK is received again. When automatic increment is used, only one item of data

Address Table

1.Slave Address

Mode	D7	D6	D5	D4	D3	D2	D1	D0
White	1	0	0	0	1	1	0	0
Read	1	0	0	0	1	1	0	1

2. SUB ADDRESS

2-1 Write Mode <>: initial condition at power on reset

sub Address	D7	D6	D5	D4	D3	D2	D1	D0
00_{HEX}	X-ray Protector(XP) 0:normal <1:reset>	H OUT Control(HO) 0:exhibit 1:inhibit	PWN OUT Control(PO) 0:exhibit 1:inhibit	HORIZONTAL DUTY(HDUTY) <1>	<0>	<0>	<0>	<0>
01_{HEX}	Horizontal Size <HSIZE> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>
02_{HEX}	Horizontal Position<HPOSI> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>
03_{HEX}	V.BLK Width<VBW> <0:short> 1:long	SIDE PIN BALANCE <SPB> <1>	<0>	<0>	<0>	<0>	<0>	<0>
04_{HEX}	DF.OUT SELECT 0:SEP. <1:MIX>	PARALLELOGRAM <PARA> <1>	<0>	<0>	<0>	<0>	<0>	<0>
05_{HEX}	V.Period Transfer Mode <0:Off> 1:On	SIDE PIN CORNER BALANCE TOP <SPCBT) <1>	<0>	<0>	<0>	<0>	<0>	<0>
06_{HEX}	Unused <0>	SIDE PIN BALANCE BOTTOM(SPCBB) <1>	<0>	<0>	<0>	<0>	<0>	<0>
07_{HEX}	Clamp Pulse Position<CP> <0:Trailing> 1:Leading	SIDE OIN CORNER TOP<SPCT> <1>	<0>	<0>	<0>	<0>	<0>	<0>
08_{HEX}	V-BLKACI amp Select<BCI> <0:BLK+CLP> 1:Select2	SIDE PIN CORNER BOTTOM<SPCB> <1>	<0>	<0>	<0>	<0>	<0>	<0>
09_{HEX}	V-BLKA CIamp Select2<BC2> <0:BLK> 1:CLP	SIDE PIN<SP> <1>	<0>	<0>	<0>	<0>	<0>	<0>

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0A_{HEX}$	FHOSC Max. Frequency <0:100kHz> 1:150kHz	Trapezoid <TRAP> <1>	<0>	<0>	<0>	<0>	<0>	<0>
$0B_{HEX}$	Vertical Size <Vsize> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>
$0C_{HEX}$	Vertical Position <VPOSI> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>
$0D_{HEX}$	Unused <0>	Vertical Linearity S<VLS> <1>	<0>	<0>	<0>	<0>	<0>	<0>
$0E_{HEX}$	HEHT-fH Tracking EW-HSIZE	Vertical Linearity C<VLC> <1>	<0>	<0>	<0>	<0>	<0>	<0>
$0F_{HEX}$	Tracking <0:Track> 1:Unrack	Horizontal Moire cancellor <HMC> <0>	<0>	<0>	<0>	<0>	<0>	<0>
10_{HEX}	EW-fH Tracking 0:Untrack <1:Track>	Vertical Moire cancellor <VMC> <0>	<0>	<0>	<0>	<0>	<0>	<0>
11_{HEX}	HDF-HSIZE Tracking <0:Untrack> 1:Track	Horizontal Dynamic Focus Amplitude<HDFA> <1>	<0>	<0>	<0>	<0>	<0>	<0>
12_{HEX}	Unused <0>	Horizontal Dynamic Focus Phase<HDFP> <1>	<0>	<0>	<0>	<0>	<0>	<0>
13_{HEX}	Unused <0>	Vertical Dynamic Focus Amplitude<VDF> <1>	<0>	<0>	<0>	<0>	<0>	<0>

2-2 Read Mode

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
00_{HEX}	Unused <0>	Unused <0>	Unused <0>	Unused <0>	Unused <0>	Power On Reset 0:Power on 1:Power Off	H Lock Detector 0:Lock 1:Unlock	X-ray Detector 0:Undetct 1:Detect

Details of Each Sub Address

Those value in carets <>indicate the settings at a Power On Reset.

Write Mode

1.Sub address 00_H

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
00_{HEX}	X-ray Protector(XP) 0:Normal <1:Reset>	H OUT Control(HO) <0:Exhibit> 1:Inhibit	PWM OUT Control(PO) <0:Exhibit> 1:Inhibit	Horizontal DUTY <HDUTY> <1>	<0>	<0>	<0>	<0>

D7: X-ray protector
When the input of Pin19 is over 5V,X-ray protection circuit is active. So the output of the horizontal output signal(H-OUT)from Pin17 and the output of the PWM pulse (PWMO) from Pin14 disappear.

D6: H-OUT Control
Bit for controlling the output of the horizontal output signal (H-OUT) from Pin17.
When this bit is set to 0,output is possible. When this bit is set to 1,output is disabled.

D5: PWM OUT Control
Bit for controlling the output of the PWM pulse for high voltage control from Pin14.
When this bit is set to 0,output is possible. When this bit is set to 1,output is disabled.

D4 to D0: Horizontal DUTY (HDUTY)
Bit for controlling the duty of the horizontal output signal, output from Pin17.
The duty can be held to roughly will be large.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
01_{HEX}	Horizontal Size <HSIZE> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

D7 to D0: Horizontal Size (HSIZE)
Bit for controlling the horizontal size.
This data is used to modify the DC voltage of the waveform output from Pin5.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
02_{HEX}	Horizontal Position<HPOSI> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

D7 to D0: Horizontal Position (HPOSI) Bit for controlling the horizontal position. Based on this data, the horizontal oscillator signal (Pin17)for the horizontal sync input signal can be converted.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
03_{HEX}	V.BLK Width<VBW> <0:Short> 1:long	Side Pin Balance<SPB> <1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: V BLK Width
Bit for selecting the vertical blanking pulse width.
When this bit is set to 0, the width is short pulse width. When this bit is set to 1,the width is long pulse width.

D6 to D0: Side Pin Balance (SPB)
The amount of compensation for the side pin balance can be set using the seven bits from D6 to D0.The initial value is 40_{HEX} .The variable range is from 01_{HEX} to $7F_{HEX}$. When the value is 00_{HEX} Side Pin Balance correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
04_{HEX}	DF.OUT Select 0:sep. <1:Mix>	Parallelogram <PARA> <1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: DF.OUT Select
Bit for selecting the output of the parabola wave for dynamic focus signal from Pin8.
When this bit is set to 0,output the vertical dynamic focus signal from Pin8. When this bit is set to 1,output the mixed signal of the horizontal and vertical dynamic focus from Pin8.

D6 to D0: Parallelogram (PARA)
The amount of compensation for the horizontal square wave is set using the seven bits from D6 to D0.The initial value is 40_{HEX} the variable range is from 01_{HEX} to $7F_{HEX}$. When the value is 00_{HEX} Parallelogram correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
05_{HEX}	V Period Transfer Mode <0:Off> 1:On	Side Pin Corner Balance Top<SPCRT> <1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: V.Period Transfer Mode Bit for setting whether I 2 C-Bus write data transfer is performed in free-run mode or in sync with the V-Sync signal. When this bit is set to 0,data transfer is performed in free-run mode. When this bit is set to 1,data transfer is performed in sync with the V-Sync signal.

D6 to D0: Side Pin Corner Balance Top(SPCBT)The amount of compensation for the side pin corner balance top can be set using the seven bits from D6 to D0.The initial value is 40_{HEX} .The variable range is from 00_{HEX} to $7F_{HEX}$ .When this value and Side Pin Corner Balance Bottom DAC value is 00_{HEX} ,Side Pin Corner Balance Top correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
06_{HEX}	Unused	Side Pin Corner Balance Bottom<SPCBB>						
	<0>	<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: Unused
D6 to D0: Side Pin Corner Balance Bottom (SPCBB)
The amount of compensation for the side pin corner balance bottom can be set using the seven bits from D6 to D0. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX} and Side Pin Corner Balance Top DAC value is 00_{HEX}, Side Pin Corner Balance Bottom correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
07_{HEX}	Clamp Pulse Position<CP> <0:Trailing> 1:Leading	Side Pin Corner Top<SPCT>						
		<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: Clamp Pulse Position
Bit for tuning the clamp pulse signal output.
When this bit is set to 0, the clump pulse is output at the trailing edge of the horizontal sync input signal.
When this bit is set to 1, the clump pulse is output at the leading edge of the horizontal sync input signal.
D6 to D0: Side Pin Corner Top (SPCT)
The amount of compensation for the side pin corner top can be set using the seven bits from D6 to D0. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX} and Side Pin Corner Balance Top DAC value is 00_{HEX}, Side Pin Corner Top correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
08_{HEX}	V-BLK&Clamp Select1 (BC1) <0:BLK+CLP> 1: Select 2	Side Pin Corner Bottom<SPCB>						
		<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: V-BLK&Clamp Select1
Bit for selecting the output from Pin (BLKO)
When this bit is set to 0,the vertical blanking pulse and the clamp pulse are output.
When this bit is set to 1, this output depends on the bit D7 of the sub address"09"

D6 to D0: Side Pin Corner Bottom (SPCB)
The amount of compensation for the side pin corner bottom can be set using the seven bits from D6 to D0. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX} and Side Pin Corner Top DAC value is 00_{HEX}, Side Pin Corner bottom correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
09_{HEX}	V-BLK&Clamp Select2<BC2> (0: BLK) 1:CLP	Side Pin<SP> <0>	<0>	<0>	<0>	<0>	<0>	<0>

D7: V-BLK&Clamp Select2
Bit for selecting the output from Pin28 (BLKO)
When this bit is set to 0,the vertical blanking pulse is output
When this bit is set to 1, the clamp pulse is output.

D6 to D0: Side Pin (SP)
The amount of compensation for the side pin can be set using the seven bits from D6 to D0. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX}, Side Pin correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0A_{HEX}$	fH OSC Max Frequency <0:100kHz> 1:150kHz	Trapezoid <TRAP> <1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: fH OSC Max. Frequency
Bit for setting the maximum horizontal oscillation frequency.
When this bit is set to 0, the maximum oscillation frequency is 100kHz. When this bit is set to 1, the maximum oscillation frequency is 150kHz.

D6 to D0: Trapezoid (TRAP)
The amount of trapezoid is set using the seven bits from D6 to D0. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX}, Trapezoid correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0B_{HEX}$	Vertical Size <VSIZE> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

D7 to D0: Vertical Size (VSIZE)
Bit used for controlling the vertical size.
The input data is used to control the amplitude of the vertical sawtooth waveform output from Pin4. The initial value is 80_{HEX}. The variable range is from 00_{HEX} to FF_{HEX}.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0C_{HEX}$	Vertical Position <VPOSI> <1>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

D7 to D0: Vertical Position (VPOSI)
Bit for controlling the vertical position.
The Data is used to control the DC voltage of the vertical sawtooth waveform output from Pin4.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0D_{HEX}$	Unused	Vertical Linearity S<VLS>						
	<0>	<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: Unused
D6 to D0: Vertical Linearity S (VLS)
Bits D6 to D0 are used to set the amount of vertical S compensation.
The compensation signal is mixed with the vertical SAW waveform output from Pin4, then output. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX}, Vertical Linearity S correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0E_{HEX}$	HEHT-fH Tracking 0:Untrack <1:Track>	Vertical Linearity C<VLC>						
	<1>	<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: HEHT-fH Tracking
Bit for selecting whether HEHT gain is tracking to horizontal frequency or not. This function works on EW fH Tracking (10H:D7)=1 and this bit =1. If EW fH Tracking (10H:D7)=0, this function does not work.

D6 to D0: Vertical Linearity C (VLC)
Bits D6 to D0 are used to set the amount of vertical C compensation.
The compensation signal is mixed with the vertical SAW waveform output from Pin4, then output. The initial value is 40_{HEX}. The variable range is from 00_{HEX} to $7F_{HEX}$. When this value is 00_{HEX}, Vertical Linearity C correction is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
$0F_{HEX}$	EW-HSIZE Tracking <0:Track> 1:Untrack	Horizontal Moire Cancellor <HMC>						
	<0>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

D7: EW-HSIZE
Bit for selecting whether E/W output is tracking to HSIZE or not.
When this bit is set to 0, E/W output is tracking to HSIZE. When this bit is set to 1, E/W output is not tracking to HSIZE.
D6 to D0: Horizontal Moire Cancellor (HMR)
Bits D6 to D0 are used to set the compensation amount for H moiré cancel.
When the value is 00_{HEX}, horizontal Moire Cancellor is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
10_{HEX}	EW-fH Tracking 0:Untrack <1:Track>	Vertical Moire Cancellor <VMC>						
		<0>	<0>	<0>	<0>	<0>	<0>	<0>

D7: EW-fH Tracking
Bit for selecting whether E/W output is tracking to horizontal frequency or not.
When this bit is set to 0, E/W output is tracking to horizontal frequency. When this bit is set to 1, E/W output is not tracking to horizontal frequency.

D6 to D0: Vertical Moire Cancellor (VMC)
Bits D6 to D0 are used to set the compensation amount for V moiré cancel.
When the value is 00_{HEX}, Vertical Moire Cancellor is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
11_{HEX}	HDF-HSIZE Tracking <0:Untrack> 1:Track	Horizontal Dynamic Focus Amplitude<HDFA>						
		<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: HDF-HSIZE Tracking
Bit for selecting whether HDF output is tracking to HSIZE or not.
When this bit is set to 0, HDF output is tracking to HSIZE. When this bit is set to 1, HDF output is not tracking to HSIZE.

D6 to D0: Horizontal Dynamic Focus Amplitude (HDFA)
Bits D6 to D0 are used to set the amplitude of the dynamic focus parabola.
When the value is 00_{HEX}, Horizontal Dynamic Focus is OFF status.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
12_{HEX}	Unused	Horizontal Dynamic Focus Phase<HDFP>						
	<0>	<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: Unused
D6 to D0: Horizontal Dynamic Focus Phase (HDFP)
Bits D6 to D0 are used to set the amount of compensation for the dynamic focus phase.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
13_{HEX}	Unused	Vertical Dynamic Focus Amplitudes<VDF>						
	<0>	<1>	<0>	<0>	<0>	<0>	<0>	<0>

D7: Unused
D6 to D0: Vertical Dynamic Focus Amplitude (VDF)
Bits D6 to D0 are used to set the amplitude of the dynamic focus parabola.
When the value is 00_{HEX}, Vertical Dynamic Focus is OFF status.

Read Mode

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
00_{HEX}	Unused <0>	Unused <0>	Unused <0>	Unused <0>	Unused <0>	Power On Reset 0: Power on 1: Power off	H. Lock Detector 0: Lock 1: Unlock	X-ray Detector 0: Undetect 1: Detect

D7 to D3: Unused

D2: Power On Reset
Used to detect a power on reset. When a power on reset is applied, this bit is set to 1. Usually, set this bit to 0.Immediately after power-on, or if the power supply voltage ever drops below around 6.5V(low →high)or 6.2V(high →low),this bit is set to 1.After this bit has been set to 1, it should be cleared to 0 after two read cycles, provided the 12V power is applied normally. If, for example, the 12V power is not applied, no matter how many times read is performed, this bit will not be cleared to 0 and instead will remain set to 1.

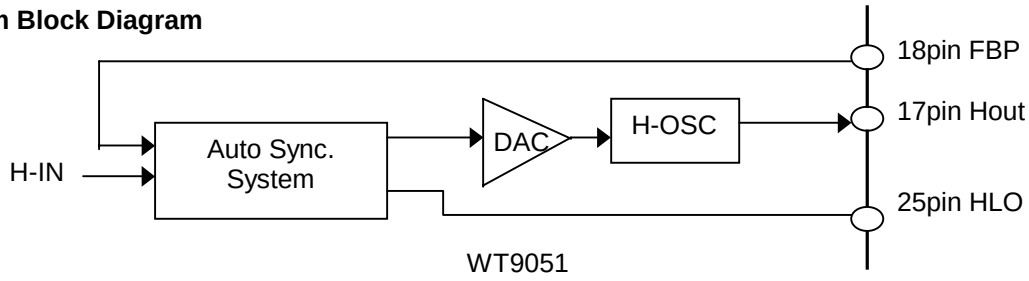
D1: H Lock Detector
Used to detect the Lock status of the horizontal sync signal and the oscillator output. In the lock status, this bit will be set to 0.In the unlock status, this bit will be set to 1.

D0: X-ray Detector
Used to detect the X-ray protection. When the X-ray protection circuit is active, this bit is set to 1.Usually, set this bit to 0.

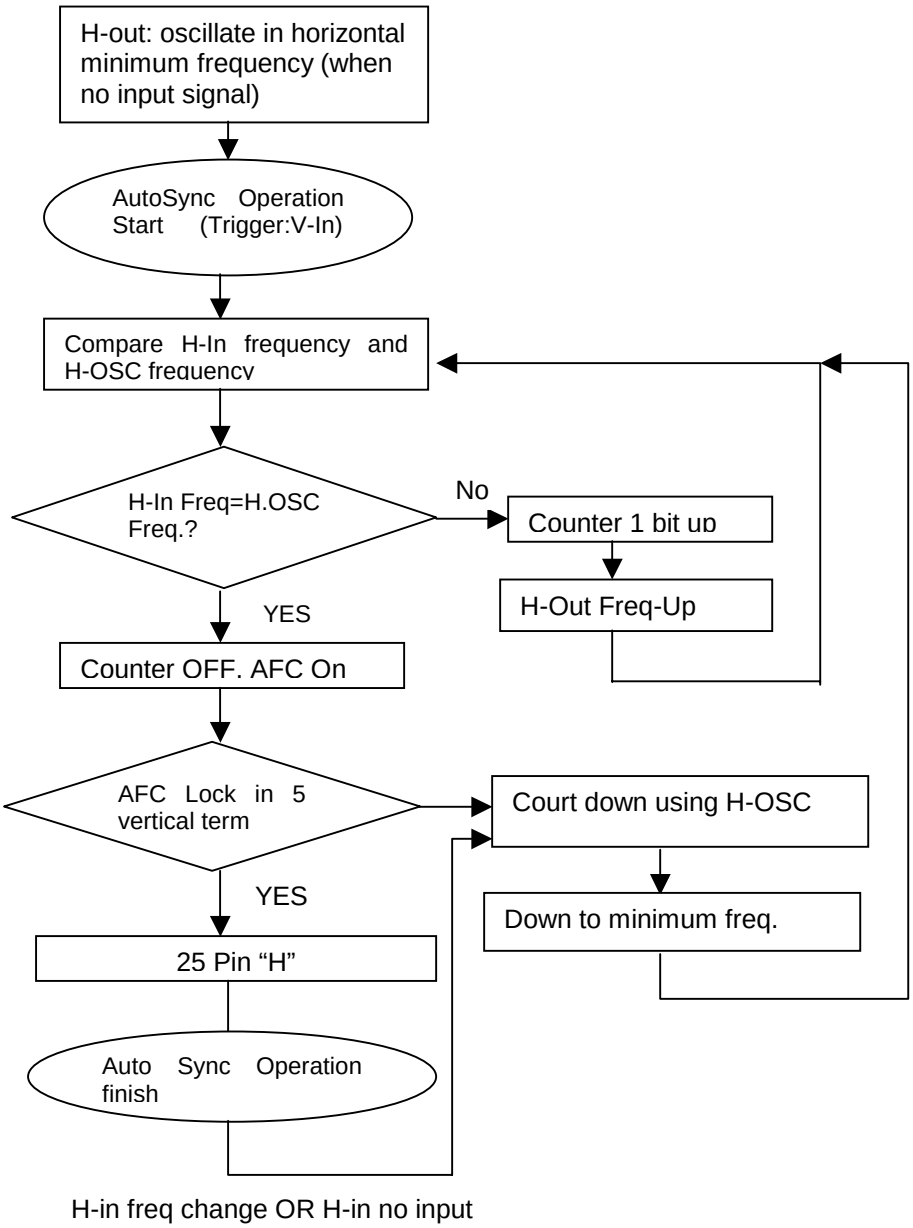
OPERATION DESCRIPTION

Automatic Sync. Processing System Sequence

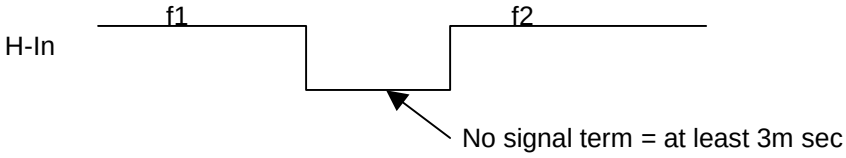
System Block Diagram



Processing Sequence



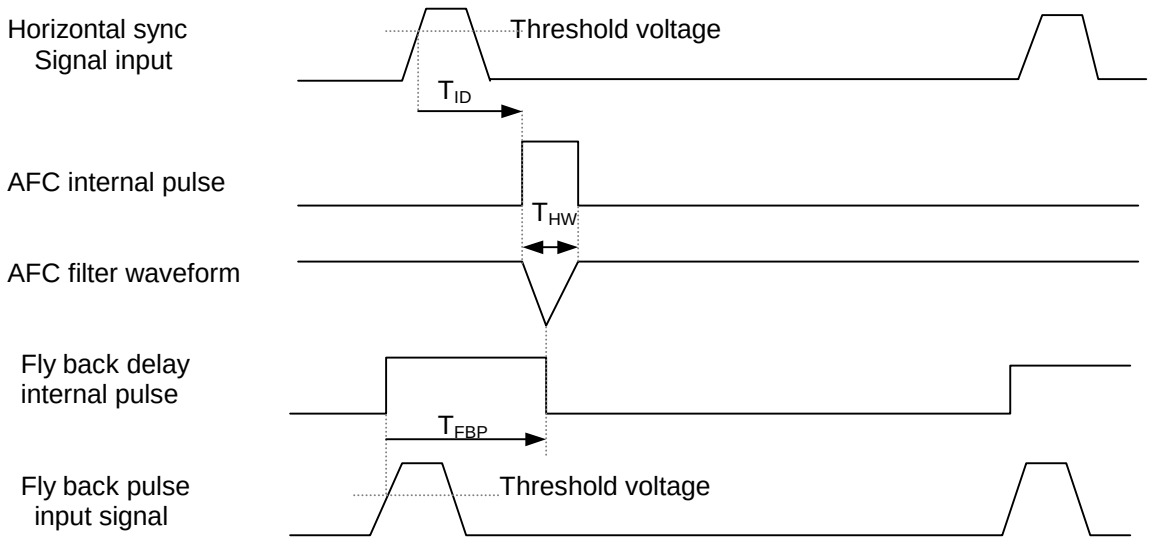
Notice
1) Automatic Sync. system can 't start count up operation without vertical sync signal input.
   The start trigger of count up operation is vertical sync signal input.
2) WT9051 oscillates in minimum free-run frequency during no signal status. Please input desirable frequency quasi-pulse from MCU to WT9051during no signal status.
3) Please input no signal term for at least 3m sec in changing frequency at any time (Please show in the following figure.).In the following figure,f1 and f2 means a horizontal input signal which corresponds to a mode or quasi-pulse signal from MCU.



TIMING CHART

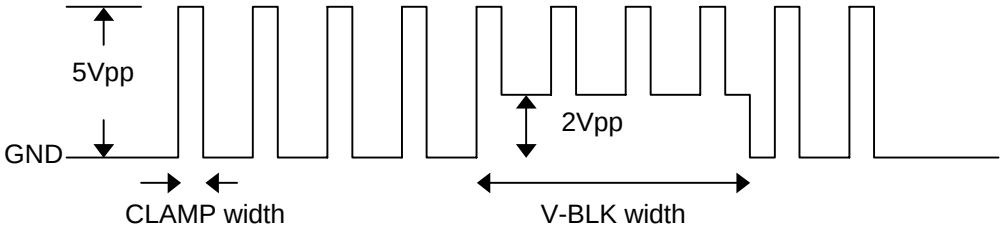
The timing of horizontal stage is set by ratio to horizontal frequency (fH).For example, if the delay time is 10 μs and fH is 30kHz,the ratio is 30%.

T_{ID} : I 2 C bus control this delay time.
The control range is form 16%to 43%.
T_{HW} : The pulse width of signal to the AFC.
This value is 10%.
T_{FBP} : This delay time is 30%from the rising edge of the fly back pulse.

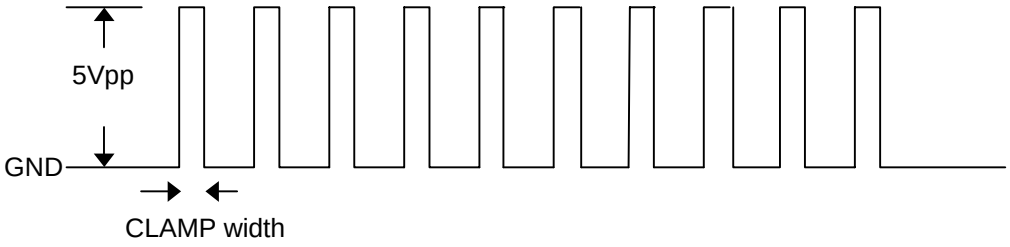


Vertical Blanking Pulse (V-BLK)and Video Clamp Pulse (CLAMP)Generator
The WT9051 has an on-chip circuit that generates vertical blanking pulse and clamp pulse.
The output signal mode must be selected by I 2 C bus. Figure illustrates the output signal. (WT9051) was selecting with outside the putting device. WT9051 was only mixed signal output. However, WT9051 can be simply selected with the bus.)
The vertical blanking pulse width must be selected by I 2 C bus. It is 288 μs (typical)or 335 μs (typical).The video clamp pulse width is 0.8 μs (typical). (Provided that 20pin resistor is set to 47K Ω.
The clamp pulse can choose the leading edge or the trailing edge of the horizontal sync by I2C BUS.

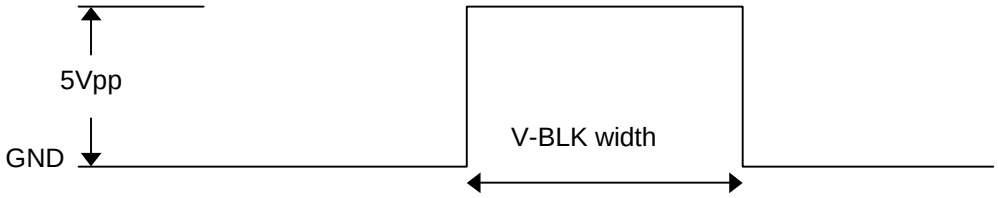
1. mixed signal output



2. clamp pulse (CLAMP) output



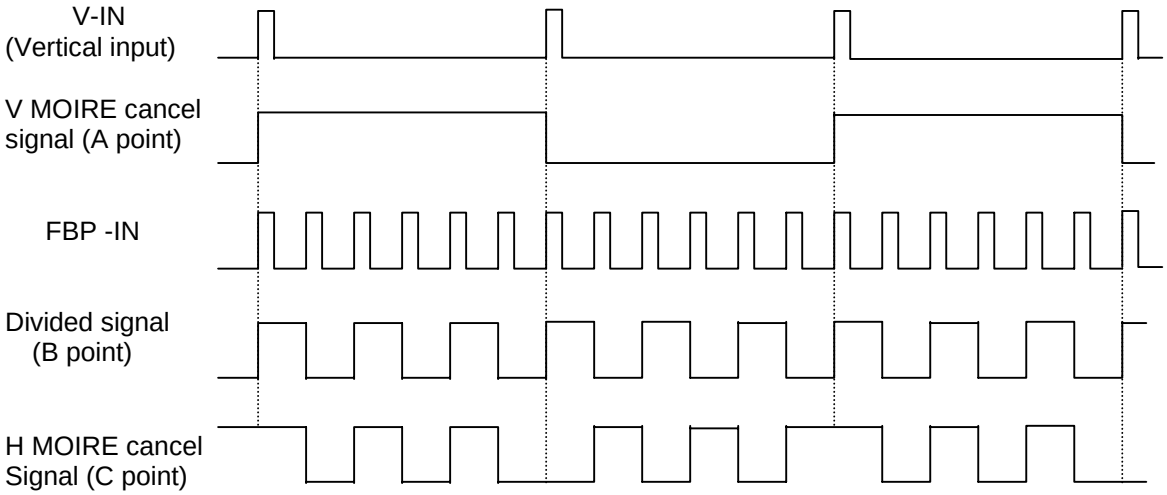
3. vertical blanking pulse (V-BLK) output

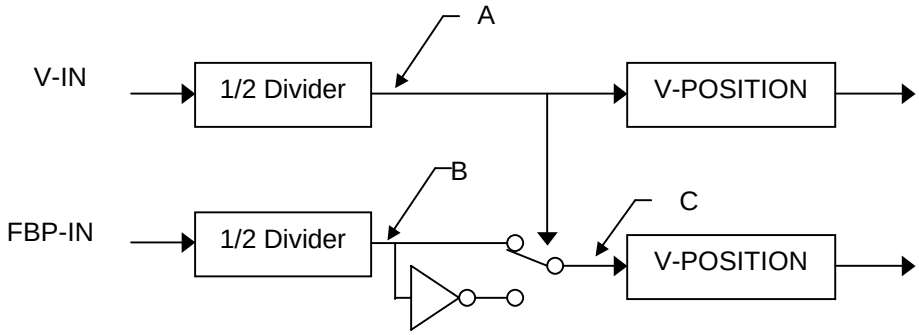


MOIRE Canceller

1. Vertical MOIRE canceller
   It divides V-IN.
   The MOIRE can be canceled when shifting a vertical position by this signal.
   The shift value can be controlled by I^2C bus.

2.Horizontal MOIRE canceller
   It divides FBP.
   And, it generates the signal, which reversed a phase every other vertical period.
   The MOIRE can be canceled when shifting a horizontal position by this signal.
   The shift value can be controlled by I^2C bus.





4.5 PWM for B+ control

The PWM Block consists of the error amplifier, and the flip-flop, the oscillator.

1. Error amplifier
   The error amplifier is the transconductance amplifier type. The non-inverting input is connected to the pin11.The non-inverting input is connected to the reference voltage (=2.5Volts). The output is connected to pin12 and the comparator, the clamp. The clamp limits the maximum output voltage to 5.0Volts.

2. Oscillator
   The external capacitor is charged by a external resistor. When the flip-flop is reset, it is discharged. The discharge is done until it becomes limit voltage (=1.0Volts).

3. Flip-Flop
   This flip-flop will be set at the rising edge of the H-OUT. When the charging voltage (pin13) of the condenser becomes equal to the output voltage (pin12)of the error amplifier, the output of the comparator resets a flip-flop.

4. Inhibit mode
   It doesn't output in the following case.
   - When the X-ray protection becomes active.
   - When lower than the voltage of Power On Reset.
   - When setting to off by I^2C Bus.

Tracking Specifications

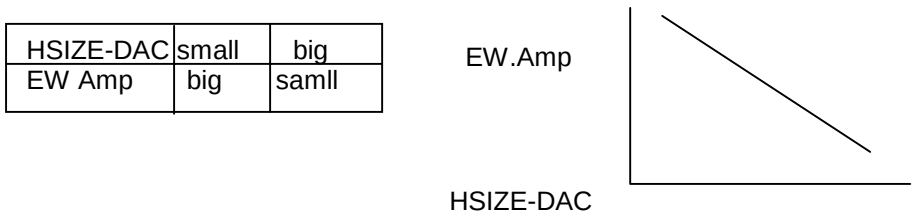
Tracking specifications of each waveform and function are shown in the following.

*) " ( ) " stands for ON/OFF switch for tracking function.

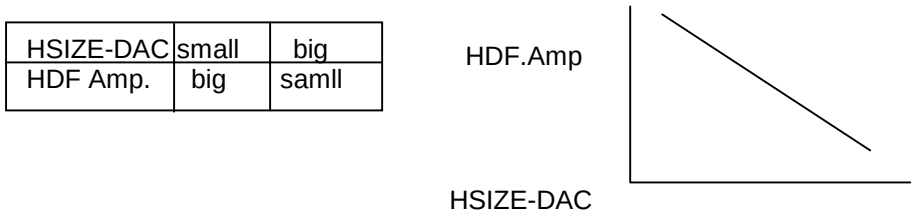
Waveform/Function	Tracking items
VSAW Amplitude	VSIZE, V-EHT
Vertical S-Linearity	VSIZE, VPOSI, V-EHT
Vertical C-Linearity	VSIZE, VPOSI, V-EHT
Trapezoid	VSIZE, VPOSI, V-EHT, HSIZE(0FH:D7), fH(10H:D7)
Side Pin	VSIZE, VPOSI, V-EHT, HSIZE(0FH:D7), fH(10H:D7)
Side Pin Corner Top	VSIZE, VPOSI, V-EHT, HSIZE(0FH:D7), fH(10H:D7)
Side Pin Corner Bottom	VSIZE, VPOSI, V-EHT, HSIZE(0FH:D7), fH(10H:D7)
Vertical Dynamic Focus	VSIZE, VPOSI, V-EHT
Horizontal Dynamic Focus	HSIZE(11H:D7)
EW DC	HSIZE, fH(10H:D7), H-EHT
V-EHT Gain	VSIZE
H-EHT Gain	FH(10H:D7)

Details of Tracking Specifications

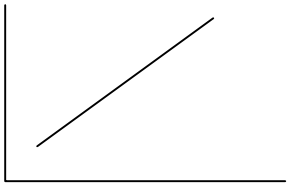
1.EW output tracking to HSIZE

1	HSIZE-DAC vs EW amplitude
	
2	On/Off Switch of this function
	Sub address 0FH:D7 "0": Track(Initial) "1":Untrack
3	Note
	When HSIZE-DAC is changed form FFH to 00H. EW amplitude becomes bigger 30%

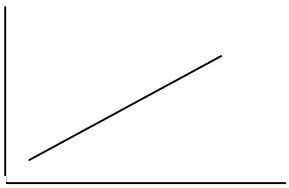
2.HDF output tracking to HSIZE

1	HSIZE-DAC vs. HDF amplitude
	
2	On/Off Switch of this function
	Sub address 11H:D7 "0": Track(Initial) "1":Untrack
3	Note
	When HSIZE-DAC is changed form FFH to 00H. HDF amplitude becomes bigger 70%

3. EW output tracking to horizontal frequency

1	Horizontal frequency vs. EW DC voltage
	<table><tr><td>FH</td><td>low</td><td>high</td></tr><tr><td>EW DC</td><td>low</td><td>high</td></tr></table> EW DC  fH
2	On/Off Switch of this function
	Sub address 10H:D7 "0": Untrack (Initial) "1":track
3	Note
	Formula for EW DC voltage EW DC=((fH/100k-1)x 0.325+1)x 5V

4. H-EHT Gain tracking to horizontal frequency

1	Horizontal frequency vs. Gain(=△EWO/△HEI)
	<table><tr><td>FH</td><td>low</td><td>high</td></tr><tr><td>Gain</td><td>small</td><td>big</td></tr></table> △ EWO/ △HEI  fH
2	On/Off Switch of this function
	Sub address 0FH:D7(only on the condition that the data of sub address 10H:D7 is "1" "1": Track (Initial) "0":Untrack

Electrical Characteristics

Absolute Maximum Ratings (Unless otherwise specified, Ta=25° C)

Parameter	Symbol	Condition	Rating	Unit
Power Supply	V_{CC}	Input Voltage of pin16	14	V
SDA Input Voltage	V_{SDA}	Input Voltage Range of pin29	-0.2~Vcc	V
SDA Output Sink Current	I_{SDA}	Output sink current of pin29	10	mA
SCL Input Voltage	V_{SCL}	Input Voltage Range of pin30	-0.2~Vcc	V
VSAW Output Source Current	I_{VSAWO}	Output Source Current of pin4	4.5	mA
VSAW Output Sink Current	I_{VSAWI}	Output Sink Current of pin4	4.5	mA
E/W Output Source Current	I_{EWO}	Output Source current of pin5	4.5	mA
VEI Input Voltage	V_{VEI}	Input Voltage Range of pin6	-0.2~Vcc	V
HEI Input Voltage	V_{HEI}	Input Voltage Range of pin7	-0.2~Vcc	V
BAMPI Input Voltage	V_{BAMPI}	Input Voltage Range of pin11	-0.2~Vcc	V
BAMPO Input Voltage	V_{BAPO}	Input Voltage Range of pin12	-0.2~Vcc	V
PWM Output Sink Current	I_{PWMI}	Output Sink Current of pin14	10	mA
V.DF Output Source Current	I_{VDF1}	Output Source Current of pin8	4.5	mA
H.DF Output Source Current	I_{HDF1}	Output Source Current of pin9	4.5	mA
Fly Back Pulse Input Voltage	V_{FBP}	Input Pulse Voltage Range of pin18	-0.2~Vcc	V
Horizontal Output Sink Current	I_{HOUTI}	Output Sink Current of pin17	10	mA
Horizontal Input Voltage	V_{HIN}	Input Pulse Voltage Range of pin26	-0.2~Vcc	V
Vertical Input Voltage	V_{VIN}	Input Pulse Voltage Range of pin27	-0.2~Vcc	V
BLK&CLP Output Source Current	I_{BLK}	Output Source Current of pin28	4.5	mA
Permissible package power dissipation	P_d	Ta=70。C, R_{TH}=55。C	1.0	W
Operating ambient temperature	T_a		-10~+75	。C
Storage temperature	T_{STG}		-40~+125	。C

Notice:
If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. In other words, absolute maximum ratings specify the values exceeding which the product may be physically damaged. Be sure to use the product with these ratings never exceeded. In addition, pins not listed in the above table must also be used in a range of 0 to Vcc .

RECOMMENDED OPERATING RANGE(Vcc=12V, Ta=25° C, Vcc=12V, unless otherwise noted)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	Pin16 input voltage	11.5	12.0	12.5	V
SDA Input Low Level	V_{SDAL}	Pin29 input low level	0	0	1.5	V
SDA Input High Level	V_{SDAH}	Pin29 input high level	2.3	5	5	V
SCL Input Low Level	V_{SCLL}	Pin30 input low level	0	0	1.5	V
SCL Input High Level	V_{SCLH}	Pin30 input high level	2.3	5	5	V
Horizontal Operating Frequency Range	F_H	Pin26 input frequency	30	-	150	KHz
Horizontal Input Duty Ratio1	D_{HIN1}	Pin26 input pulse duty ratio amplitude=5Vp-p input polarity: positive	-	-	20	%
Horizontal Input Duty Ratio2	D_{HIN2}	Pin26 input pulse duty ratio amplitude =5Vp-p input polarity: Negative	60	-	-	%
Vertical Operating Frequency Range	F_v	Pin27 Input Frequency	50	-	200	Hz
Vertical Input Pulse Width	W_{VIN1}	Pin27 Input Pulse duty ratio amplitude =5Vp-p Input Polarity: Positive	-	-	580	us

ELECTRONICAL CHARACTERICS(TA=25° C, Vcc=12V, unless otherwise noted)

<Common>

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Supply Current	I_{CC}	Supply current of pin16 no signal	60	69	81	mA
Reference Voltage	VREF	Pin20	4.5	5.0	5.5	V
Power on reset voltage1 (Low→High)	V_{PORH}	Input Vcc from 0V to 12V.Judged by existence of ACK	6.0	6.5	7.0	V
Power on Reset Voltage2 (High→Low)	V_{PORL}	Input level from 0V to 5V	5.7	6.2	6.7	V
SDA Input Threshold Voltage1	V_{SDA1}	Input level from 0V to 5V	1.7	2.0	2.3	V
SDA Input Threshold Voltage2	V_{SDA2}	Input level from 5V to 0V	1.4	1.7	2.0	V
SCL Input Threshold Voltage1	V_{SCL1}	Input level from 0V to 5V	1.7	2.0	2.3	V
SCL Input Threshold Voltage2	V_{SCL2}	Input level from 5V to 0V	1.4	1.7	2.0	V

<Horizontal sync signal processing Unit>

Horizontal Sync Input Block (measurement at Pin26(HIN)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Direct input Threshold Voltage	V_{HTH}	Input signal: separate sync direct input	0.4	0.6	0.8	V

H.IN Delay Block(measurement at Pin24 (HAFC))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
HIN Delay Variable 1	T_{HPD1}	HPOSI=00_{HEX}, Difference from pin26 to pin24. Ratio with period.fH=30kHz	11.5	15.5	19.4	%
HIN Delay Variable 2	T_{HPD2}	HPOSI=FF_{HEX}, Difference from pin26 to pin24. Ratio with period. fH=30kHz	33.6	40.0	46.4	%
HIN Delay Variable Amount1	T_{HPDA1}	(T_{HPD2}-T_{HPD1})/255 fH=30kHz	0.083	0.105	0.127	%/step
HIN Delay Variable 3	T_{HPD3}	HPOSI=00_{HEX}, Difference from pin26 to pin24. Ratio with period. fH=150kHz	14.3	17.5	20.7	%
HIN Delay Variable 4	T_{HPD4}	HPOSI=FF_{HEX}, Difference from pin26 to pin24. Ratio with period. fH=150kHz	36.3	42.0	47.7	%
HIN Delay Variable Amount 2	T_{HPDA2}	(T_{HPD4}-T_{HPD3})/255 fH=30kHz	0.079	0.100	0.121	%/step

H-WIDH BLOCK(measurement at pin24(HAFC))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
H-WIDTH Variable1	T_{HWD1}	F_H=30kHz	8.5	10.0	11.5	%
H-WIDTH Variable2	T_{HWD2}	F_H=150kHz	8.5	10.0	11.5	%

AFC BLOCK(measurement at pin24(HAFC))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Horizontal AFC Pull in Range1	AFC1	Positive Capture Range at F_H =30kHz	7.47	8.30	9.13	%
Horizontal AFC Pull in Range2	AFC2	Negative Capture Range at F_H =30kHz	-9.13	-8.30	-7.47	%
Horizontal AFC Pull in Range3	AFC3	Positive Capture Range at F_H =150kHz	7.65	8.50	9.35	%
Horizontal AFC Pull in Range4	AFC4	Negative Capture Range at F_H =150kHz	-9.35	-8.50	-7.65	%

FBP Delay Block(measurement at pin18(FBPIN) and pin24(HAFC))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
FBP Input Threshold Voltage1	V_{FBP1}	Input level from 0V to 5V	2.2	2.5	2.8	V
FBP Input Threshold Voltage 2	V_{FBP2}	Input level from 5V to 0V	1.9	2.2	2.5	V
FBP Delay	T_{FBP}	Difference from pin18 to pin24.Ratio with period	24.3	30	30	%

H-OSC Block(measurement at pin17(HOUT)) these value is excluding spread of external components

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
H.free-run frequency 1	F_{H01}	No input signal pin22 resistor=1.8KΩ	20.38	22.30	24.22	KHz
H.free-run frequency 2	F_{H02}	No input signal pin22 resistor=1.6KΩ	22.92	25.09	27.25	KHz
H-OSC frequency 1	F_{H01}	No input signal pin22 is 1V. Pin22 resistor=1.8KΩ	34.4	37.0	39.6	KHz
H-OSC frequency 2	F_{H02}	No input signal when pin22 resistor =1.8KΩ	135	145	155	KHz

H-Duty Block(measurement at pin17(HOUT))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
H-duty 1	H_{DUTY1}	HDUTY=00_{HEX} fH=30kHz	34.3	39.0	43.7	%
H-duty 2	H_{DUTY2}	HDUTY=10_{HEX} fH=30kHz	44.0	50.0	56.0	%
H-duty 3	H_{DUTY3}	HDUTY=$1F_{HEX}$ fH=30kHz	53.2	60.5	67.8	%
H-duty Amount1	H_{DUTYA1}	(H_{DUTY3}-H_{DUTY1})/31 fH=30kHz	0.590	0.694	0.798	%/step
H-duty 4	H_{DUTY4}	HDUTY=00_{HEX} fH=150kHz	34.3	39.0	43.7	%
H-duty 5	H_{DUTY5}	HDUTY=10_{HEX} fH=150kHz	44.0	50.0	56.0	%
H-duty 6	H_{DUTY6}	HDUTY=$1F_{HEX}$ fH=150kHz	53.2	60.5	67.8	%
H-duty Amount 2	H_{DUTYA2}	(H_{DUTY6}-H_{DUTY4})/31 fH=150kHz	0.590	0.694	0.798	%/step

H-Out Block(measurement at collector of transistor attached at pin17)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
H-Out Low Level	V_{HOL}	Pull up resistor 20KΩ Difference from GND Level	0	0.2	0.3	V
H-Out High Level	V_{HOH}	Pull up resistor 20KΩ Difference from Vcc Level	-0.2	0	0	V

<Vertical sync signal processing Unit>

Vertical Input Block (measurement at pin27(VIN))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Vertical Input Threshold Voltage	V_{VIN}	Threshold voltage of pin27	2.2	2.5	2.8	V

V Position Block (measurement at pin4(VSAWO))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Vertical Position1	V_{P01}	VPOSI=00_H	2.962	3.153	3.348	V
Vertical Position2	V_{P02}	VPOSI=$7F_H$	3.325	3.500	3.675	V
Vertical Position3	V_{P03}	VPOSI=FF_H	3.620	3.847	4.076	V
Vertical Position Amount	V_{P0A}	(VP_{03}-VP_{01})/255	2.32	2.72	3.15	mV/step

V-SAW Block measurement at pin4(VSAWO))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Vertical Saw wave Amplitude 1	V_{SAW1}	VSIZE=00_H	1.65	2.0	2.35	V_{P-P}
Vertical Saw wave Amplitude 2	V_{SAW2}	VSIZE=FF_H	2.65	3.0	3.35	V_{P-P}
Vertical Saw wave Amplitude Amount	V_{SAW}	V_{SAW1}- V_{SAW2} /255	3.27	3.94	4.61	mV/step
V.free-run frequency	F_{V0}	No input signal	10	25	40	Hz
V.free-run Amplitude	V_{SAW0}	No input signal	3.2	3.6	4.0	V

<V-BLK/CLAMP Pulse unit>

V-BLK/CLAMP Pulse (measurement at pin28)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Vertical Blanking Pulse Width1	T_{BLK1}	VBW=0, 20pin Resistor=47kΩ	225	265	305	us
Vertical Blanking Pulse Width2	T_{BLK2}	VBW=1, 20pin Resistor=47kΩ	260	305	350	us
Vertical Blanking Pulse Amplitude	V_{BLK}		4.5	5.0	5.5	V_{P-P}
Video Clamp Pulse Width	T_{CLP}	20pin Resistor=47kΩ	0.4	0.6	0.8	us
Video Clamp Pulse Amplitude	V_{CLP}		4.5	5.0	5.5	V_{P-P}

<Correction Unit>

Vertical Linearity "s" Correction Block(measurement at pin4(VSAWO), (notice1, 2)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Vertical Linearity"S" Correction Amplitude1	V_{S1}	VLS=$01_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at top part	-370	-240	-110	mV
Vertical Linearity"S" Correction Amplitude2	V_{S2}	VLS=$01_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at bottom part	110	240	370	mV
Vertical Linearity"S" Correction Amplitude3	V_{S3}	VLS=$40_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at top part	-70	0	70	mV
Vertical Linearity"S" Correction Amplitude4	V_{S4}	VLS=$40_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at bottom part	-70	0	70	mV
Vertical Linearity"S" Correction Amplitude5	V_{S5}	VLS=$7F_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at top part	110	240	370	mV
Vertical Linearity"S" Correction Amplitude6	V_{S6}	VLS=$7F_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at bottom part	-370	-240	-110	mV
Vertical Linearity"S" Correction Amount	V_S	(V_{S5}-V_{S1})/126	2.39	3.81	5.23	mV/step

Vertical Linearity"C" Correction Block(measurement at pin4(VSAWO), (notice1, 3))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Vertical Linearity"C" Correction Amplitude1	V_{C1}	VLC=$01_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at top part	60	135	210	mV
Vertical Linearity"C" Correction Amplitude1	V_{C2}	VLC=$01_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at bottom part	60	135	210	mV
Vertical Linearity"C" Correction Amplitude2	V_{C3}	VLC=$40_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at top part	-100	0	100	mV
Vertical Linearity"C" Correction Amplitude2	V_{C4}	VLC=$40_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at bottom part	-100	0	100	mV
Vertical Linearity"C" Correction Amplitude3	V_{C5}	VLC=$7F_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at top part	-210	-135	-60	mV
Vertical Linearity"C" Correction Amplitude3	V_{C6}	VLC=$7F_{HEX,}$ VSIZE=FF_{HEX} Difference from V_{POC} at bottom part	-210	-135	-60	mV
Vertical Linearity"C" Correction Amount	V_C	$(V_{C5}-V_{C1})/126$	1.55	2.14	2.75	mV/step

H-Size Control Block(measurement at Pin5(EWO), (notice4, 5, 6)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
E/W Output DC Voltage1	V_{EW1}	HSIZE=$00_{H,}$ fH-track=off	3.15	3.5	3.85	V
E/W Output DC Voltage2	V_{EW2}	HSIZE=$7F_{H,}$ fH-track=off	3.83	4.25	4.68	V
E/W Output DC Voltage3	V_{EW3}	HSIZE=$FF_{H,}$ fH-track=off	4.5	5.0	5.5	V
E/W Output DC Voltage Amount	V_{EW}	$(V_{EW3-}\ V_{EW1)}/255$	5.31	5.91	6.51	mV/step
E/W Output DC Voltage4	V_{EW4}	HSIZE=$FF_{H,}$ fH=30k	3.40	3.86	4.32	V
E/W Output DC Voltage5	V_{EW5}	HSIZE=$FF_{H,}$ fH=150k	5.11	5.81	6.51	V

Trapezoid Correction Block(measurement at pin5(EWO), (notice5, 6)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Trapezoid Correction Amplitude1	V_{TRA1}	TRAP=01_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-350	-280	-210	mV
Trapezoid Correction Amplitude2	V_{TRA2}	TRAP=01_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	210	280	350	mV
Trapezoid Correction Amplitude3	V_{TRA3}	TRAP=40_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-50	0	50	mV
Trapezoid Correction Amplitude4	V_{TRA4}	TRAP=$40F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-50	0	50	mV
Trapezoid Correction Amplitude5	V_{TRA5}	TRAP=$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	210	280	350	mV
Trapezoid Correction Amplitude6	V_{TRA6}	TRAP=$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-350	-280	-210	mV
Trapezoid Correction Amplitude Amount	V_{TRA}	$V_{TRA5-}\ V_{TRA1}/126$	3.55	4.44	5.33	mV/step
Trapezoid Correction Amplitude7	V_{TRA7}	V_{TRA5} , HSIZE=FF_H, fH=30k	175	235	295	mV
Trapezoid Correction Amplitude8	V_{TRA8}	V_{TRA5} , HSIZE=FF_H, fH=150k	256	344	432	mV
Trapezoid Correction Amplitude9	V_{TRA9}	V_{TRA5} , HSIZE=FF_H, fH-track=off	273	364	455	mV

Side Pin Correction Block (measurement at pin5(EWO), (notice4, 6)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Side Pin Correction Amplitude1	V_{SP1}	SP=01_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-120	0	120	mV
Side Pin Correction Amplitude2	V_{SP2}	SP=01_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-120	0	120	mV
Side Pin Correction Amplitude3	V_{SP3}	SP=40_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	430	725	1020	mV
Side Pin Correction Amplitude4	V_{SP4}	SP=$40F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	430	725	1020	mV
Side Pin Correction Amplitude5	V_{SP5}	SP=$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	1025	1450	1875	mV
Side Pin Correction Amplitude6	V_{SP6}	SP=$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	1025	1450	1875	mV
Side Pin Correction Amplitude Amount	V_{SP}	V_{SP5-} V_{SP1} /126	9.21	11.51	13.81	mV/step
Side Pin Correction Amplitude7	V_{SP7}	V_{SP5} , HSIZE=FF_H, fH=30k	844	1215	1586	mV
Side Pin Correction Amplitude8	V_{TSP8}	V_{SP5} , HSIZE=FF_H, fH=150k	1237	1780	2323	mV
Side Pin Correction Amplitude9	V_{SP9}	V_{SP5} , HSIZE=FF_H, fH-track=off	1320	1885	2451	mV

Side Pin Corner "Top" Correct Block (measurement at Pin5(EWO), (notice4, 5, 8)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
SPC-T Correction Amplitude1	V_{SPCT1}	SPCT=00_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-480	-340	-200	mV
SPC-T Correction Amplitude2	V_{SPCT2}	SPCT=00_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-80	0	80	mV
SPC-T Correction Amplitude3	V_{SPCT3}	SPCT =40_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-80	0	80	mV
SPC-T Correction Amplitude4	V_{SPCT4}	SPCT =$40F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-80	0	80	mV
SPC-T Correction Amplitude5	V_{SPCT5}	SPCT =$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	200	340	480	mV
SPC-T Correction Amplitude6	V_{SPCT6}	SPCT =$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-80	0	80	mV
SPC-T Correction Amplitude Amount	V_{SPCT}	V_{SPCT5-} V_{SPCT1} /127	3.17	5.40	7.62	mV/step
SPC-T Correction Amplitude7	V_{SPCT7}	$V_{SPCT\,5}$, HSIZE=FF_H, fH=30k	165	285	405	mV
SPC-T Correction Amplitude8	V_{SPCT8}	$V_{SPCT\,5}$, HSIZE=FF_H, fH=150k	242	417	592	mV
SPC-T Correction Amplitude9	V_{SPCT9}	$V_{SPCT\,5}$, HSIZE=00_H, fH-track=off	256	442	628	mV

Side Pin Corner "BOTTOM" Correct Block (measurement at Pin5(EWO), (notice4, 5, 8)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
SPC-B Correction Amplitude1	V_{SPCB1}	SPCB=00_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-80	0	80	mV
SPC-B Correction Amplitude2	V_{SPCB2}	SPCB=00_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-480	-340	-200	mV
SPC-B Correction Amplitude3	V_{SPCB3}	SPCB =40_H , VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-80	0	80	mV
SPC-B Correction Amplitude4	V_{SPCB4}	SPCB =$40F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	-80	0	80	mV
SPC-B Correction Amplitude5	V_{SPCB5}	SPCB =$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at top part, fH-track=off	-80	0	80	mV
SPC-B Correction Amplitude6	V_{SPCB6}	SPCB =$7F_H$, VSIZE= $FF_{H,}$ HSIZE= $FF_{H,}$ Difference from V_{EW3} at bottom part, fH-track=off	200	340	480	mV
SPC-B Correction Amplitude Amount	V_{SPCB}	V_{SPCB6-} V_{SPCB2} /127	3.17	5.40	7.62	mV/step
SPC-B Correction Amplitude7	V_{SPCB7}	$V_{SPCB\ 6}$, HSIZE=FF_H, fH=30k	165	285	405	mV
SPC-B Correction Amplitude8	V_{SPCB8}	V_{SPCB6} , HSIZE=FF_H, fH=150k	242	417	592	mV
SPC-B Correction Amplitude9	V_{SPCB9}	V_{SPCB6} , HSIZE=FF_H, fH-track=off	256	442	628	mV

Parallelogram Correction Block (internal measurement, (notice 10,11))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Parallelogram Correction Amplitude1	V_{PARA1}	PARA=01_H , Top part	-300	-240	-180	mV
Parallelogram Correction Amplitude2	V_{PARA2}	PARA=01_H , Bottom part	180	240	300	mV
Parallelogram Correction Amplitude3	V_{PARA3}	PARA =40_H , Top part	-45	0	45	mV
Parallelogram Correction Amplitude4	V_{PARA4}	PARA=40_H , Bottom part	-45	0	45	mV
Parallelogram Correction Amplitude5	V_{PARA5}	PARA =$7F_H$, Top part	180	240	300	mV
Parallelogram Correction Amplitude6	V_{PARA6}	PARA=$7F_H$, Bottom part	-300	-240	-180	mV
Parallelogram Correction Amount	V_{PARA}	T_{PARA5-} T_{PARA1} /126	3.04	3.81	4.58	mV/step

Side Pin Balance Correct Block (internal measurement, (notice9, 11))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
SPB Correction Amplitude1	V_{SPB1}	SPB=01_H , Top part	-600	-460	-320	mV
SPB Correction Amplitude2	V_{SPB2}	SPB=01_H , Bottom part	-600	-460	-320	mV
SPB Correction Amplitude3	V_{SPB3}	SPB =40_H , Top part	-120	0	120	mV
SPB Correction Amplitude4	V_{SPB4}	SPB=40_H , Bottom part	-120	0	120	mV
SPB Correction Amplitude5	V_{SPB5}	SPB =$7F_H$, Top part	320	460	600	mV
SPB Correction Amplitude6	V_{SPB6}	SPB=$7F_H$, Bottom part	320	460	600	mV
SPB Correction Amount	V_{SPB}	T_{PARA5-} T_{PARA1}/126	5.84	7.30	8.76	mV/step

Side Pin Corner Balance Top Correction Block(internal measurement, (notice9,10, 13))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
SPCB-T Correction Amplitude1	V_{SPCBT1}	SPCBT=00_H , Top part	-410	-310	-210	mV
SPCB-T Correction Amplitude2	V_{SPCBT2}	SPCBT=00_H , Bottom part	-80	0	80	mV
SPCB-T Correction Amplitude3	V_{SPCBT3}	SPCBT =40_H , Top part	-80	0	80	mV
SPCB-T Correction Amplitude4	V_{SPCBT4}	SPCBT=40_H , Bottom part	-80	0	80	mV
SPCB-T Correction Amplitude5	V_{SPCBT5}	SPCBT =$7F_H$, Top part	210	310	410	mV
SPCB-T Correction Amplitude6	V_{SPCBT6}	SPCBT=$7F_H$, Bottom part	-80	0	80	mV
SPCB-T Correction Amount	V_{SPCBT}	$V_{SPCBT5-}$ V_{SPCBT1}/127	3.33	4.92	6.51	mV/step

Side Pin Corner Balance Bottom Correction Block(internal measurement, (notice9,10, 12))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
SPCB-B Correction Amplitude1	V_{SPCBB1}	SPCBB=00_H , Top part	-80	0	80	mV
SPCB- B Correction Amplitude2	V_{SPCBB2}	SPCBB=00_H , Bottom part	210	310	410	mV
SPCB- B Correction Amplitude3	V_{SPCBB3}	SPCBB =40_H , Top part	-80	0	80	mV
SPCB- B Correction Amplitude4	V_{SPCBB4}	SPCBB=40_H , Bottom part	-80	0	80	mV
SPCB- B Correction Amplitude5	V_{SPCBB5}	SPCBB =$7F_H$, Top part	-80	0	80	mV
SPCB-B Correction Amplitude6	V_{SPCBB6}	SPCBB=$7F_H$, Bottom part	-410	-310	-210	mV
SPCB- B Correction Amount	V_{SPCBB}	$V_{SPCBB5-}$ V_{SPCBB1}/127	3.33	4.92	6.51	mV/step

<EHT Unit>

H-EHT Block(measurement at pin5(EW))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
7pinOpen Voltage	V_{7PIN}		3.6	4.0	4.4	V
Input Minimum D-Range	V_{LEHTH}	Minimum input voltage	-	-	2.2	V
Input Maximum D-Range	V_{HEHTH}	Maximum input voltage	4.77	-	-	V
EHT-H Correction Gain1	G_{EHTH1}	Between EWO to EHTH gain FH- tracking =off	-1.06	-0.88	-0.70	Times
EHT-H Correction Gain2	G_{EHTH2}	$G_{EHTH1,}$ fH=30k	-0.28	-0.20	-0.12	Times
EHT-H Correction Gain3	G_{EHTH3}	$G_{EHTH1,}$ fH=150k	-1.70	-1.42	-1.14	Times

V-EHT Block (measurement at pin4(VSAWO))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
6pinOpen Voltage	V_{6PIN}		3.6	4.0	4.4	V
Input Minimum D-Range	V_{LEHTV}	Minimum input voltage	-	-	3.81	V
Input Maximum D-Range	V_{HEHTV}	Maximum input voltage	4.75	-	-	V
EHT-V Correction Gain1	G_{EHTV1}	Between Vsawo to EHTV gain Vsize=FF	1.47	1.72	1.97	Times
EHT-V Correction Gain2	G_{EHTV2}	Between Vsawo to EHTV gain Vsize=01	1.65	1.92	2.19	Times

<Moire Canceller Unit>

Horizontal Moire Canceller Block(measurement at 17pin(HOUT))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
H Moire Canceller Variable1	T_{HMC1}	$HMC=01_{H,}$ fH=30kHz Ratio with period	0	2.8	5.0	ppm
H Moire Canceller Variable2	T_{HMC2}	$HMC=7F_{H,}$ fH=30kHz Ratio with period	170	200	230	ppm
H Moire Canceller Variable Amount	T_{HMC}	$T_{HMC2-}T_{HMC1}/126$	1.32	1.55	1.79	ppm

Vertical Moire Canceller Block (measurement at 4 pin(VSAWO))

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
V Moire Canceller Variable1	V_{VMC1}	$VMC=01_H$	0	0.4	0.8	mVp-p
V Moire Canceller Variable2	V_{VMC2}	$VMC=7F_H$	3.06	3.6	4.14	mVp-p
V Moire Canceller Variable Amount	V_{VMC}	$V_{VMC2-}V_{VMC1}/126$	24.09	28.35	32.60	uV/step

<Dynamic Focus Unit>

Horizontal/Vertical Mixed Dynamic Focus Block (measurement at 8pin)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
H-DF Amplitude1	V_{HDFMA1}	$HDFA=01_{HEX}$, 04_{HEX}D7="1"	0.3	0.5	0.7	Vp-p
H-DF Amplitude2	V_{HDFMA2}	$HDFA=7F_{HEX}$, 04_{HEX}D7="1"	1.5	2.0	2.5	Vp-p
H-DF Amplitude Amount	V_{HDFMA}	$V_{HDFMA2-}V_{HDFMA1}/126$	8.7	11.9	15.3	mV/step
H-DF Amplitude3	V_{HDFMA3}	$V_{HDFMA2,}$ HSIZE-Track=ON HSIZE=00_{HEX}	1.8	2.41	3.01	Vp-p
H-DF Amplitude4	V_{HDFMA4}	$V_{HDFMA2,}$ HSIZE-Track=ON HSIZE=FF_{HEX}	1.05	1.4	1.75	Vp-p
V-DF Amplitude1	V_{VDFMA1}	$VDFA=01_{HEX}$, 04_{HEX}D7="1"	0.3	0.5	0.7	Vp-p
V-DF Amplitude2	V_{VDFMA2}	$VDFA=01_{HEX}$, 04_{HEX}D7="1"	1.5	2.0	2.5	Vp-p
V-DF Amplitude Amount	V_{VDFMA}	$V_{VDFA2-}V_{VDFM1}/126$	8.7	11.9	15.3	mV/step
H-DF Phase1	V_{HDFP1}	$HDFP=00_{HEX}$	0.25	0.36	0.47	us
H-DF Phase2	V_{HDFP2}	$HDFP=7F_{HEX}$	0.70	1.00	1.30	us
H-DF Phase Amount	V_{HDFP}	$V_{HDFP2-}V_{HDFP1}/127$	3.6	5.1	6.6	ns/step

Vertical Dynamic Focus Block (measurement at 9pin)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
V-DF Amplitude1	V_{VDFA1}	VDFA=01_{HEX}, DFSelect="0"	0.6	1.0	1.4	Vp-p
V-DF Amplitude2	V_{VDFA2}	VDFA=$7F_{HEX}$, DFSelect="0"	3.0	4.0	5.0	Vp-p
V-DF Amplitude Amount	V_{VDFA}	V_{VDFA2-} V_{VDFA1} /126	18	24	30	mV/step

<PWM Unit>

Error AMP Block (measurement at pin12)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Input Low Voltage	V_{EINL}	Input V_{EIN} at pin11, short between pin11and pin12	0	0	0	V
Input High Voltage	V_{EINH}	input V_{EIN} at pin11, short between pin11 and pin12	4.5	5.0	5.5	V
Reference Voltage	V_{REF}	No signal at pin11, short between pin11 and pin12	2.25	2.5	2.75	V
Limit level	V_{LIM}	Input 6V at pin11, short between pin11 and pin12	4.5	5.0	5.5	V

PWM OSC Block (measurement at pin13)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Low level	V_L	Input 5V at pin11	0.8	1.0	1.2	V

PWM OUT Block(measurement at pin14)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
PWM Duty1	P_{D1}	f_H=30kHz, V_{12}=1V	94	99	100	%
PWM Duty2	P_{D2}	f_H=30kHz, V_{12}=2V	88	93	98	%
PWM Duty3	P_{D1}	f_H=30kHz, V_{12}=3V	81	86	91	%
PWM Duty4	P_{D4}	f_H=30kHz, V_{12}=4V	73	78	83	%
PWM Duty5	P_{D5}	f_H=30kHz, V_{12}=5V	65	70	75	%
PWM Duty1	P_{D1}	f_H=90kHz, V_{12}=1V	93	98	100	%
PWM Duty2	P_{D2}	f_H=90kHz, V_{12}=2V	74	79	84	%
PWM Duty3	P_{D3}	f_H=90kHz, V_{12}=3V	53	58	63	%
PWM Duty4	P_{D4}	f_H=90kHz, V_{12}=4V	30	35	40	%
PWM Duty1	P_{D1}	f_H=150kHz, V_{12}=1V	91	96	100	%
PWM Duty2	P_{D2}	f_H=150kHz, V_{12}=2V	60	65	70	%
PWM Duty3	P_{D3}	f_H=150kHz, V_{12}=3V	25	30	35	%

<X-RAY Det. Units>

X-RAY Det. Block (measurement at pin19)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Threshold Voltage	V_{XRAY}		4.8	5.0	5.2	V

Notice:
1.The period is the time, which excluded retrace width of V-SAW from the vertical period.
2.The Vertical C Correction is off mode.
3.The Vertical S Correction is off mode.
4.The Trapezoid Correction is off mode.
5.The Side Pin Correction is off mode.
6.The Side Pin Corner Top/Bottom Correction is off mode.
7.The Side Pin Corner Top Correction is center.
8.The Side Pin Corner Bottom Correction is center.
9.The Parallelogram Correction is off mode.
10.The Side Pin Balance Correction is off mode.
11.The Side Pin Corner Balance Top/Bottom Correction is off mode.
12.The Side Pin Corner Balance Top Correction is center.
13.The Side Pin Corner Balance Bottom Correction is center.
14.The precision of the D/A converter is as follows.
8bits DAC ： --1LSB ～ +2LSB
7bits DAC ： --1LSB ～ +1.5LSB

ORDERING INFORMATION

Part Number	Package
WT9051	**30-pin plastic shrink DIP (400 mil)**